Improving the Light Load Efficiency of a VI Chip® Bus Converter Array

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Introduction

Parallel arrays of the bus converters are often used in applications where the output power of a single bus converter is not sufficient for the maximum-load conditions. Parallel arrays are very efficient under high-load conditions, but can suffer from inefficiency under light-load or no-load operation. This note describes a mechanism that minimizes the power dissipation of a VI Chip bus converters array for no-load and light-load conditions, while maintaining all of the maximum-load performance. The scope of technique and discussion is limited to a maximum BCM® array size to six. Different techniques are possible for managing larger arrays which are beyond the scope of this application note.

Background

Simple Parallel Array of Bus Converters

In a simple parallel array of bus converters (Figure 1), the power input pins (+IN and –IN) and the power output pins (+OUT and –OUT) of each bus converter in the array are directly connected together. The PC pin of each bus converter are also connected together to allow for synchronous start up and shut down of each bus converter in the array. In this type of array, each bus converter start synchronously when the common PC pin is allowed to float and each bus converter will share the load current at all power levels from light load to full load.

Figure 1
Block Diagram of Parallel Bus Converter Array
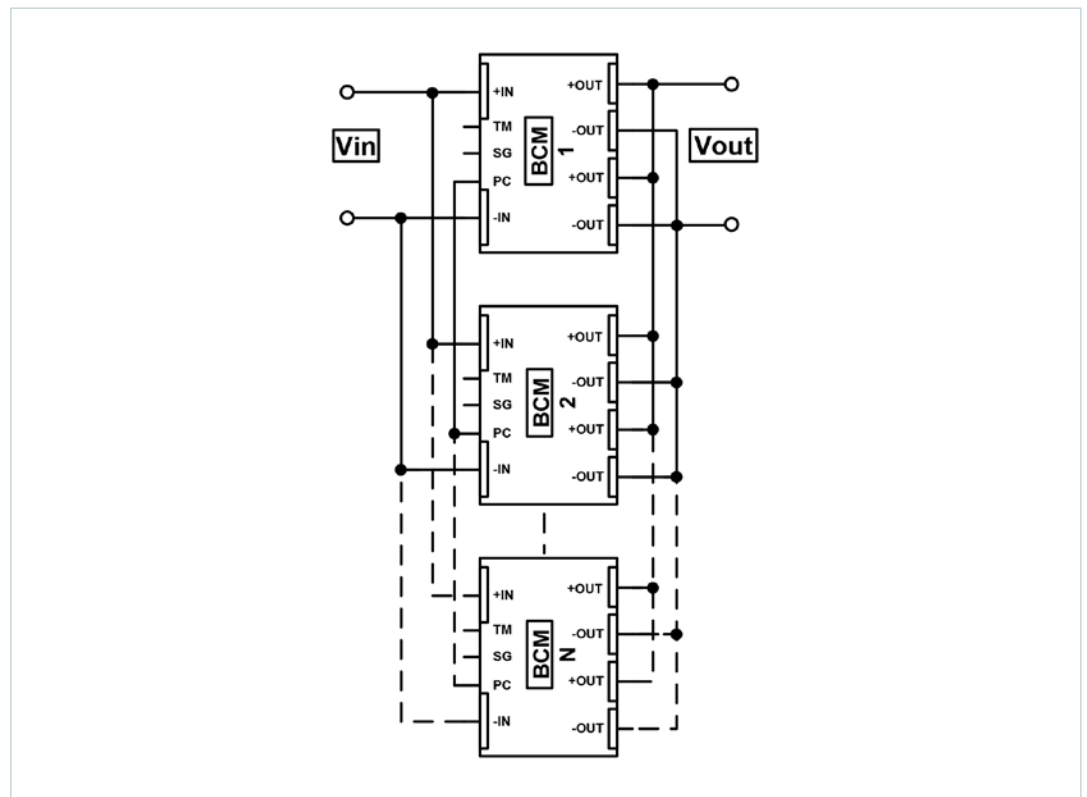
This simple paralleling of bus converters is commonly used in high-power DC-DC bus conversion. The advantages of this common practice are ease of design and lower components count. In such simple array, all of the bus converters are always on, which provides maximum current capability for dealing with fast-load current increases. On the other hand, it is not effective at limiting no-load power dissipation and improving the light-load efficiency.

Improving Light-Load Efficiency with Current-Sensing Control

Reducing the number of active bus converters in an array at no-load or light-load conditions will increase efficiency, since each active bus converter consumes a small but measurable amount of power at no-load and light-load operating conditions. The bus converters array that reduces the number of active bus converters as the load decreases and adds bus converters as the load increases, maximizes efficiency. Under low-power conditions, only one bus converter is enabled. As the load current increases the current-sensing control circuit switches on additional bus converters to share the load up to the maximum load current of the array.

The control circuit in this solution requires an input signal that is proportional to the load current and output signal that controls the primary reference PC pin of the bus converter. PC pin is used to enable or disable the bus converter module. The bus converter module (BCM®) is the fixed-ratio DC-DC converter which provides the step-down unregulated voltage conversion and step-up current conversion from primary to secondary side. Therefore, primary (input) current is proportional to secondary (output) load current. Proportionality constant is defined as the ratio of output voltage and input voltage. Therefore the primary current provides the indication of the secondary side-load current. The primary (input) referenced current sensing control circuit and primary referenced PC pin eliminates the need for an isolation device.

Using a technique we will call module-level current-sensing control, a designer can design an array where the primary current of each BCM is sensed by a single current-sense resistor inserted into the return path of the primary side (–IN) of each BCM. N-1 control circuits are required for an array of N BCMs. The input of each control circuit senses the input current proportional to the load current passing through the single-sense resistor, and its output enables or disables the next BCM in the array based on set threshold levels. The control circuits are designed such that the first BCM in the array is always enabled and additional BCMs are added as the load increases. Each control circuit would be designed to enable and disable the next BCMs as fixed power levels are reached on both increasing power and decreasing power.

This technique has several advantages. The design of the control circuits for each BCM is simpler due to commonality in the circuits, the sense resistors consume less power and the configuration offers more flexibility to the designer. Lower power dissipation in the current-sense resistors is critical because this results in smaller, less expensive components.

Figure 2 illustrates an array of bus converters designed to provide high output current and utilizing module-level current-sensing control to improve the light-load efficiency. This "Eco Array" implementation uses N-1 control circuits for the array of N BCMs. The input of the first control circuit senses the current passing through Rsense1, the current through the first BCM, and enables or disables the second BCM in the array based on the power level of the first BCM. The second control circuit senses the current passing through Rsense2, and enables or disables the third BCM in the array based on the power level of the second BCM. The current-sense resistor in the last BCM is not necessary for current sensing; it is added to balance the voltage drop in the return path of the input current to achieve better current-sharing accuracy when all BCMs are ON. The control circuits are also designed to disable BCMs sequentially when the sense resistors indicate that the load has decreased.

Figure 2

*Block Diagram of Parallel BCM
Array (the Eco Array)*
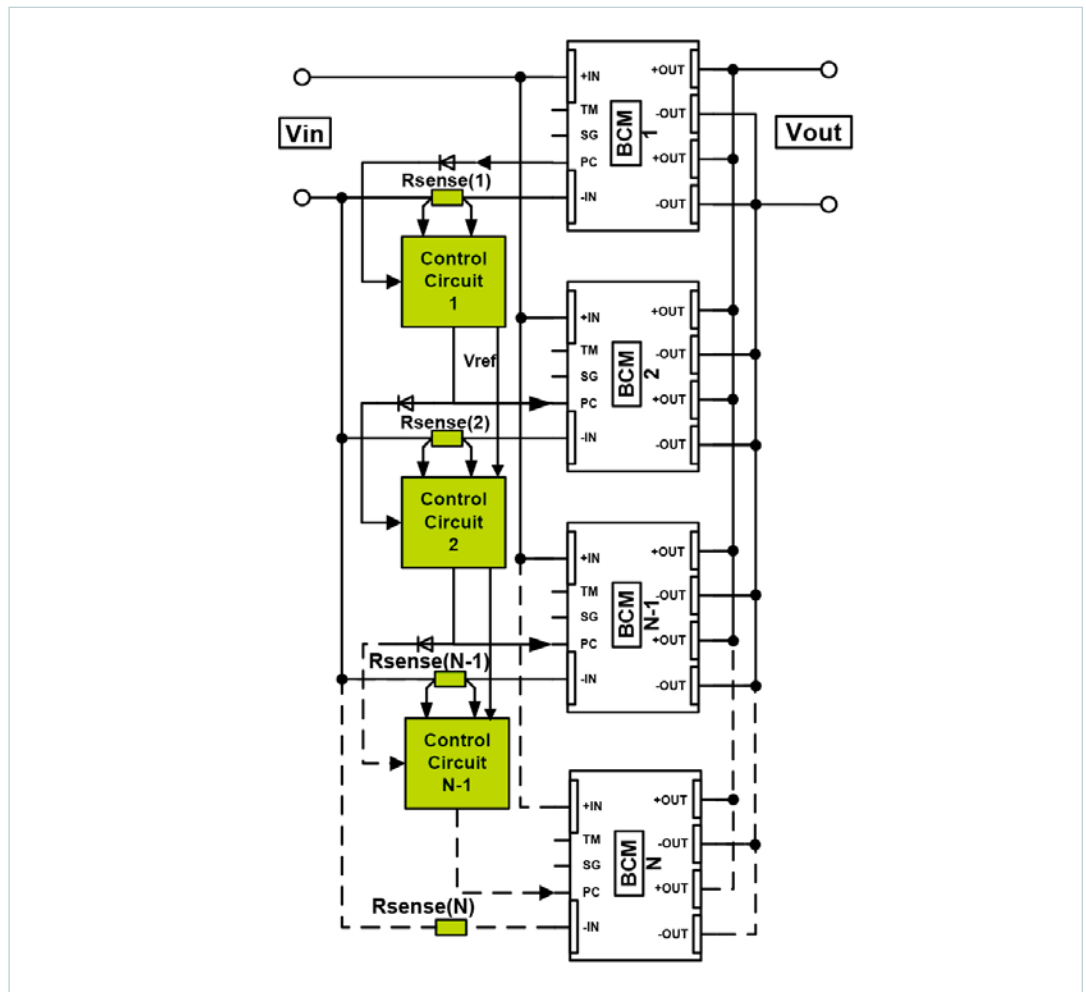
Let's understand the process to switch the BCM® on and off sequentially. At no load to 270 Watts input power, only BCM1 is active. As the current demand rises above 270 Watts, BCM2 switches on and the current is divided equally between BCM1 and BCM2. As the power from BCM2 increases above 270 Watts (total power of 540 Watts), BCM3 switches on and the power is divided among all three converters. So on and so forth.

As the total power drops below 1200 Watts, BCM6 will be ready to switch off and the current will be divided between BCM1 to BCM5 (240W each at 1200W). As the power decreases further, BCM5 will be ready to switch off at total power of 800 Watts and current will be divided between BCM1 to BCM4 (200W each at 800W). So on and so forth. Note that the current level at which BCM switches off is different from the level at which it is switched on. This is necessary to prevent BCM from repeatedly switching on and off due to the switching noise. It is important to keep the separation between lower switch (trip) points to prevent the overlap BCM turn-off events when load decreases. The design of the hysteresis in the comparator circuit is a very important part of the design.

Designing an Eco Array of Bus Converters

A reference schematic for Eco Array is shown in Figure 3 which shows the location of the current sensing control circuits to sense input current of each BCM® and control the next BCMs. The reference schematic for each control circuit block is shown in Figure 4. The system will spend a considerable time at low or no-load conditions; therefore the converter array is being designed for low-idle power using the module level current sensing control.

Selecting Appropriate BCM the Bus Converter from Product Listing

The BCM, an isolated fixed-ratio DC-DC bus-conversion module, is selected based on the following electrical parameters:

- Input voltage range

- Output voltage range

- Input to output voltage ratio

- Rated output power

To find a BCM to meet a particular design requirement, visit:
http://www.vicorpower.com/dc-dc-converters-board-mount/bus-converter-module

Array requires more than one BCM therefore calculate the number of BCM required in parallel array from the rated output power of single BCM with 5% de-rating to allow the mismatch in the load sharing and specified output power of the parallel array.

Choosing the Current-Sense Resistors

Figure 3 shows the location of current-sense resistors in the Eco Array with module level current-sensing control circuits. Current-sense resistor tolerances have a significant impact on the overall accuracy of the current sharing and set point voltages. It is critical to select these resistors with a tolerance consistent with the overall current sharing accuracy desired.

The value of the current-sense resistor must be large enough such that the voltage drop is considerably higher than the input offset voltage of the differential amplifier. The sense resistors contribute to overall power loss. Their values should be kept low to minimize power dissipation. The maximum value of the current-sense resistor based on maximum desired power dissipation is calculated using the following equation.

$$R_{SENSE} < \frac{P_{R_{SENSE\_MAX}} \bullet \left(V_{IN}\right)^2 \bullet \eta^2}{\left(P_{OUT\_MAX}\right)^2} \quad \Rightarrow \qquad (1)$$

$$R_{SENSE} < \frac{P_{R_{SENSE\_MAX}}}{\left(I_{IN\_MAX}\right)^2}$$

Where:

R_{SENSE} = Resistance of the current-sense resistor in ohms

$P_{R_{SENSE\_MAX}}$ = Allowed maximum power dissipation in each current-sense resistor in watts. One can allow up to 1W.

V_{IN} = Operating input voltage in volts

η = Efficiency of the bus converter at maximum output power

P_{OUT_MAX} = Maximum output power of the bus converter in watts

I_{IN_MAX} = Maximum input current of the bus converter in amps. It can be determined from the respective product data sheet.

All current-sense resistors should be equal for better load sharing.

Table 1 defines the value of current-sense resistor required for various BCMs.

Nominal Input Voltage of BCM	Current-Sense Resistor (mΩ)
384V (352V, 270V)	XmΩ
48V	X / 8mΩ

Five current-sense resistors are required for array of six. Last BCM® does not require the current-sense resistor, but it is inserted to improve the current-sharing accuracy of each BCM when all six BCMs are ON in the array. 384V nominal input BCM requires the XmΩ standard current-sense resistor. For same voltage drop and to use the same control circuit, 48V nominal input BCM requires X/8mΩ current-sense resistor for BCMs with same rated power. Select standard current-sense resistor for given input voltage and allowable power dissipation in resistor. Multiple resistors can be paralleled to get the desired resistor value.
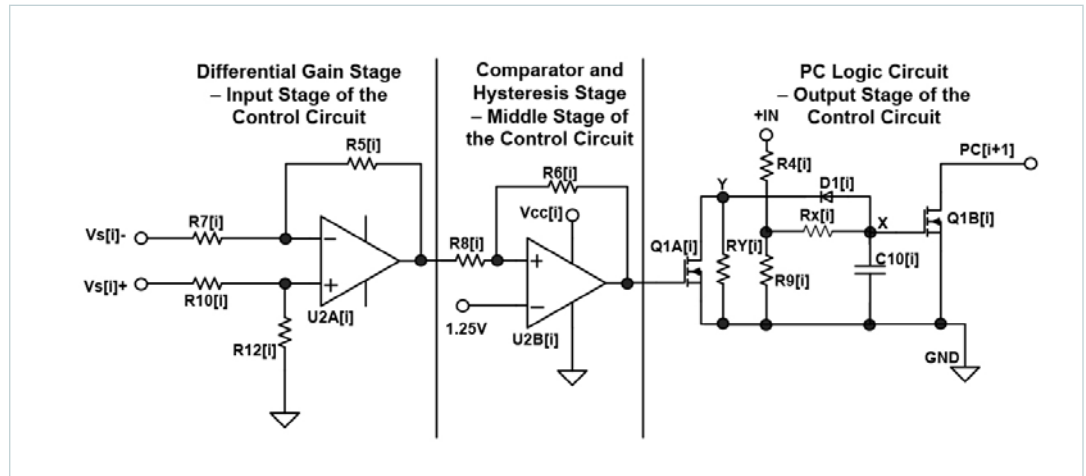
Figure 3

Eco Array of the Bus Converter Modules
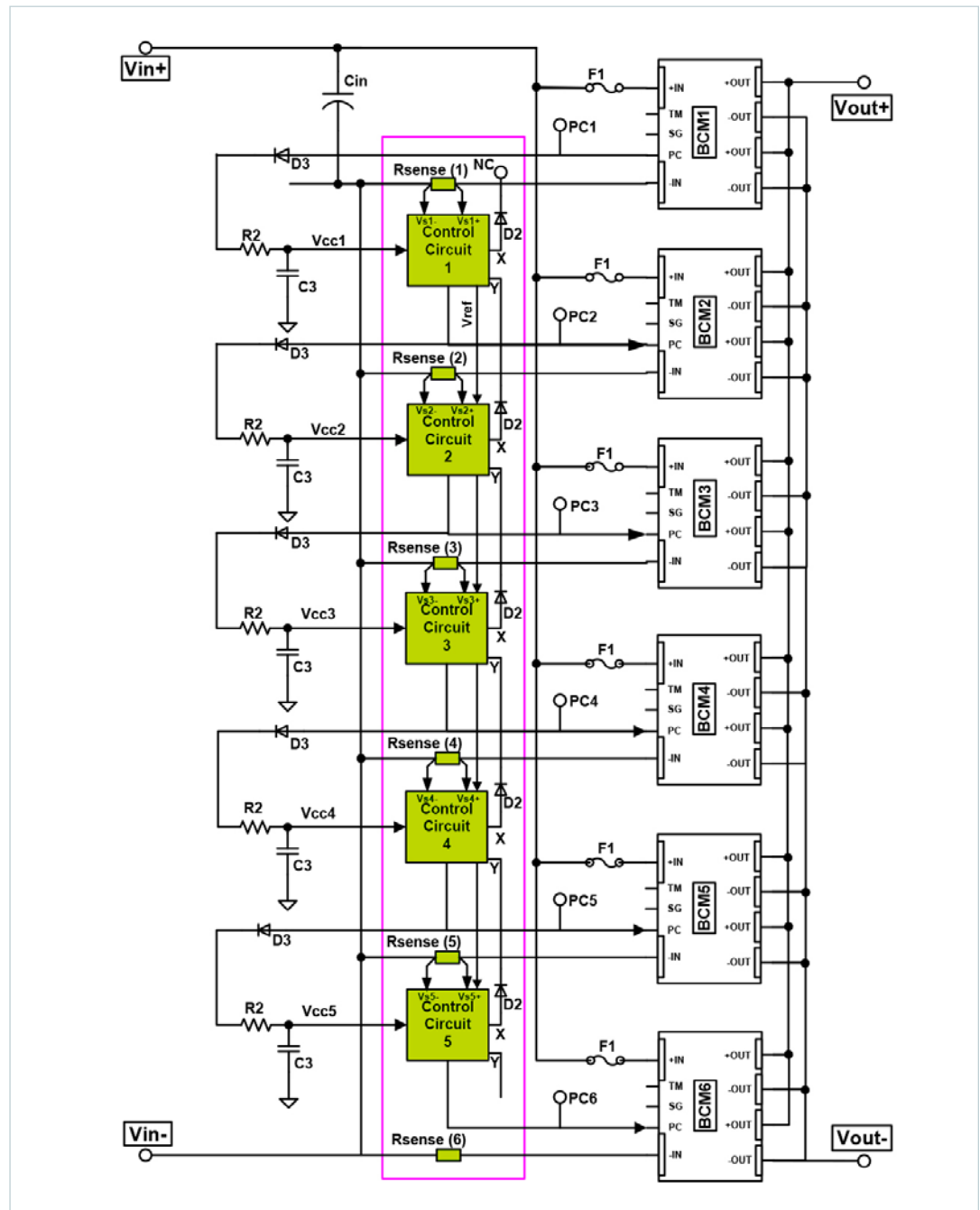
Designing the Control Circuits

Each of the control circuits has three blocks as shown in Figure 4. They are (1) the differential gain stage which is the input stage, (2) the comparator stage – which is the middle stage and (3) the PC logic circuit which is the output stage of the control circuit.

The BCM® PC pin provides a 5V voltage supply with 2.4mA current drive capability. Since the control circuits are very low power, the PC pin is capable of providing the supply voltage for the differential-gain circuit, comparator circuit and the voltage-reference circuit. The PC pin voltage eliminates need of an external power supply in the array by providing the V_{CC} power to control circuits. The external PC Logic circuit also uses a +IN rail to establish the proper logic.

The voltage reference IC (U1) is a precision, low-power and low drop out 1.25V voltage references which is available with accuracy of ±0.2%. The reference voltage is connected to the inverting terminal of the op-amp used in the comparator stage. An alternative reference can be substituted if higher precision is required, provided that the components are implemented properly. For more information, please follow the voltage reference data sheet. Figure 5 shows a circuit for generating a 1.25V voltage reference from the PC signal of first BCM in the array.
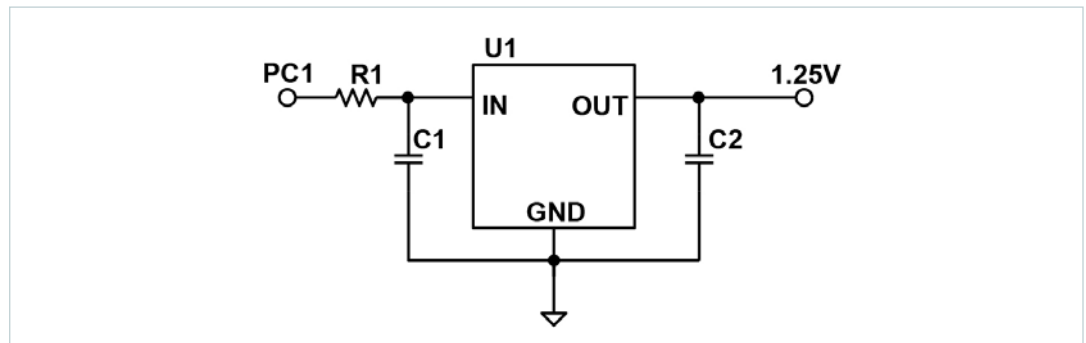
Selecting the Op-Amp for Differential Amplifier and Comparator Circuits

The op-amp (U2[i]) was selected due to its low input offset voltage, micro-power, cost and small package option, which allows the same part to be used for all of the designs recommended in this application note. If the use of a different part is desired, the user should evaluate the parameters of the device to ensure that it will function properly and not affect the overall performance.

A low-offset voltage is preferable because this, in combination with the sense resistor tolerance, will factor into the trip-point accuracy. Additional considerations include power dissipation, speed and output current sinking/sourcing capability. One should use an op-amp with micro power consumption. The op-amp output should have enough voltage capability to drive the gate of the logic MOSFET. Follow the op-amp manufacturer's data sheet on decoupling. In general, the op-amp supply terminal should always be bypassed locally with a low-ESR capacitor. Do not put more than 1000pF bypass capacitance directly at the PC pin of the BCM®. If more capacitance is required, it should be added with series resistance between the capacitor and the PC pin as shown in Figure 3.

Differential Gain Stage and Selecting the Gain Resistors

The voltage drop across the current sense resistor is low and the differential gain circuit boosts the signal to a level that will work with the comparator circuit. The op-amp is configured as a differential amplifier. The input resistors and feedback resistors set the differential voltage gain of the stage. Good common-mode rejection and wide common-mode voltage range are important because the amplifier works with large, changing common-mode signals.

Differential Gain Stage Control Circuit # i
The gain of the differential current-sense amplifier for ith control circuit is given by the following equation, with the assumption that $R_7[i] = R_{10}[i]$ and $R_5[i] = R_{12}[i]$.

$$A_V[i] = \frac{V_{OD}[i]}{V_{SENSE}[i]} = \frac{R_5[i]}{R_7[i]} = \qquad (2)$$

$$\left(\frac{V_{PC}}{P_{UTP}[i] - P_{LTP}[i]}\right) \cdot \left(\frac{R_8[i]}{R_6[i]}\right) \cdot \left(\frac{V_{IN}}{R_{SENSE}}\right)$$

Where:

$A_V[i]$ = Voltage gain of the differential-gain stage in control circuit # i

V_{PC} = PC voltage = 5V

$P_{UTP}[i]$ = BCM[i] input power at which control circuit #i output prepare to enable the BCM [i +1] = Upper trip point for the ith circuit

$P_{LTP}[i]$ = BCM[i] input power at which control circuit #i output prepare to disable the BCM [i +1] = Lower trip point for the ith circuit

$R_8[i]$ **and** $R_6[i]$ are hysteresis resistors in control circuit #i

V_{IN} = Operating input voltage

R_{SENSE} = Current-sense resistor

$V_{OD}[i]$ = Output voltage of the differential-gain amplifier in control circuit #i

$R_5[i]$ **and** $R_7[i]$ are the differential amplifier gain resistors in control circuit #i

$V_{SENSE}[i]$ = Voltage drop across the current-sense resistor in control circuit #i

Comparator Stage and Selecting the Hysteresis Resistors

The amplified-sense voltage is available at the differential-gain stage output. It is compared with the voltage reference in the comparator stage. The op-amp is configured as a comparator with hysteresis with the amplified-sense voltage present on the non-inverting input and the reference voltage at the inverting input. The comparator produces a logic-low to logic-high transition of output, when the amplified-sense voltage crosses above the voltage reference. This logic-high output will go to the positive supply rail of the op-amp. The comparator produces a logic-high to logic-low transition at the output, when the sense voltage at the non-inverting terminal of the op-amp crosses below the voltage reference. Positive feedback is also added around the comparator to generate the hysteresis. The amount of hysteresis is determined by the values of resistors (R6[i], R8[i]) and the 1.25V voltage reference. The following equation determines the resistors (R6[i], R8[i]) for ith control circuit.

Determining the Comparator Circuit Values of Control Circuit # i

$$\frac{R_6[i]}{R_8[i]} = \frac{V_{PC} \bullet P_{UTP}[i]}{\left(P_{UTP}[i] - P_{LTP}[i]\right) \bullet V_{REF}} - 1 \qquad (3)$$

Where:

V_{REF} = Reference voltage for comparator = 1.25V

All other variables are defined in Equation 2.

Following Table 2 provides the upper-trip points and lower-trip points for each control circuit to calculate the hysteresis resistors and differential-gain resistors. Non-percentage numbers are given as an example for 325W rated BCM®.

Table 2

Upper and Lower Threshold Levels for Six-Up Eco Array.

For i = 1 – 5	UTP in terms of Module Input Power	LTP in terms of Module Input Power
Control Circuit [1]	270W, (83%)	70W, (21.5%)
Control Circuit [2]	270W, (83%)	100W, (30.7%)
Control Circuit [3]	270W, (83%)	130W, (40.0%)
Control Circuit [4]	270W, (83%)	160W, (49.2%)
Control Circuit [5]	270W, (83%)	190W, (58.4%)

Selecting the MOSFETS for PC Logic Circuit

When switch Q1B[i] turns on, it pulls PC to SG and draws worst-case 5mA current through single BCM PC pin.

Gate threshold voltage is the key parameter for selection of MOSFET Q1A[i] and Q1B[i]. The gate threshold voltage for 2N7002V is 1.0V to 2.5V. The maximum rating for the gate-to-source voltage is 20V and drain-to-source voltage is 60V.

On-state drain current is one more key parameter for selection of Q1A[i] and Q1B[i] under transient conditions at corner points. It is good to know the transfer characteristic drain current vs. gate-to-source voltage at various junction temperatures, especially in low-threshold gate-to-source voltage range. The maximum rating for continuous-drain current is 280mA.

Selecting the Diodes, Resistors and Capacitors for PC Logic Circuit

The PC logic circuit drives the PC pin of the next BCM® in the array based on the comparator output. The PC Logic stage has an open-drain output that utilizes the internal pull-up resistor of the PC-pin. When the comparator output is logic-high, the BCM PC voltage is floating and the BCM is enabled. When the comparator output is logic-low, the BCM PC voltage is pulled low and the BCM is disabled. This circuit is designed using MOSFETs (Q1A[i], Q1B[i]) and resistors (R4 [i], R9 [i]).

R4 [i] and R9 [i] form a voltage divider between the BCM +IN supply rail and the gate of MOSFET Q1B[i] as shown in the schematic of Figure 4 and 8. The voltage at the gate of MOSFET Q1B is given by following equation when Q1A is OFF.

$$V_{G1} = \left(\frac{R_9}{R_9 + R_4} \right) \bullet \left(V_{IN} \right)$$

It is necessary to keep the gate of MOSFET Q1B above Vgs (max th) under start-up condition at less than minimum input voltage turn-on so the MOSFET Q1B turns on before the BCM1 turns ON and disables next BCMs by pulling PC LOW. Therefore, the following equation should be true in order for the minimum input voltage level to turn BCM2 OFF at no load.

$$\left(\frac{R_9}{R_9 + R_4} \right) \bullet \left(V_{IN\_MIN\_ON} \right) \geq V_{GS\_MAX\_TH}$$

$$R_9 \geq \frac{R_4}{\left(\frac{V_{IN\_MIN\_ON}}{V_{GS\_MAX\_TH}} - 1 \right)} \qquad\qquad (4)$$

Where:

$V_{IN\_MIN\_ON}$ = Minimum input voltage required to turn BCM on

$V_{GS\_MAX\_TH}$ = Maximum gate-to-source threshold voltage for selected MOSFET such as 2N7002V

One can also select these values for 4 – 5V gate-to-source voltage of MOSFET Q01B. Voltage across R4 resistor is in the range of HV BCM input voltages. Maximum voltage allowed across 2512 resistor is 500V. 1206 Resistor can be used for 48V nominal input BCMs. Diodes used in PC logic circuit can be small signal logic schottky type diode.

Understanding the Functionality of Two-BCM Turn-On for Positive Load Transient with Staggered BCM Turn-Off

This PC logic circuit is designed using MOSFETs Q1, resistors R4, R9 and Rx and capacitor C10 to generate delay on the falling edge of load. It is necessary to have a proper separation in delay for each control circuit to prevent the overlap events of BCM turn-off when load decreases. This circuit should also be designed keeping maximum toggle rate of PC in consideration. Sequential staggered turn-off of each BCM can be achieved by setting the proper time constant in the output stage of the control circuit. The first control circuit has the highest time constant and fifth control circuit has the lowest time constant for six-converter array.

To prevent the overlap turn-off due to the component tolerance in the output stage of the control circuit and to allow the minimum restart time [TON1] of the BCM as specified in the data sheet, it is important to keep BCM sequential turn-off slower than the turn-on and Eco Array requires, (1) Staggered sequential turn-off of all BCMs on falling edge of the load pulse with sufficient separation between adjacent BCMs, (2) Two bus converters turn-on instead of one for positive-load transient. This is described in timing diagram of Figure 6. Let's understand why this is important using following conceptual-timing diagram in Figure 7. Two-BCM turn-on for positive-load transient can also increase the reliability of bus converters by reducing the stress on each BCM in the array in comparison to single-BCM turn-on. This scenario for six-BCM array can be achieved using the circuit diagram of Figure 8. Following, Table 3 defines the time constant needed for each control circuit to generate the extended sequential turn-off. The conceptual timing diagram in Figure 6 is drawn for an array of six bus converters. It shows the load-current pulse and the outputs of control circuit 1 – 5, which are the PC inputs for BCM2 to BCM6 and indicates the turn-on and turn-off of the BCM2 to BCM6.
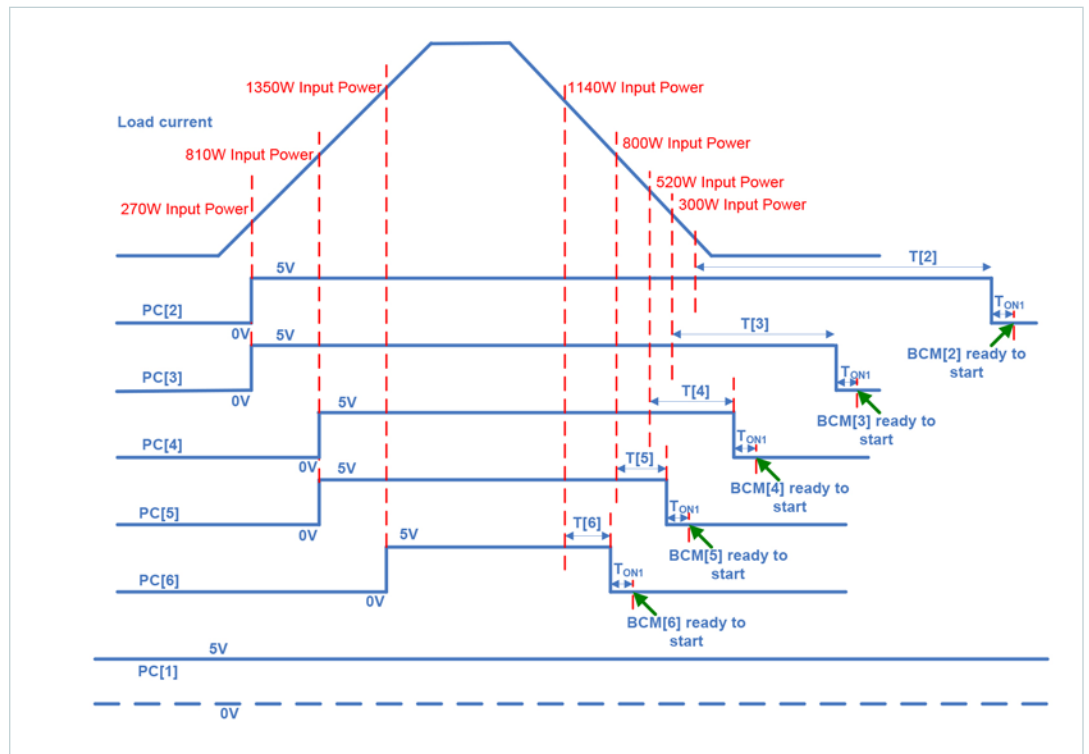
Figure 6
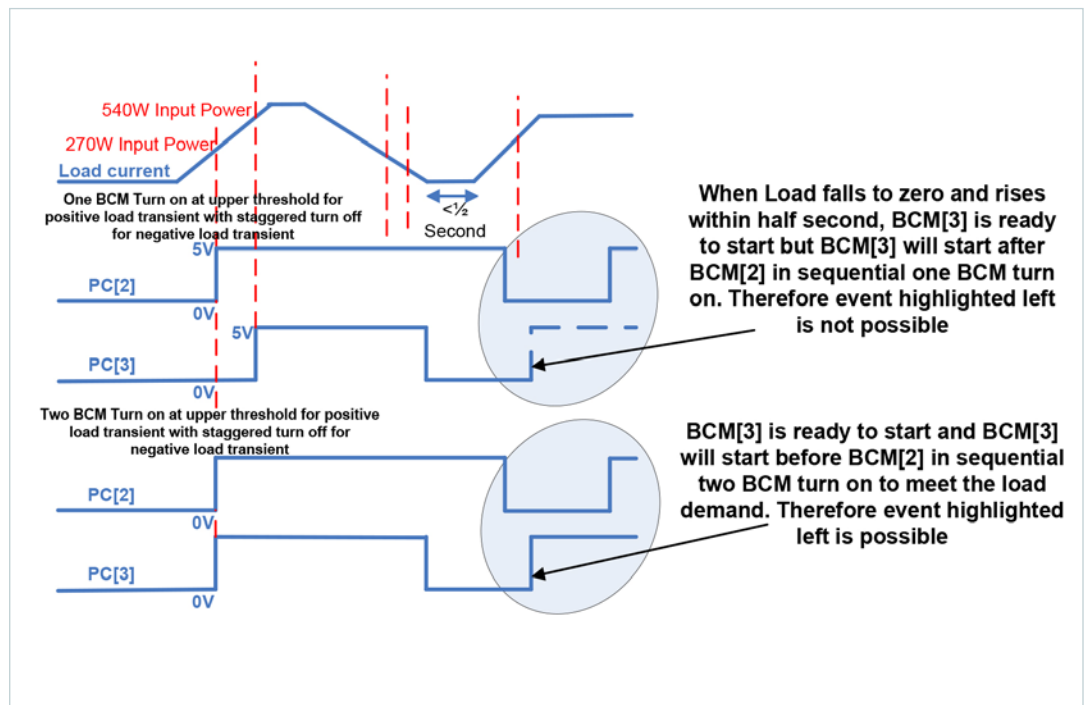Conceptual Timing Diagram
(Not to Scale)

Figure 6
Conceptual Timing Diagram
(Not to Scale)

Figure 7
Conceptual Timing Diagram
(Not to Scale)

Figure 7
Conceptual Timing Diagram
(Not to Scale)

Defining Needed Time Constant for Staggered BCM® Turn-Off

Voltage across capacitor C10 during charging and discharging is given by Equation 5 and Equation 6 respectively for five control circuits.

$$V_{CC10}[i] = V_{TH}[i]\left(1 - \ell^{\left(-\frac{t[i]}{\tau_C[i]}\right)}\right) \qquad (5)$$

Where,

$$R_{TH}[i] = \frac{R_4[i]R_9[i]}{R_4[i] + R_9[i]} + R_X[i] = R_X[i] \qquad (5a)$$

$$for\ R_4\|R_9 << R_X[i]$$

$$V_{TH}[i] = V_{IN}\left(\frac{R_9[i]}{R_4[i] + R_9[i]}\right) = 4V \qquad (5b)$$

(Keep $V_{TH}[i]$ above the 2.5V maximum threshold of MOSFET Q1B[i])

$$\tau_C[i] = R_{TH}[i]\ C_{10}[i] \qquad (5c)$$

$$V_{DC10}[i] = V_{TH}[i]\left(\ell^{\left(-\frac{t[i]}{\tau_D[i]}\right)}\right) \qquad (6)$$

Where,

$$\tau_D[i] = R_{DSON}\ C_{10}[i]$$

Table 3
Defines the Time Constant Needed for Staggered BCM Turn-Off for Six-Up Array

	Time Constant Needed for Staggered BCM Turn-Off	Minimum Time to Reach the $V_{GSTHMIN}$ = 1V to Turn MOSFET Q1B[i] ON Using Equation 5	Typical Time to Reach the $V_{GSTHTYP}$ = 1.76V to Turn MOSFET Q1B[i] ON Using Equation 5	Maximum Time to Reach the $V_{GSTHMAX}$ = 2.5V to Turn MOSFET Q1B[i] ON Using Equation 5
Control Circuit [5]	2 seconds	0.575 second	T6 = 1.159 seconds	1.962 seconds
Control Circuit [4]	8 seconds	2.301 seconds	T5 = 4.638 seconds	7.847 seconds
Control Circuit [3]	28 seconds	8.055 seconds	T4 = 16.234 seconds	27.463 seconds
Control Circuit [2]	97 seconds	27.905 seconds	T3 = 56.242 seconds	95.140 seconds
Control Circuit [1]	333 seconds	95.798 seconds	T2 = 193 seconds	326.616 seconds

Figure 8

*Control Circuit Diagram for*

Six-Up Array
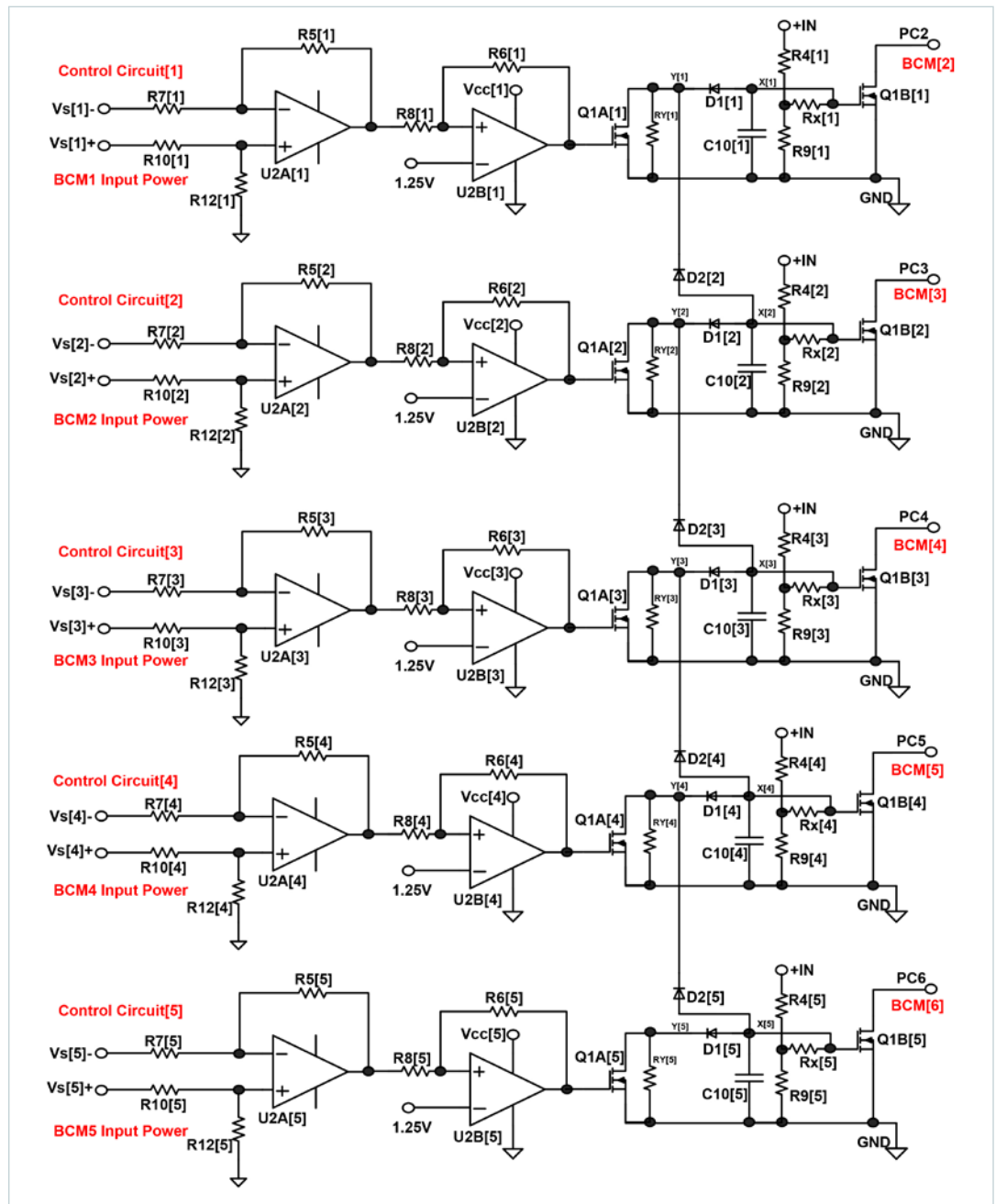
How a Control Circuit Works

Let's understand how a circuit in Figure 8 works for ECO Array of six bus converters. At no load to 270W input power, only BCM1 is active. As the current demand rises above 270W input power, output of the comparator in the first control circuit transition from logic low to logic high, capacitor C10 in the first control circuit discharged through diode D1 and R_{DSON} of MOSFET Q1A in the first control circuit and MOSFET Q1B in the first control circuit turns off and switches the BCM2 ON. The first control circuit primarily enables the BCM2. But at the same time capacitor C10 in the second control circuit discharge through diode D2 in second control circuit and R_{DSON} of MOSFET Q1A in the first control circuit and MOSFET Q1B in the output stage of the second control circuit turns off and switches the BCM3 ON. BCM2 and BCM3 switch on and the current is divided equally between BCM1, BCM2 and BCM3 (90W each at 270W input power). Lower threshold of control circuit 1 has to be at least 10W lower than 90W for proper functionality of the array. BCM1, BCM2 and BCM3 share the load up to 810W input power. At 810W input power, output of the comparator in the second and third control circuit transition from logic low to logic high, capacitor C10 in the third control circuit discharged through diode D1 and R_{DSON} of MOSFET Q1A in the third control circuit. Same capacitor C10 in the third control circuit also discharged through D2 in third control circuit and R_{DSON} of MOSFET Q1A in the second control circuit and MOSFET Q1B in the third control circuit turns off and switch the BCM4 ON.

The third control circuit primarily enables the BCM4. But at the same time capacitor C10 in the fourth control circuit discharged through the D2 in the fourth control circuit and R_{DSON} of MOSFET Q1A in the third control circuit and MOSFET Q1B in the output stage of the fourth control circuit turns off and switch the BCM5 ON. BCM4 and BCM5 switch ON and the current is divided equally between BCM1, BCM2, BCM3, BCM4 and BCM5 (162W each at 810W input power). Lower threshold of control circuit 1 – 3 has to be at least 10W lower than 162W for proper functionality of the array. BCM1, BCM2, BCM3, BCM4 and BCM5 share the load up to 1350W input power. At 1350W input power, output of the comparator in the fourth and fifth control circuit transition from logic low to logic high, capacitor C10 in the fifth control circuit discharges through diode D1 and R_{DSON} of MOSFET Q1A in fifth control circuit. Same capacitor C10 also discharged through diode D2 in the fifth control circuit and R_{DSON} of the MOSFET Q1A in the fourth control circuit and MOSFET Q1B in the output stage of the fifth control circuit turns off and switches the BCM6 ON. BCM6 switch ON and the current is divided equally between all six BCMs® (225W each at 1350W input power). Lower threshold of control circuit 1 – 5 has to be at least 10W lower than 225W for proper functionality of the array. All six BCMs share the load up to 1950W full load power. Hysteresis diagram for above circuit is shown in Figure 9 for array of six bus converters.

Figure 9
Hysteresis Diagram
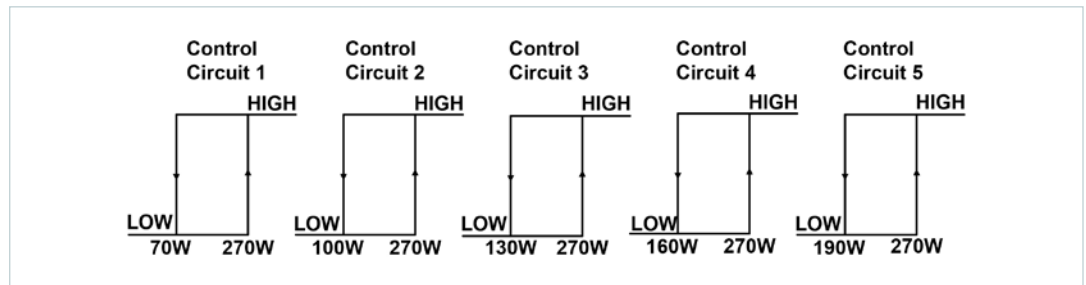
As the total input power drops to 1140W (190W times 6), comparator output in the fifth control circuit transitions from high logic to low logic. BCM6 is ready to switch off and the current will be divided between BCM1 to BCM5 (228W each at 1140W input power) after staggered BCM6 turn-off. As the input power decreases further to 800W (160W times 5), comparator output in the fourth control circuit transitions from high logic to low logic. BCM5 is ready to switch off and current will be divided between BCM1 to BCM4 (200W each at 800W input power) after staggered BCM5 turn-off. As input power decreases further to 520W (130W times 4), comparator output in the third control circuit transitions from high logic to low logic. BCM4 is ready to switch off and current will be divided between BCM1 to BCM3 (173.33W each at 520W input power) after staggered BCM4 turn-off. As input power decreases further to 300W (100W times 3), comparator output in the second control circuit transitions from logic high to logic low. BCM3 is ready to switch off and current will be divided between BCM1 to BCM2 (150W each at 300W input power) after staggered BCM3 turn-off. As the input power further decreases to 140W (70W times 2), comparator output in the first control circuit transitions from logic high to logic low. BCM2 is ready to switch off and current will be transferred to BCM1 (at 140W input power) after staggered BCM2 turn-off. Note that the current level at which BCM switches off is different from the level at which it is switched on. This is necessary to prevent BCM from repeatedly switching on and off due to the switching noise. It is important to keep the enough separation between lower-switch (trip) points of all circuits to prevent the overlap BCM turn-off events when load decreases. The design of the hysteresis in the comparator circuit is a very important part of the design.

Design Considerations

Application note AN: 005 provides board layout guidelines for using VI Chip® components. Additional consideration must be given to the external control circuit components. The current-sense resistor voltage – on the order of milivolts – is highly sensitive to noise. The control circuit should be located as close as possible to the sense resistor to minimize noise pick up through the sense lines. A four-terminal Kelvin contact is recommended for best results, eliminating the error caused by solder resistance from the resistor to the current-carrying connection on the PCB. The control signal from the sense circuit to the BCM should be shielded by enclosing them between power planes, power and ground plane or ground planes. Avoid grounding of the control circuits both side of the low side current-sense resistor to prevent a short circuit and to allow the single-point ground reference for each control circuit that ties together the input-supply ground.

Keep the output power plane as symmetrical as possible at the output for better current-sharing accuracy. Use of wider traces for power planes (+IN, –IN, +OUT, –OUT) is recommended to allow more current. Cu thickness less than 1oz should be avoided due to current density in the traces. Resistance introduced by power traces particularly on the output of the BCM® can be minimized by allocating the multiple layers for current-carrying traces, assigning 2 – 3oz Cu weight to current-carrying traces and using wider and shorter current-carrying traces.

The worst-case PC-to-V_{OUT} enable delay is 240ms (T1) for B384F120T30. The delay from the upper-trip point to PC high is 0.2ms. Total delay is 240.2ms. Delay limits the load-current slew rate to 20.8A/s. If the load-current slew rate is more than 20.8A/s, then it's possible that the load current will hit the BCM power limit (current limit) and the BCM can go through the restart sequence. It is necessary to apply load with a slew rate of less than 20.8A/s to prevent a multiple restart situation.

The worst-case PC-to-V_{OUT} enable delay is 150µs for a VTM2-based BCM such as VIB0002TFJ. It is recommended that load-current slew rates are more than 20.8A/s and less than 21A/ms. Addition of C10 can also affect the BCMs turn-off during the falling edge of load current. So VTM1 based designs are beyond the scope of this app note. Keeping more than one BCM ON at no load at some cost of light load efficiency can increase the load-current slew rate further. So there is a tradeoff between light-load efficiency and slew-rate of the load current. In addition, increase in the upper-threshold levels also puts the maximum limit on load-current slew rate. All these points needs to be considered while designing the control circuits for proper operation.

The Eco Array using module current-sensing technique (as shown here) limits the number of bus converters in the array to six. Different design techniques can be incorporated to increase the number of bus converters in a parallel array, but they are beyond the scope of this application note. Following hysteresis number in Figure 10 with six control circuits can increase the number of bus converters in the array to seven.

Figure 10
Hysteresis Diagram
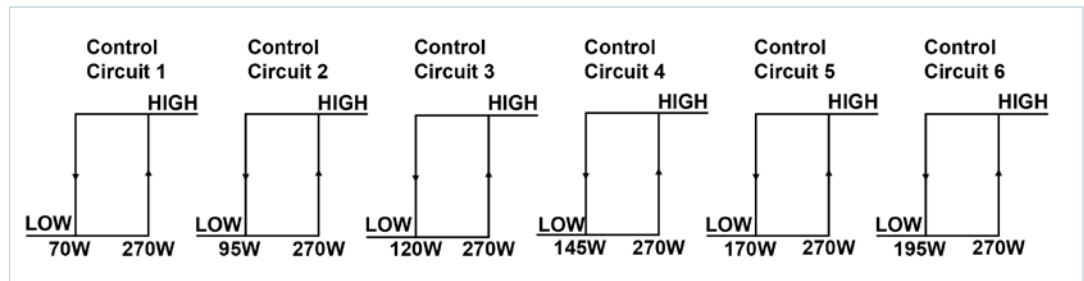
Six-sigma accuracy of upper and lower threshold levels can be improved by selecting lower-tolerance resistors, using a high-precision voltage reference, minimizing variations in input voltage and PC voltage and using a lower offset voltage op-amp with good common-mode rejection and wide common-mode voltage range for amplifier.

Efficiency and Power Dissipation for Six-Up Eco Array and Simple Parallel Array

Figure 11 compares the efficiency of a simple-parallel array with that of an Eco Array of Six 384V – 48V BCMs® over the output-power range. The light-load efficiency can be improved up to 20% under light-load conditions using eco array. Figure 12 shows that no-load power dissipation of eco array is lower by 31W for six 384V – 48V BCMs using the module current-sensing technique.

Figure 11
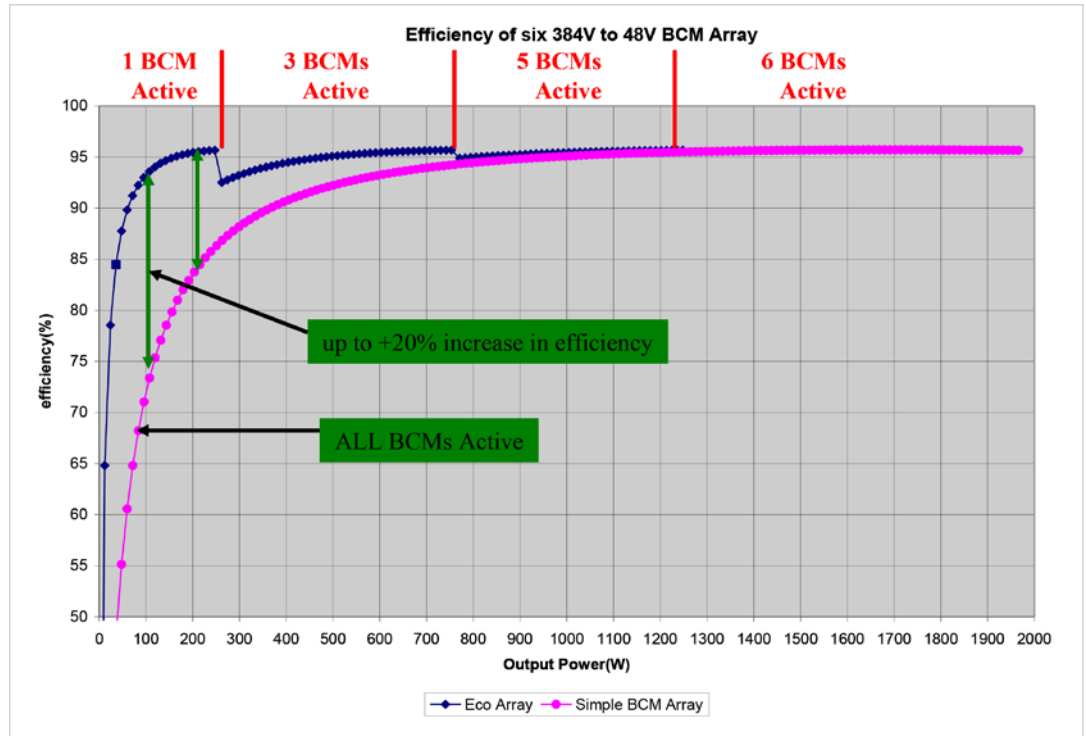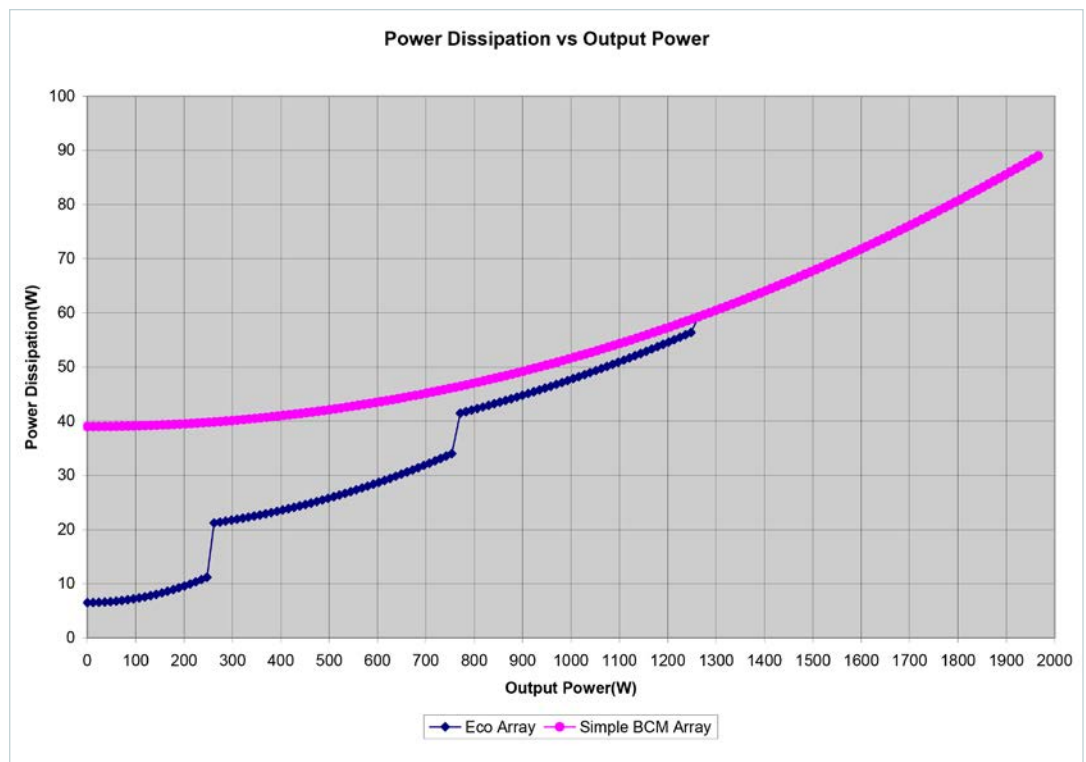*Efficiency of Eco Array and*
Simple Parallel Array

Figure 12
Power Dissipation in Eco Array
and Simple Parallel Array

Design Example

An application requires the bus converters be placed in parallel for higher power up to 1800W. A 384V nominal output voltage of PFC front-end drives the bus converter array. The output of the bus converters array drives 48V nominal input voltage load.

Selecting Appropriate BCM® from Product listing

Ratio of input voltage to output voltage is close to 8. The BCM384F480T325A00 provides a fixed ratio of 8 and 325W rated output power. Operating 384V input voltage falls within the input voltage range of BCM384F480T325A00 as specified in the product data sheet. Operating 48V output voltage also falls within the output voltage range of the BCM384F480T325A00.

Determine the number of BCMs required in parallel array

N = number of bus converters required in the parallel array = $\dfrac{1800W}{0.95 \bullet 325W} = 5.82 = 6$

Choosing the Current-sense Resistors

Using Equation 1

$$R_{SENSE} < \frac{P_{R_{SENSE\_MAX}}}{\left(I_{IN\_MAX}\right)^2} = \frac{0.25}{1^2} = 0.25\Omega$$

Choose the standard current-sense resistor value lower than 0.250Ω.

All current-sense resistors are equal to 0.1Ω 1% 1W rated.

Selecting the Components Value for five Control Circuits for 384 V input voltage

Selecting the Hysteresis Resistors R_6 and R_8

Using Equation 3 and Table 2

$$\frac{R_6[i]}{R_8[i]} = \frac{V_{PC} \bullet P_{UTP}[i]}{\left(P_{UTP}[i] - P_{LTP}[i]\right) \bullet V_{REF}} - 1$$

1st Control Circuit

$$\frac{R_6[1]}{R_8[1]} = \frac{5V \bullet 270W}{\left(270W - 70W\right) \bullet 1.25V} - 1 = 4.4 \implies R_8[1] = 10k\Omega,\ 1\% \implies R_6[1] = 44.2k\Omega,\ 1\%$$

2nd Control Circuit

$$\frac{R_6[2]}{R_8[2]} = \frac{5V \bullet 270W}{\left(270W - 100W\right) \bullet 1.25V} - 1 = 5.3529 \implies R_8[2] = 10k\Omega,\ 1\% \implies R_6[2] = 53.6k\Omega,\ 1\%$$

3rd Control Circuit

$$\frac{R_6[3]}{R_8[3]} = \frac{5V \bullet 270W}{\left(270W - 130W\right) \bullet 1.25V} - 1 = 6.7142 \implies R_8[3] = 10k\Omega,\ 1\% \implies R_6[3] = 66.5k\Omega,\ 1\%$$

4th Control Circuit

$$\frac{R_6[4]}{R_8[4]} = \frac{5V \bullet 270W}{\left(270W - 160W\right) \bullet 1.25V} - 1 = 8.8181 \implies R_8[4] = 10k\Omega,\ 1\% \implies R_6[4] = 88.7k\Omega,\ 1\%$$

5th Control Circuit

$$\frac{R_6[5]}{R_8[5]} = \frac{5V \bullet 270W}{\left(270W - 190W\right) \bullet 1.25V} - 1 = 12.5 \implies R_8[5] = 10k\Omega,\ 1\% \implies R_6[5] = 124k\Omega,\ 1\%$$

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Selecting the Differential Current-Sense Amplifier Resistors R_5 and R_7 for 384V Input Voltage

Using Equation 2, Table 2 and hysteresis resistors $R_6[i]$ and $R_8[i]$

$$\frac{R_5[i]}{R_7[i]} = \left(\frac{V_{PC}}{P_{UTP}[i] - P_{LTP}[i]}\right) \bullet \left(\frac{R_8[i]}{R_6[i]}\right) \bullet \left(\frac{V_{IN}}{R_{SENSE}}\right)$$

1st Control Circuit

$$\frac{R_5[1]}{R_7[1]} = \left(\frac{5V}{270W - 70W}\right) \bullet \left(\frac{1}{4.4}\right) \bullet \left(\frac{384V}{0.1\Omega}\right) = 21.8181 \Rightarrow R_7[1] = 10k\Omega, 1\% \Rightarrow R_5[1] = 221k\Omega, 1\%$$

2nd Control Circuit

$$\frac{R_5[2]}{R_7[2]} = \left(\frac{5V}{270W - 100W}\right) \bullet \left(\frac{1}{5.3529}\right) \bullet \left(\frac{384V}{0.1\Omega}\right) = 21.0991 \Rightarrow R_7[2] = 10k\Omega, 1\% \Rightarrow R_5[2] = 210k\Omega, 1\%$$

3rd Control Circuit

$$\frac{R_5[3]}{R_7[3]} = \left(\frac{5V}{270W - 130W}\right) \bullet \left(\frac{1}{6.7142}\right) \bullet \left(\frac{384V}{0.1\Omega}\right) = 20.4258 \Rightarrow R_7[3] = 10k\Omega, 1\% \Rightarrow R_5[3] = 205k\Omega, 1\%$$

4th Control Circuit

$$\frac{R_5[4]}{R_7[4]} = \left(\frac{5V}{270W - 160W}\right) \bullet \left(\frac{1}{8.8181}\right) \bullet \left(\frac{384V}{0.1\Omega}\right) = 19.7940 \Rightarrow R_7[4] = 10k\Omega, 1\% \Rightarrow R_5[4] = 196k\Omega, 1\%$$

5th Control Circuit

$$\frac{R_5[5]}{R_7[5]} = \left(\frac{5V}{270W - 190W}\right) \bullet \left(\frac{1}{12.5}\right) \bullet \left(\frac{384V}{0.1\Omega}\right) = 19.2 \Rightarrow R_7[5] = 10k\Omega, 1\% \Rightarrow R_5[5] = 191k\Omega, 1\%$$

Selecting the Resistors and Capacitors for PC Logic Circuit for 384V Input Voltage

Using Equation 4 and 5b, R4 and R9 are selected:

$$R_9 \geq \frac{R_4}{\left(\dfrac{V_{IN\_MIN\_ON}}{V_{GS\_MAX\_TH}} - 1\right)} \Rightarrow \frac{R_9}{R_4} \geq \frac{1}{\dfrac{290}{2.5} - 1} = \frac{8.6956}{1000}$$

$$\Rightarrow R_4 = 1M\Omega, 1\%, 1W, 2512$$

$$\Rightarrow R_9 \geq 8.6956k\Omega$$

Using Equation 5b,

$$V_{TH}[i] = V_{IN}\left(\frac{R_9[i]}{R_4[i] + R_9[i]}\right) \Rightarrow 4V = 384V\left(\frac{R_9}{1M\Omega + R_9}\right) \Rightarrow R_9 = 10.5k\Omega, 1\%$$

Selecting the Resistors RX[i] and Capacitors C10[i] using Equation 5a and 5c for Needed Time Constant for Staggered BCM Turn-Off as Specified in Table 3

$$\tau_C[i] = R_X[i]\, C_{10}[i]$$

1st Control Circuit
$$\tau_C[1] = R_X[1]\, C_{10}[1] = 333 \Rightarrow R_X[1] = 1.6M\Omega \Rightarrow C_{10}[1] = 208.125\mu F$$

2nd Control Circuit
$$\tau_C[2] = R_X[2]\, C_{10}[2] = 97 \Rightarrow R_X[2] = 1.6M\Omega \Rightarrow C_{10}[2] = 60.625\mu F$$

3rd Control Circuit
$$\tau_C[3] = R_X[3]\, C_{10}[3] = 28 \Rightarrow R_X[3] = 1.6M\Omega \Rightarrow C_{10}[3] = 17.5\mu F$$

4th Control Circuit
$$\tau_C[4] = R_X[4]\, C_{10}[4] = 8 \Rightarrow R_X[4] = 1.6M\Omega \Rightarrow C_{10}[4] = 5\mu F$$

5th Control Circuit
$$\tau_C[5] = R_X[5]\, C_{10}[5] = 2 \Rightarrow R_X[5] = 1.6M\Omega \Rightarrow C_{10}[5] = 1.25\mu F$$

For all control circuit
$$R_Y[i] = (6.25 \text{ to } 10) \cdot R_X[i] \Rightarrow R_Y[1] = R_Y[2] = R_Y[3] = R_Y[4] = R_Y[5] = 10M\Omega$$

Eco Array Demonstration System

The designed Eco Array demonstration system, for proof of concept, has an interesting feature that allows the system to shut down the unused bus converters at no load and light load and bring them up as load demands. This would benefit the light-load efficiency of parallel bus converters. This system has ability to manage up to a total of six bus converters. With the system's ability to monitor the input current of each bus converter, it is possible to control each bus converter to meet the needs of the load. In light-load condition, it is possible for the eco array system to turn-off five out of six bus converters which will improve the efficiency at light-load operating conditions.

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