Designing High-Power Arrays Using Maxi, Mini and Micro Family DC-DC Converters

Introduction

Vicor's Maxi, Mini and Micro DC-DC converters are designed for easy paralleling to increase output power. The unique paralleling interface allows multi-kW capable designs to be implemented with few external components. For information on paralleling up to 12 modules, see the Application Note "Converter PR Pin Facilitates Parallel Operation for Power Expansion or Redundancy". For very high-power arrays of more than 12 modules, buffering of the PR signal is required as the fan-out limit of the communication bus is reached. This note describes how to use buffering to increase the capability of the bus to drive large numbers of converters, and gives an example of how to quickly prototype a multi-kW system. This allows the benefits of the Maxi, Mini and Micro family to be applied for systems with output power into the multi-kW range.

PR Bus Architecture

Master / Slave Configurations

One of the first decisions that must be made when designing large arrays is to define the number of master modules. Large numbers of possible masters will increase redundancy but complicate PR and +S/–S line busing. Initially it may be tempting to configure all modules in a democratic array, but this may become cumbersome for arrays of greater than three modules. For large arrays a better choice is to define up to three modules as masters and add additional slaves for more power. This provides adequate redundancy for most applications.

Distribution Across Multiple Boards

It is often necessary to break an array of converters into multiple PC boards due to space and thermal requirements. Separation between boards will introduce additional impedance between the converters because of added lead/trace length. To keep interconnect impedance between boards from corrupting the control signals, Vicor's PR isolation transformer (Vicor P/N 29768) must be used to isolate the PR bus. It is recommended that all masters be located on the same board. This keeps noise and line delay between the masters to a minimum. This is especially important for very large arrays that will be subject to high di/dts and dv/dts. If an application requires redundancy between boards or between more than 12 modules, a bidirectional buffer must be implemented. This is beyond the scope of this note.

The PR signal should be bussed between boards with a relatively lossy low-inductance connection. Twisted pair works well while coaxial cable is not appropriate. Reflections caused by the mismatch of PR bus source, load, and cable impedance will not be damped by the low-loss coaxial cable and result in reduced quality of the PR pulse.

Buffering

High-speed buffering may be required with large arrays or if the distance between modules is greater than a few inches. This is because all modules, except the one that's talking, are in the listening mode. Each listener presents a load to the master (talker) of approximately 500 Ω shunted by 30 pF; see Figure 1. Long leads for the interconnection introduce losses and parasitic reactance on the bus that can attenuate and distort the sync-pulse signal. The bandwidth of the bus must be at least 60 MHz.

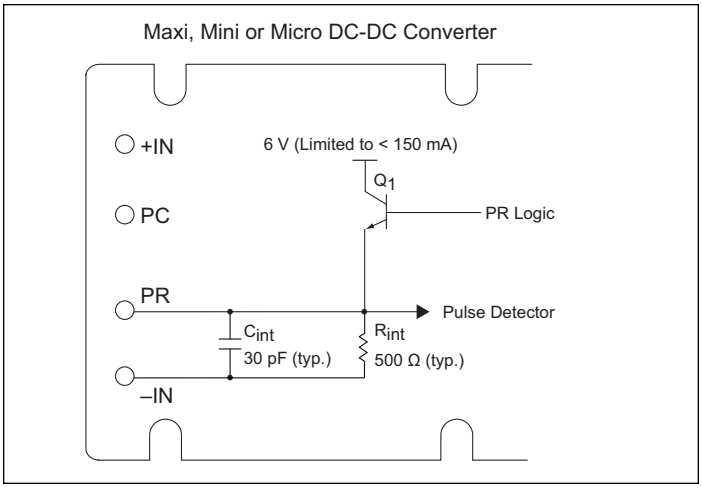

Figure 1 — PR pin equivalent circuit

One simple and robust PR buffer scheme is shown in Figures 2 and 3. The system is separated into one master board (Figure 2) and a number of slave boards (Figure 3). The master board consists of five modules. Two of these are configured in a democratic array with one trimmed down by 2% relative to the other. These modules drive two buffers. The first buffer (Q_2) drives three additional slave modules on the master board. The second drives the slave boards. Each slave board contains five modules that are configured as slaves by tying their SC pins to –S. There is a PR isolation transformer on each slave board that isolates the incoming PR signal. This signal is then buffered and fed to each slave module.

The buffers are basic emitter followers that use general-purpose NPN transistors. Transformers labeled T_1 have 1:1 turns ratios and can be implemented by using Vicor's PR isolation transformer with one coil left open circuited. Transformers labeled T_2 have turns ratios of 2:1 to give better matching to the PR distribution bus. The return path for each transformer or buffer must be Kelvin connected to the –IN pin of the appropriate converter. An 8 V auxiliary supply gives sufficient headroom for the followers. It is a low-power rail that can be derived from a higher voltage using a linear regulator. A separate auxiliary supply must be derived on each board so that PR bus isolation is maintained. The high frequency bypassing directly at each buffer is essential.

Because of the high speed of the PR signal careful attention must be paid to the signal fidelity of the PR bus. Locations for both series and shunt damping resistors or ferrite beads should be included in the layout as shown in Figures 2 and 3. Populating all of these components may not be necessary for all arrays depending on the geometry of the PR bus. Both master and slave modules should have reverse-polarity protection diodes (D_1) on the PR pins.

Bypassing

Selection of bypassing components has important consequences for stability and EMI performance of high-power arrays. Common-mode bypassing for each converter should be implemented as shown in the Design Guide and Application Manual for the Maxi, Mini and Micro family.

Differential-mode bypassing can be considered in two parts. Low-frequency bypassing that keeps source impedance low and stabilizes the converter's voltage loop and high-frequency bypassing that reduces switching related EMI. Low-frequency bypassing should be done according to the Design Guide. Array input impedance is the individual converter negative input impedance divided by the number of converters in the array. This can present a challenge for very large low-input-voltage arrays where impedances must be kept very low.

5 kW, 1,000 Amp Example Array

The following prototype was implemented with modules placed on evaluation boards and connected as shown in Figures 2 and 3. It uses 25 modules with part number V300B5C200B operating in parallel. The array has a 300 V input, 5 V 1000 A output, and is connected in a 5 x 5 array. Output leads must be very heavy gauge so as to have sufficient ampacity to safely carry the high output currents. To reduce the chance of noise causing the masters to swap control, R_5 is configured for 2% trim down. When using Micro family converters in parallel arrays it is imperative that the output voltage of each master is trimmed a minimum of 2% apart.

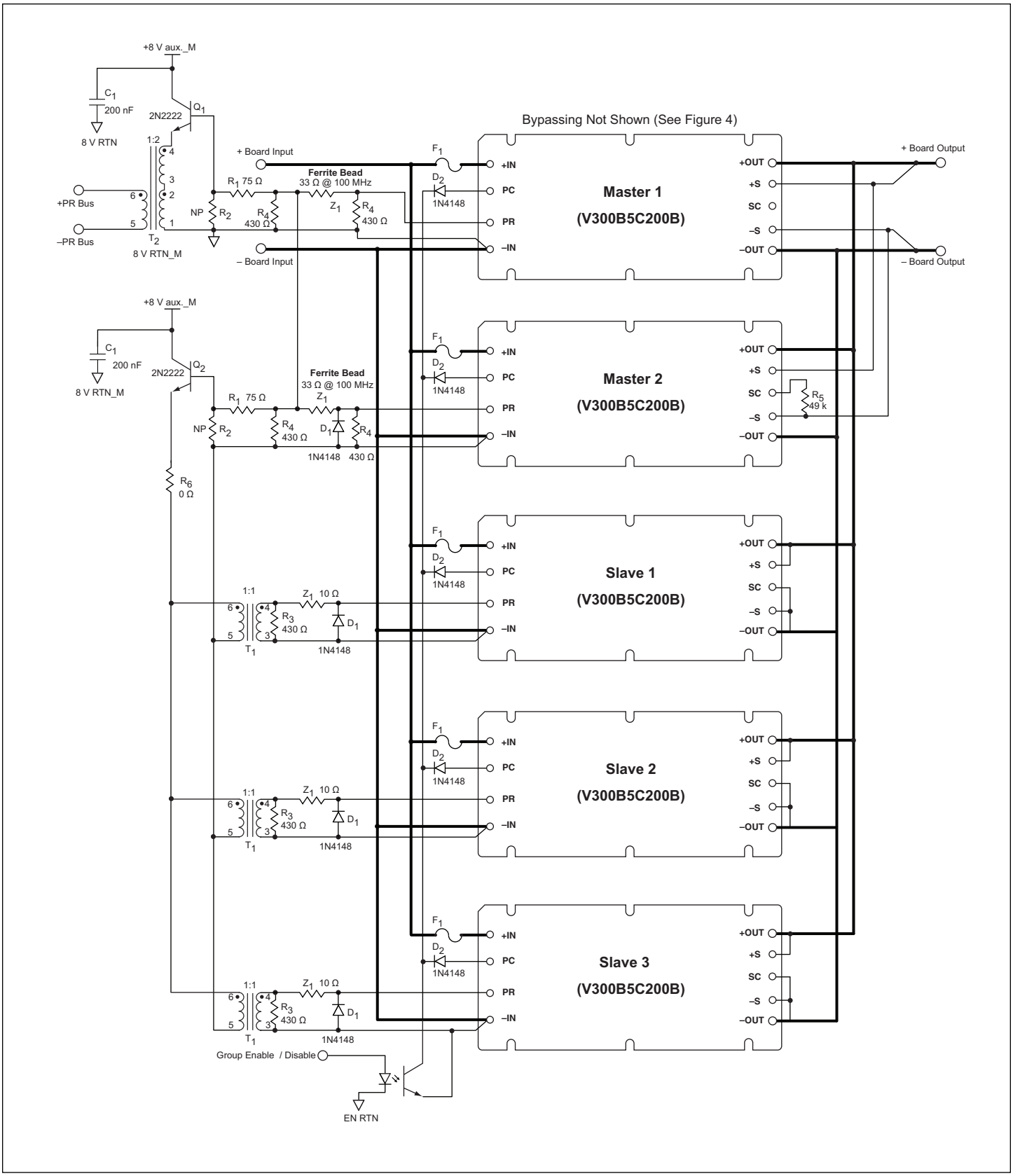

Figure 2 — Prototype array master board, one per system

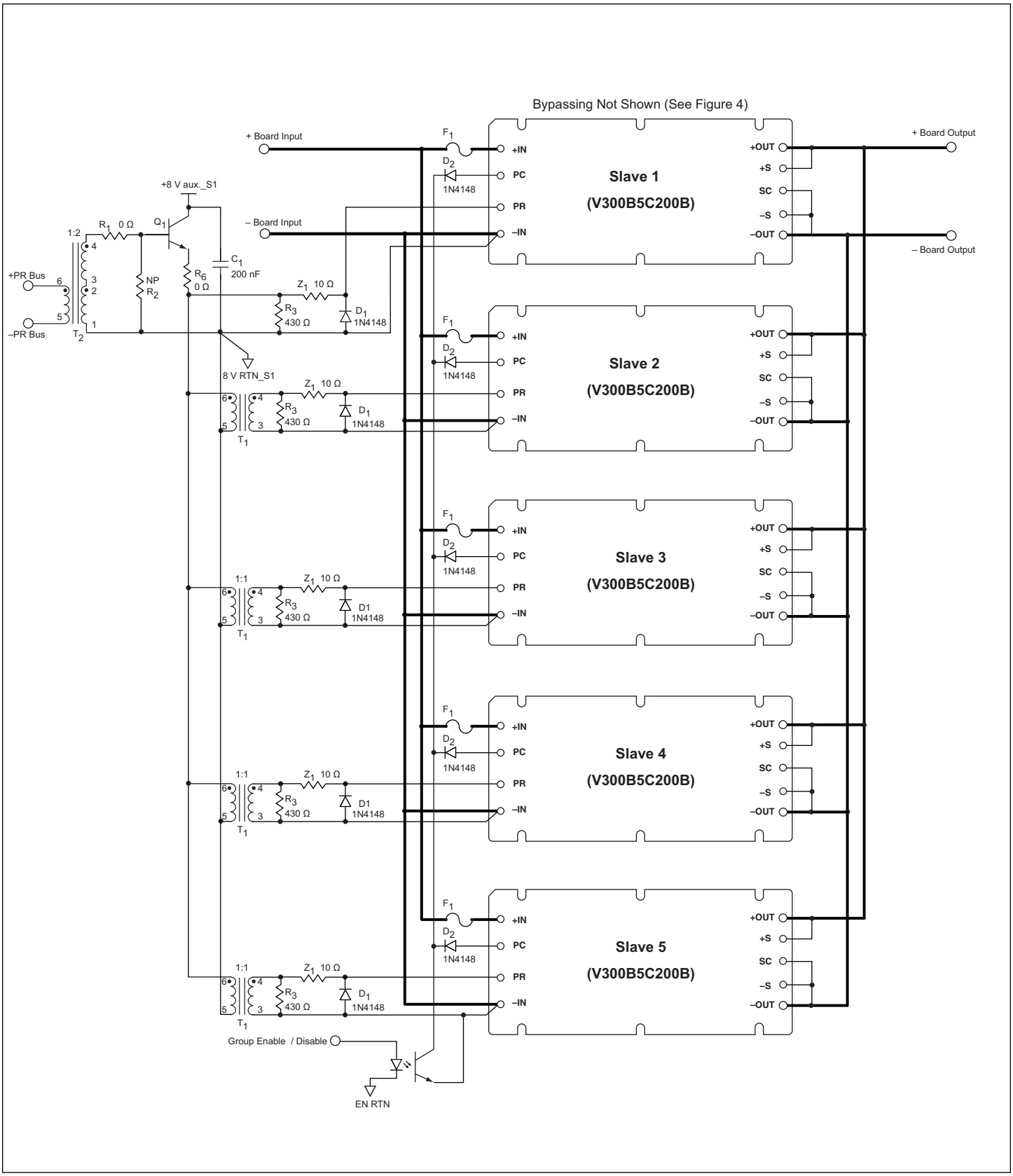

Figure 3 — Prototype array slave board, four per system

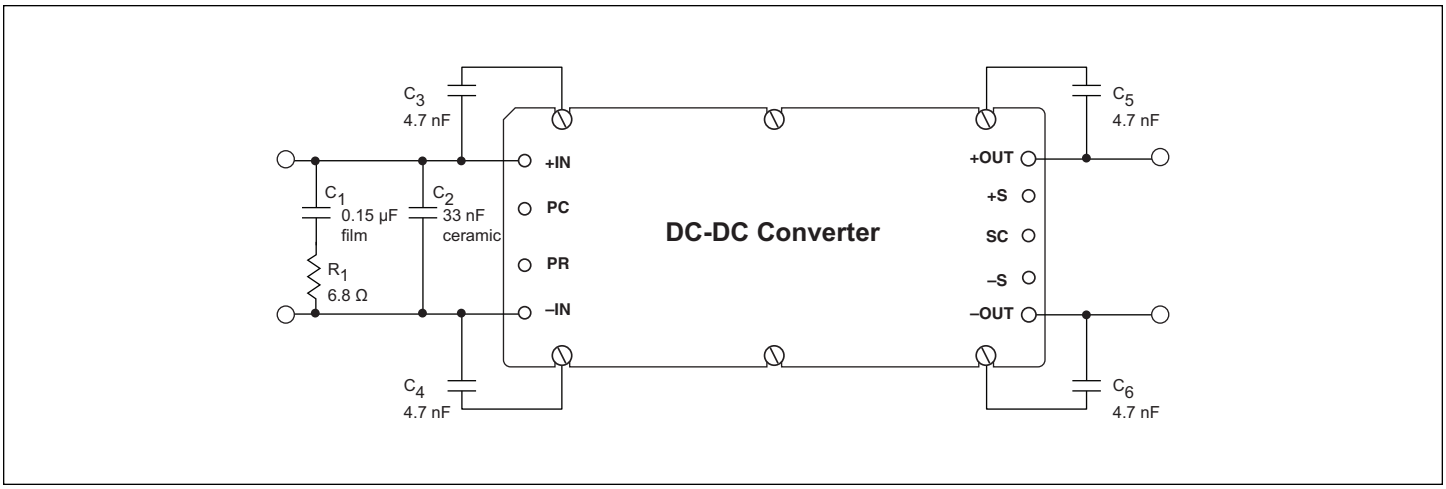

Figure 4 — Differential-mode and common-mode bypassing for 5 kW array, each module

The PC pins of the converters have been diode OR'd to provide group enable / disable for the array. An external control circuit such as a microprocessor can provide this signal. At a minimum, group undervoltage / overvoltage lockout is required, see the Vicor application note "Undervoltage / Overvoltage Lockout". Because of voltage drops between input leads of individual boards an optocoupler must be used to correctly drive the PC pins.

Differential and common-mode bypass capacitors were added close to each converter as shown in Figure 4. In addition, a 24 µF capacitor in series with 6.8 Ω damping resistor was added across the input of the entire array. See Page 7 for information on how these values were chosen.

Note: The high-power capability of the array's input source make proper safety precautions vital. Individual fusing is required for each converter as directed by the Design Guide and Applications Manual. If the array is supplied by an offline source an isolated scope should be used when making input side measurements. Never apply power to an array without connecting the output of the master board and all slave boards to the same point. Failure to do so will cause a destructive output overvoltage condition.

Initial System Testing

Even the best array design will not predict all parameters that will impact performance. Thorough testing during the prototyping phase is recommended so that optimal component values can be determined and potential issues avoided. Tests may include dynamic loading, checking input and output ripple, phase gain analysis, and PR bus signal fidelity. For safety and to simplify testing, initial power up should be performed on a subset of modules. For example, the master board of the above array was tested first and the system was subsequently checked as each new slave board was added.

PR Signal Fidelity

Optimal component values for damping the PR bus were found by testing the master board and one slave board (ten modules total). The PR bus should always be checked with an oscilloscope even if the array appears to behave properly.

Figure 5 shows the initial PR signal with series damping resistors / ferrite beads (Z_1), and shunt damping (R_3, R_4) removed. This displays undesirable ring up due to parasitic L and C. This pulse violates the 7 V absolute maximum rating on the PR pin. Insufficient damping may cause the pulse to make multiple transitions through the 2.5 V latching threshold. This can cause extra power pulses to be generated and should be avoided to prevent module damage.

Figures 6 and 7 show the PR waveform on the primary master and on the most distant slave module after the damping is added. Both are examples of well-damped PR pulses. The damping values shown are good starting values for other array configurations.

The peak amplitude of the PR pulse should be at least 4 V at every module for the pulse to be reliably detected, so more damping is not always better. The forward voltage drop associated with each emitter follower will add to PR signal attenuation.

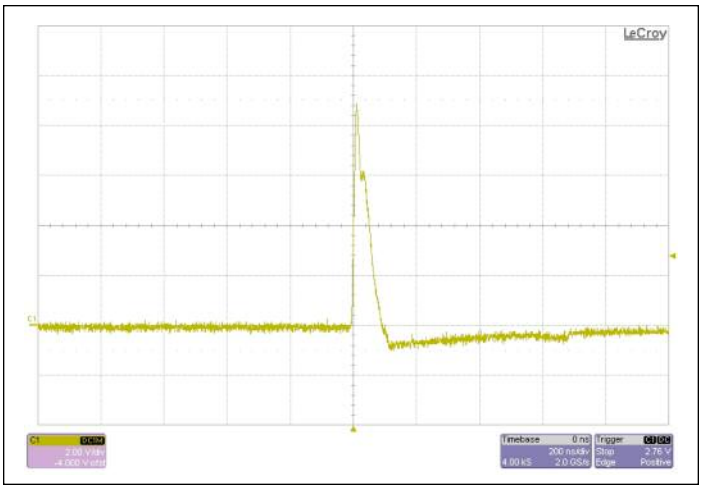

Figure 5 — PR pin with insufficient damping, farthest from master

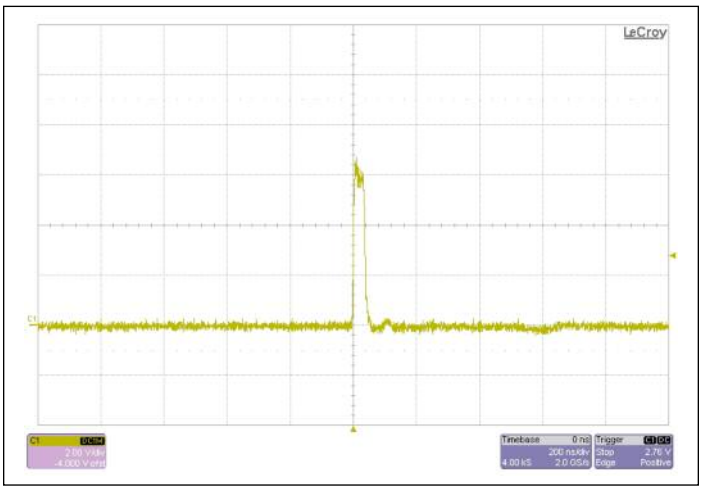

Figure 6 — PR pin, primary master

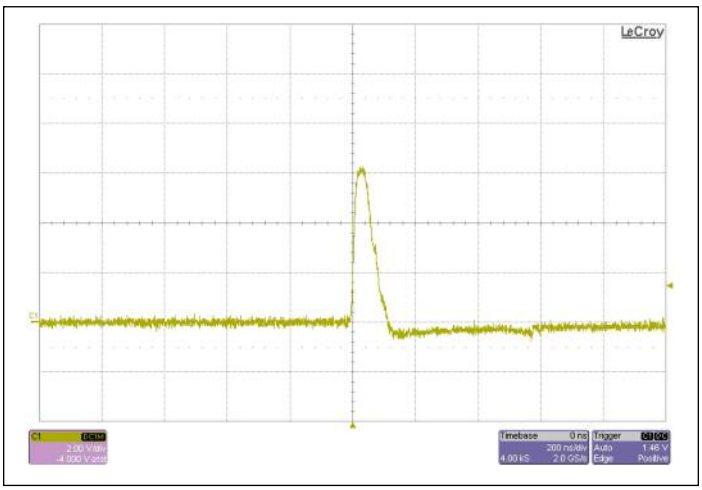

Figure 7 — PR pin, farthest from master

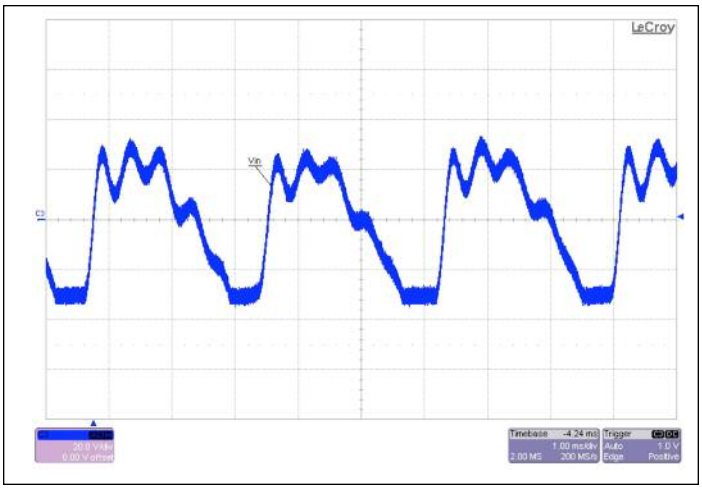

Figure 8 — 5 kW array input, full load

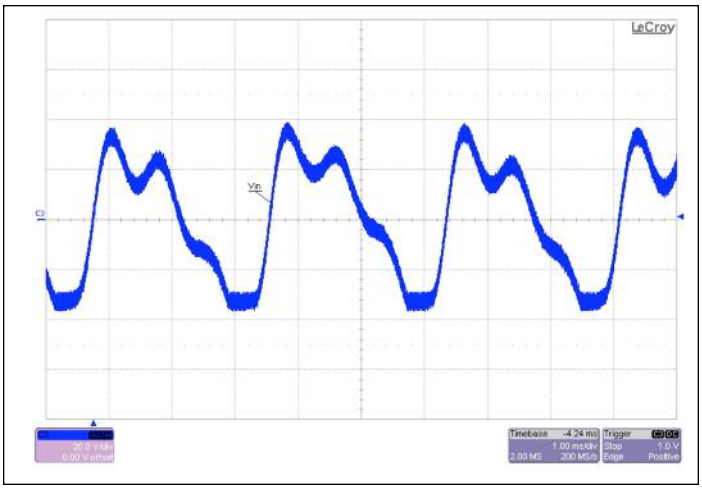

Figure 9 — 5 kW array input, full load, 24 µF bypass

Input Ripple

For the 25 module prototype, using a high input voltage meant little low frequency bypassing was required. Input impedance was low since the array was supplied with short leads from Vicor's 5 kW 3-Phase front end (Vicor P/N VI-TRY6-ICX). However, testing at full load uncovered a 2 kHz oscillation on the DC input bus due to distribution inductance, see Figure 8. This high-frequency ring is undesirable and will increase the output ripple of the DC-DC converters. The 360 Hz ripple is from the rectified 3-Phase 60 Hz AC line.

To dampen this parasitic resonance, the following steps were taken. First the nominal line input impedance for this array was calculated:

$$Z_{in} = \frac{(V_{NL})^2\ \eta}{P_{converter}\ x\ N} = \frac{(300\ V)^2\ x\ 0.82}{200\ W\ x\ 25} = 14.8\ \Omega$$

Where:

V_{NL} is the nominal input voltage of the array

$P_{converter}$ is the output power of each converter

η is the minimum efficiency of the V300B5C200B modules.

N is the number of modules in the array

Solving for a capacitor with roughly five to ten times lower impedance at 2 kHz gives about 24 µF.

Film or ceramic capacitors must be used due to the high peak-to-peak ripple voltage on the DC input bus. The lightly filtered bus has the advantage of keeping the power factor of the supply high and minimizing inrush current. Figure 9 shows the result of adding this capacitance across the input terminals of the array.

The original ringing is gone but the added capacitors have caused a lower frequency ring. This suggests series damping resistance to reduce the Q of the added capacitors. Adding about 10 Ω of damping in series with these capacitors results in the input waveform in Figure 10. This resistance was determined experimentally to give optimal damping for the capacitor value chosen.

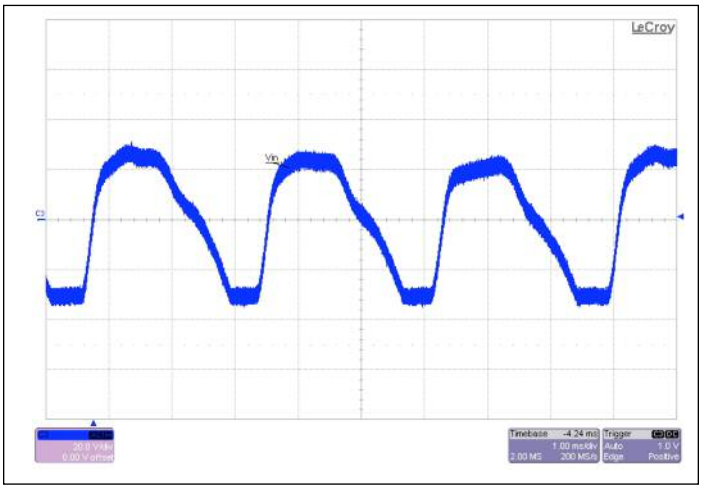

Figure 10 — 5 kW array input, full load, 24 uF bypass, 10 Ω damping

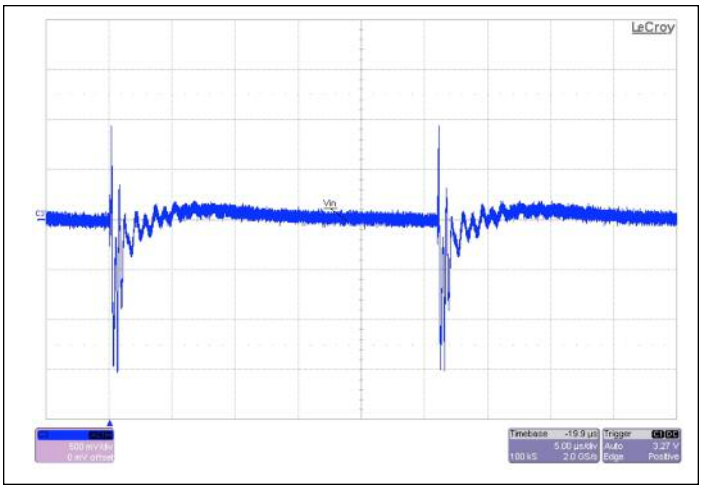

Figure 11 — Input switching noise with two modules no external differential bypass capacitors

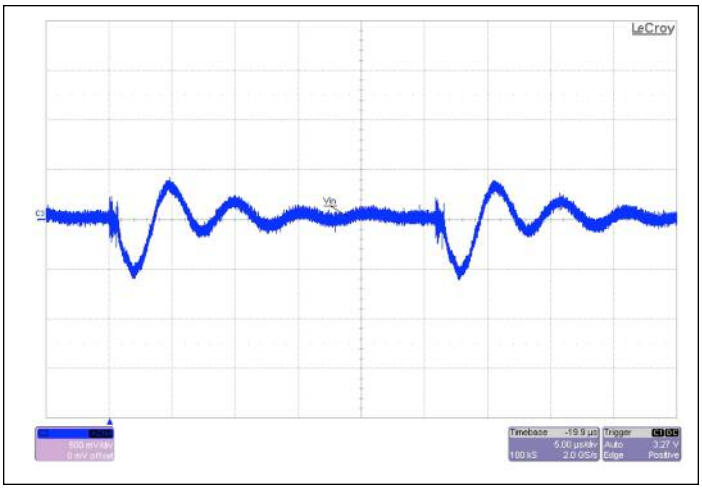

Figure 12 — Input switching noise with two modules with 0.15 µF film differential bypassing

EMI

High-frequency bypassing at the input of each module in the array can cut down on conducted noise before it can escape to the rest of the system, greatly reducing the demand for EMI filtering. Testing with several modules is the easiest method to arrive at optimal input bypassing. For example, Figure 11 shows the input waveform of two modules with no bypassing.

This waveform shows significant undesirable switching noise. To reduce it a 0.15 µF film capacitor was added at the input of each module, Figure 4. The resulting waveform is shown in Figure 12. Film capacitors were used because of their moderate Q relative to ceramics.

Much of the high-frequency noise has been eliminated but the ringing is undesirable. Series damping was added to attenuate this ringing. A starting value for the damping resistor can be found by calculating the characteristic impedance of the 200 kHz ring wave:

$$Z_{char} = \frac{1}{2\pi f C} = \frac{1}{2\pi(200\ \text{kHz})\ 0.15\ \mu\text{F}} = 5.3\ \Omega$$

Based on this result a 6.8 Ω damping resistor was added in series with the 0.15 uF capacitor. This involved a tradeoff because the resistor reduces attenuation of the highest frequency components of switching noise. To regain low impedance bypassing at high frequency a 33 nF ceramic capacitor was added directly across the input of each converter, see Figure 4. This was chosen because it represents roughly one-fifth the value of the larger capacitor and can thus be neglected at low frequency. The effect of the final bypassing network is shown in Figure 13.

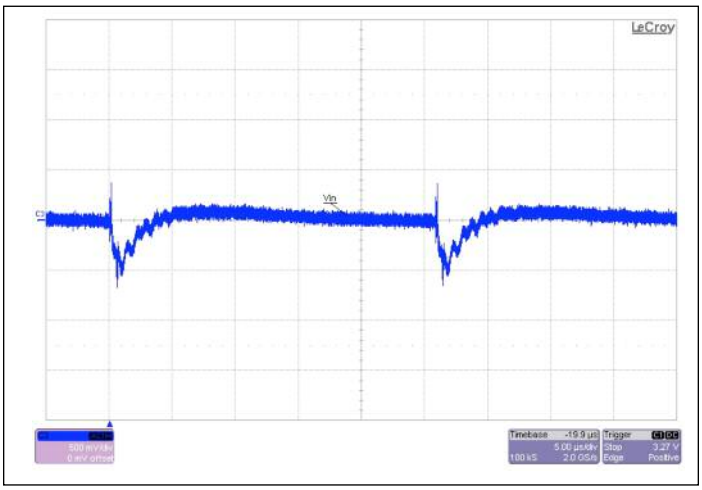

Figure 13 — Input switching noise with two modules with 0.15 µF film differential bypassing, 6.8 Ω series damping resistor, 33 nF ceramic differential bypassing

More information on high frequency bypassing can be found in the Design Requirements section of the Maxi, Mini and Micro Design Guide and Applications Manual.

Summary

The techniques demonstrated in this example allow high power arrays using Maxi, Mini and Micro converters to be implemented with a minimum of design effort. With nominal input voltages from 24 V to 375 V and outputs from 2 V to 52 V this family of converters offer exceptional versatility, reliability and ease of use. Vicor's experienced technical support can assist you in applying the benefits of these converters to your high power application.

For more information, please contact Vicor's Applications Engineers at 1-800-927-9474 or www.vicorpower.com/contact-us for worldwide assistance.