HV ChiP BCM® Reverse Start Up Circuit

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Summary

An economical, robust circuit for reverse starting Vicor HV (High Voltage) ChiP (Converter Housed-in-Package) BCM (Bus Converter Module) engines with analog mode control is described. The way the circuit works is explained.

Scope and Arrangement of Material

In the conventional mode, a DC source voltage is applied to the primary or high-voltage side of the BCM with its secondary port loaded. The BCM primary and secondary power ports are isolated. The BCM's controller is set on the primary side of the BCM. A BCM can be operated in another way, which is called reverse mode [ref 6]. In this configuration, source and load are swapped with each other: the source is set across the secondary port and load set across the primary port. To process power in this way, the BCM's controller has to "primed" first; once this is done, the primary port based load will receive power through the BCM with power sourced from the secondary port.

This app note presents a discrete component circuit for automatic start up of analog-controlled, HV ChiP formatted BCMs in reverse mode. The advent of routine BCM reverse start up opens up a wide field of applications. Examples of the use of a reverse or bidirectional BCM are seen in battery and super capacitor conditioning circuits, EV automotive power harvesting, and in HV DC tether voltage generation for UAV and AUVs [refs 4-6]. This note will pave the way to resolve issues associated with the start up of complex systems and the sequencing of power flow operations. (Dealing with arrays of BCMs is beyond the scope of this application note. Vicor Applications Engineering should be contacted about these unique applications.)

Much of the detail, associated with the BoM (bill of materials), waveform oscillograms of the operation of the primer and the like are provided in the appendix.

Introduction

BCM and VTM power components are members of the SAC (sine amplitude converter) family. The internal controller sub-systems of all SACs developed and manufactured to date are referenced to the primary side of their isolation barriers. In order to allow power flow through a SAC, irrespective of its direction, it is necessary to first activate the controller by feeding it a primary referenced supply voltage.

HV ChiP BCMs that have no primary HV (High Voltage) energy source available can be started or primed with the low-cost circuit described herein. The energy needed for start up is transferred from a secondary LV (Low-Voltage) DC source as a charge packet stream. This source is anticipated to be part of the mainstream application of the BCM: it is assumed to be permanently connected to the secondary side of the BCM. The trickle of current from the LV source is directed across the BCM's isolation barrier to a HUB (Hold-up Capacitor). Once charged, the HUB is connected for a short time to the primary power port of the BCM. After start up of the BCM and reverse mode confirmation, the primer circuit goes into a low power state.

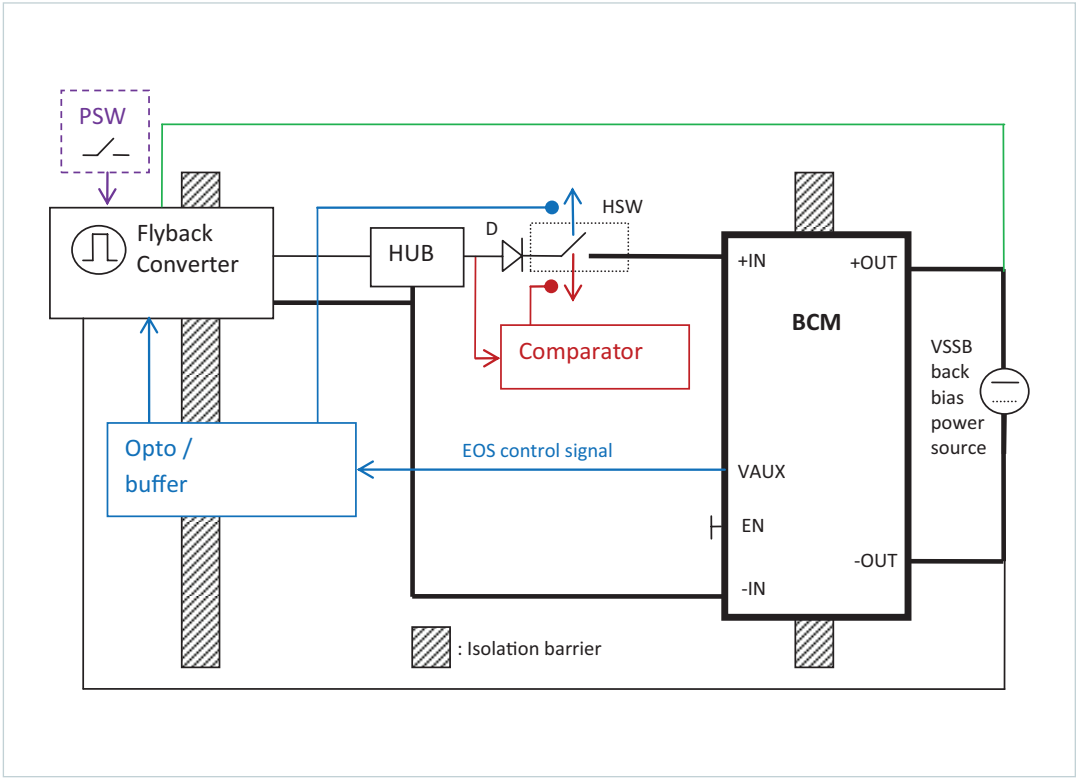
The primer system comprises a pulse generator, a low-power flyback converter, hold-up capacitor (HUB), unidirectional switch and command and control logic. The flyback power train has no linear feedback control loop installed. The power train is either ON or OFF, depending on the voltage of the hold-up capacitor and its relation to the BCM's input voltage turn-on threshold. A comparator and logic gating automatically sequences the circuit's various phases of operation.

Three variations can be made to the reverse BCM primer. The first adaptation makes it possible to accommodate some BCM applications that already have external filtering elements installed across the input port of the BCM. The second adaptation allows the circuit to work with either low- or high-voltage secondary DC power sources. A third adaptation is available for adjusting the primer circuit's turn-on threshold.

Overview of Reverse Primer Circuit Action

Figure 1 shows the reverse BCM® primer block diagram. The circuit elements in the BCM's secondary domain include a linear regulator, R-C pulse generator and flyback power train all included in the "Flyback Converter" block. This is followed by the HUB (Hold-up Capacitor) and switch HSW. The closure of this switch is not timed, but depends instead on the threshold set within the starter circuit for activating the BCM. In the specific case of HV BCMs, an opto-isolator drive is connected to the BCM's VAUX terminal. This signal will flag termination of the priming process, de-activating the pulse generator circuit drive and flyback power train.

Figure 1
System block diagram for BCM reverse starter



There are pre-defined voltage ranges for the VSBB (Voltage Source, providing secondary Back-Bias) that must not be exceeded. Rate of change of the VSBB source must also be controlled so that it does not introduce resonances or unexpected transients within the BCM.

With a correctly pre-configured VSBB source in place across the BCM's secondary port, the priming sequence occurs on closure of switch PSW. A linear auxiliary regulator that develops an internal $8V_{DC}$ rail is activated. This initiates pulse generation and the flyback converter starts switching. This power train delivers energy at high voltage for charging the HUB (Hold-up Capacitor) via a current-limiting resistor. Once the HUB voltage reaches a level that puts it well over V_{IN_UVLO+} for the BCM (input undervoltage lockout threshold – see BCM data sheet), a comparator closes the one-way switch HSW between the HUB and current-limiting resistor across the inactive BCM's primary circuit. This connection is held closed to start up the BCM.

Switch HSW opens if the reflected secondary supply voltage is greater than that delivered to the BCM by the HUB during the priming process. This condition would be consistent with a fully activated BCM being back-fed with the secondary source VSSB set at the high end of the BCM's secondary operational voltage range.

Shortly after start up has been initiated, the BCM indicates that is has been successfully primed by setting its VAUX terminal 'HIGH'. The starter is then latched OFF after reverse mode confirmation. The auxiliary DC regulator is disabled and the internal DC rail drops from 8V to approximately 1.2V: The pulse generator goes into an inactive state. This puts the low-side power switch in cut-off mode (see Figure 4 for circuit detail).

The reverse primer's automatic self-lockout from the BCM® power path avoids a situation where the start up circuit gets prematurely re-engaged. The BCM telegraphs secondary voltage fluctuations back to its primary port that are sometimes sufficient to disable its primary-referenced controller. To reset the primer, it is a simple matter to open the switch PSW and then re-close it after a short delay to reinitiate the priming sequence. The amount of time for the reset will be determined by the application circuit within which the BCM is embedded.

Primer Circuit Details

The BCM's primary-to-secondary isolation rating is preserved in the presence of the reverse starter circuit through the careful selection of an appropriate coupled inductor used in the flyback power train. This is rated at 3000 VRMS which is consistent with the isolation afforded by the HV ChiP BCM family of products. The flyback power train has power applied to its primary circuit via a linear regulator. It is important for the flyback primary supply voltage to be held close as possible to $8V_{DC}$ during primer engagement.

Given the range of secondary voltages for HV ChiP based BCM products (refer to Table 1), it is feasible to deploy a DC linear regulator which draws current from the VSBB source either with or without a power limiting resistor. Note also that the different BCM secondary voltage ranges "map" to one of two different voltage reference limiting resistor values associated with those ranges.

Table 1
HV ChiP BCM input / output voltage ranges supported by the reverse primer circuit

BCM Primary Voltage BCM V_{PRI} (V_{DC})	BCM Secondary Voltage BCM V_{SEC} (V_{DC})	Linear Regulator & VSSB V_{REF} option
260 → 410	32.5 → 51.3	UR
260 → 410	8.1 → 12.8	STD

This auxiliary linear regulator powers the circuits in the flyback converter block of Figure 1. The provision of this DC rail is subject to the customer's application. For instance, it is possible to deploy an auxiliary rail that is independent of the secondary back bias source VSSB, as the customer chooses. This regulator will only be active for a matter of a few seconds during priming. In its OFF state, it is expected that the power draw of the standard linear regulator applied in this note will be a few milliwatts.

The R-C clock oscillator internal to the flyback converter block generates a 50kHz square-wave for the low-side MOSFET power switch in the flyback converter. The oscillator is able to operate with DC bias set between 3.5V and $16V_{DC}$. With the 8V bias, the pulse train waveform's mark-time keeps the volt-second balance at an optimal level in the coupled inductor. The timing is also designed to ensure that the flyback converter operates in discontinuous conduction mode, allowing it to rapidly charge the Hold-up Capacitor. The time delay associated with the start up process will vary in accordance with the selected HUB capacitor's size [10µF – 100µF], its voltage coefficient, tolerance and temperature. The circuit uses a comparator for HUB switching, so it is not affected by these HUB variations. Thresholds in the comparator circuit are resistor-programmed, depending on the particular BCM in use.

To use Table 1, select a particular BCM and identify its input and output voltage ranges on its datasheet. Find the coincident condition in the table. This indicates whether the linear regulator will need to be adapted for either 'STD' or 'UR' - standard or upper range - VSSB source voltages.

The primer charges the HUB to a voltage consistent with the preset turn-on threshold. The comparator closes the HUB switch HSW and a pulse of charge, sufficient to turn on the BCM is transferred from the HUB.

The current delivered by the HUB is consistent with the highest no-load power draw of a BCM running in forward mode. Taking one example, a BCM rated to dissipate no more than 27W of no-load power, with activation level set to $330V_{DC}$, this current is determined to be slightly less than 82mA for a part such as the BCM6123TD1E13A3T0R. The current limit at $330V_{DC}$ is consistent with the maximum continuous current handling capability of the high voltage PMOS FET Q1 located in the HUB / HSW assembly (see Figure 5).

After the BCM's internal controller has been activated, it executes a series of house-keeping checks. Once the controller completes its checklist program, it signals that the BCM® is ready to process power by sending two pulses to the VAUX pin, as shown in Figure 2. The Opto-isolator/buffer block reacts only to the second positive-going step transition of the VAUX signal, which follows the initial short pulse some 20 to 30 milliseconds later. The buffered EOS (End of start up) signal (shown in Figure 1) disengages the auxiliary regulator. The auxiliary regulator's output voltage drops from 8V to 1.25V_{DC}. The output voltage of the flyback converter collapses to zero. A blocking diode, D, situated in the output lead of the converter, blocks backward current that would otherwise return to the HUB.

The choice of the HUB is contingent on the nature of input filtering network set between the load (or source) of the BCM on its primary port to be "hot-plugged" through the network. It is also a strong determinant in SAC applications for attaining successful start up (please consult Vicor Applications Engineering if other SACs need to be primed). In relation to external pre-installed EMI filtering, it has been found that a 100µF HUB may allow adequate charge delivery to the BCM – in spite of the sneak paths that parallel it. In the standard applications filter circuit that precedes the primary port of the BCM, bulk capacitance is not applied across the BCM's primary port, so a 10µF HUB is adequate. If the loading is heavy, then it will be necessary to "hot swap" the filter network and the downstream source/load combination in the primary circuit, once the BCM is fully operational. This is outlined in Figure 3.

The BoM is broken down in accordance with the different functions that were initially identified in the outline block diagram of Figure 1. The BoM for the reverse starter circuit is included in the Appendix.

Figure 2

Input Voltage-Enabled BCM simulation showing ramped input voltage in the top trace, EN (blue trace) and VAUX (purple trace) signals in the lower part of the figure. This is the mode for BCM turn-on that the reverse starter invokes

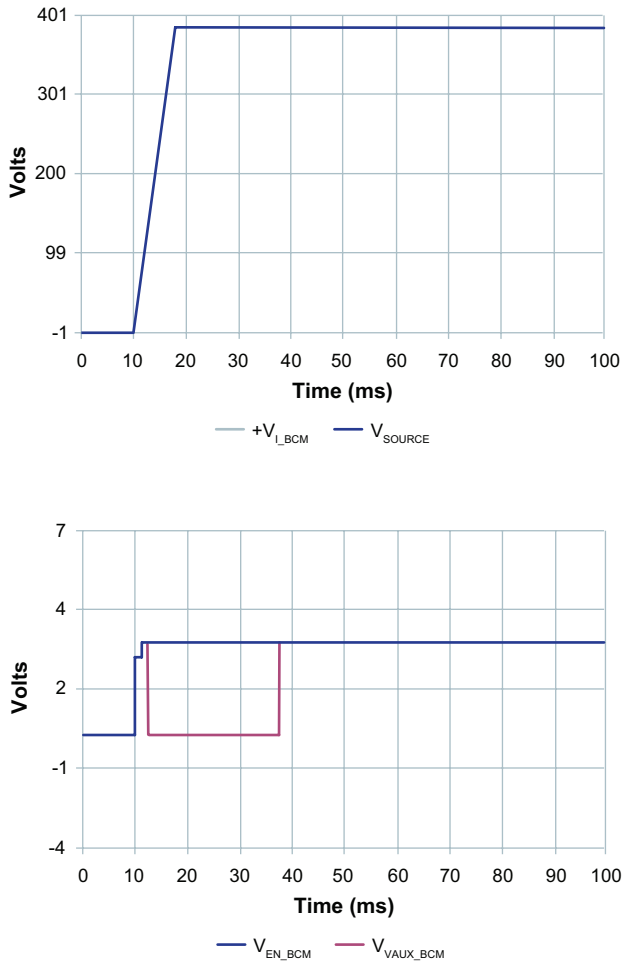


Figure 3

Showing the reference plane across which the HUB is to be switched into the BCM for start up. The primary side load and possibly the external filter / bulk capacitor may need to be temporarily disengaged until the BCM is fully operational, following completion of reverse start up

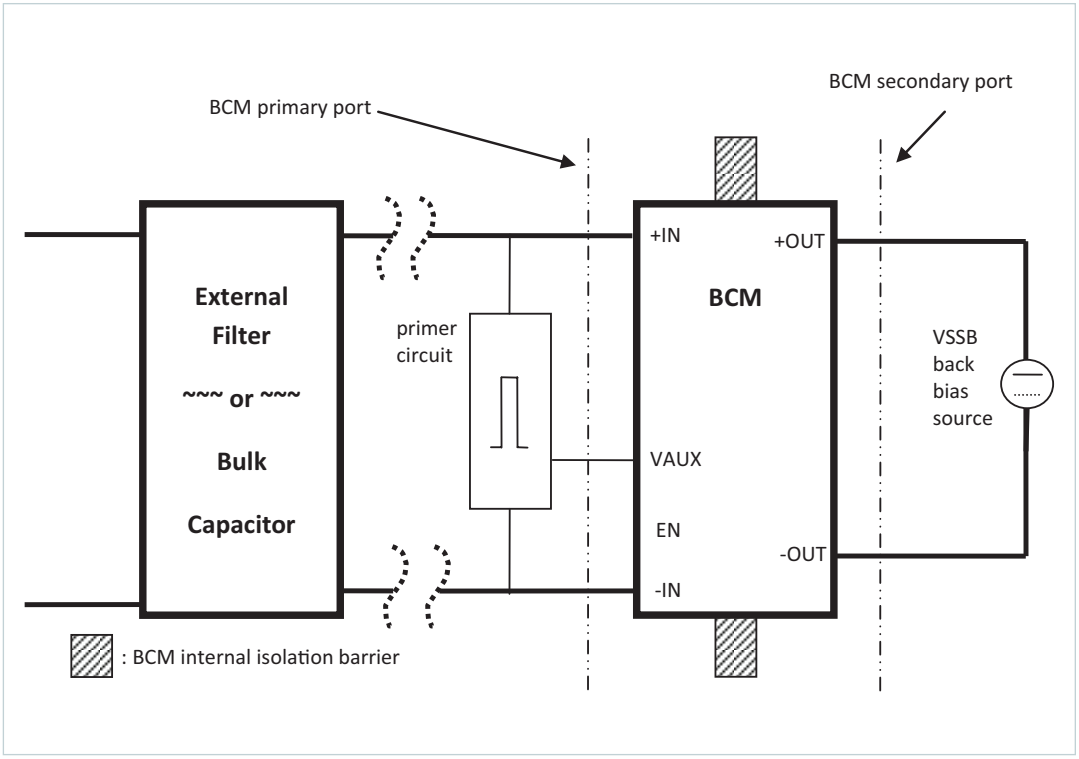
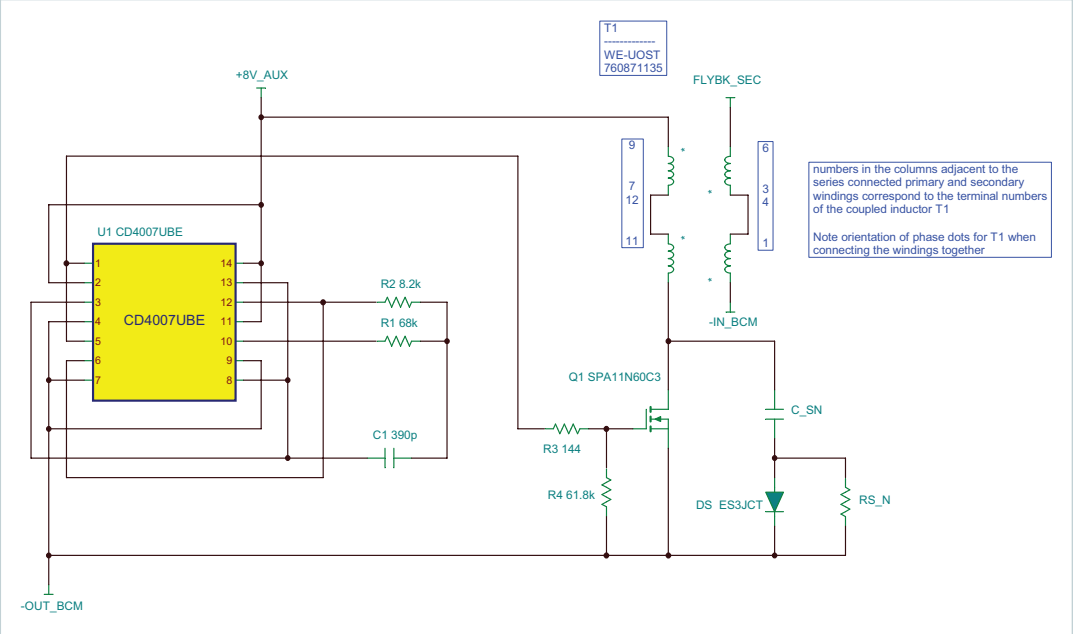


Figure 4
50kHz pulse generator and flyback converter power train schematic



The flyback converter block comprises a pulse generator and the flyback power train. The pulse generator (shown on the left hand side of Figure 4) is based on an R-C oscillator that utilizes unbuffered inverters and MOS switches contained in the CD4007UBE [ref 2]. The flyback power train comprises a drive termination network, the main power switch, R-C-D snubber and 3000V_{RMS} rated coupled inductor. Note that the snubber R-C component selections are impacted by parasitic inductance associated with the switching node of the primary side circuit. To proceed with some tentative values, setting RS_N to 680Ω and CS_N to 390pF will provide the basis of compensating the flyback power train switching node. When laying out a PCB, minimizing the pad size of the power switching MOSFET's drain node will reduce parasitics. Although values are stated, it is advisable to make measurements with the initial components selected and adjust the snubber network values until there are no significant switching oscillations present on this critical node.

HUB (Hold-Up Capacitor) and HSW (HUB Switch)

The HUB (Hold-Up Capacitor) and the HSW (HUB Switch) schematic sections are shown in Figure 5. An electrolytic capacitor is set to one of two values, depending on the BCM primary capacitance that needs to be 'swamped' by the HUB. Tracing from the FLYBK_SEC (Flyback Secondary Winding Node) terminal on the left hand side of the schematic to the right, there is high-voltage blocking diode D and a series current-limiting resistor. This assures a current-limited start up of the flyback power train. If the external input filter or bulk capacitor electrolytic or ceramic capacitors present very low impedance in relation to the HUB, these will need to be temporarily disconnected in order to permit reliable reverse start up of the BCM.

To be clear, the starter circuit is not designed to bring up both the BCM® and power elements connected ahead of its primary port. It is only capable of applying sufficient current at the correct voltage to the BCMs HV input power port alone, as shown in Figure 3. Customers with applications involving large amounts of capacitance placed at the BCM input port should consult Vicor Applications Engineering. The impedance of the inactive BCM reverse starter is very small to the extent that it should not affect the response of input filtering, particularly to CE (conducted emissions), once disabled after deployment. It has been found that in optimal CE suppression applications, that no bulk differential capacitor should be connected across the BCM input power port. Absence of external applied input capacitance prevents common mode noise imbalance in such networks.

Moving to the right of the HUB, a PMOS high side switch assembly is controlled by a comparator. The comparator senses the voltage build-up across the HUB as it charges. The comparator activates the HSW once its turn-on threshold is reached.

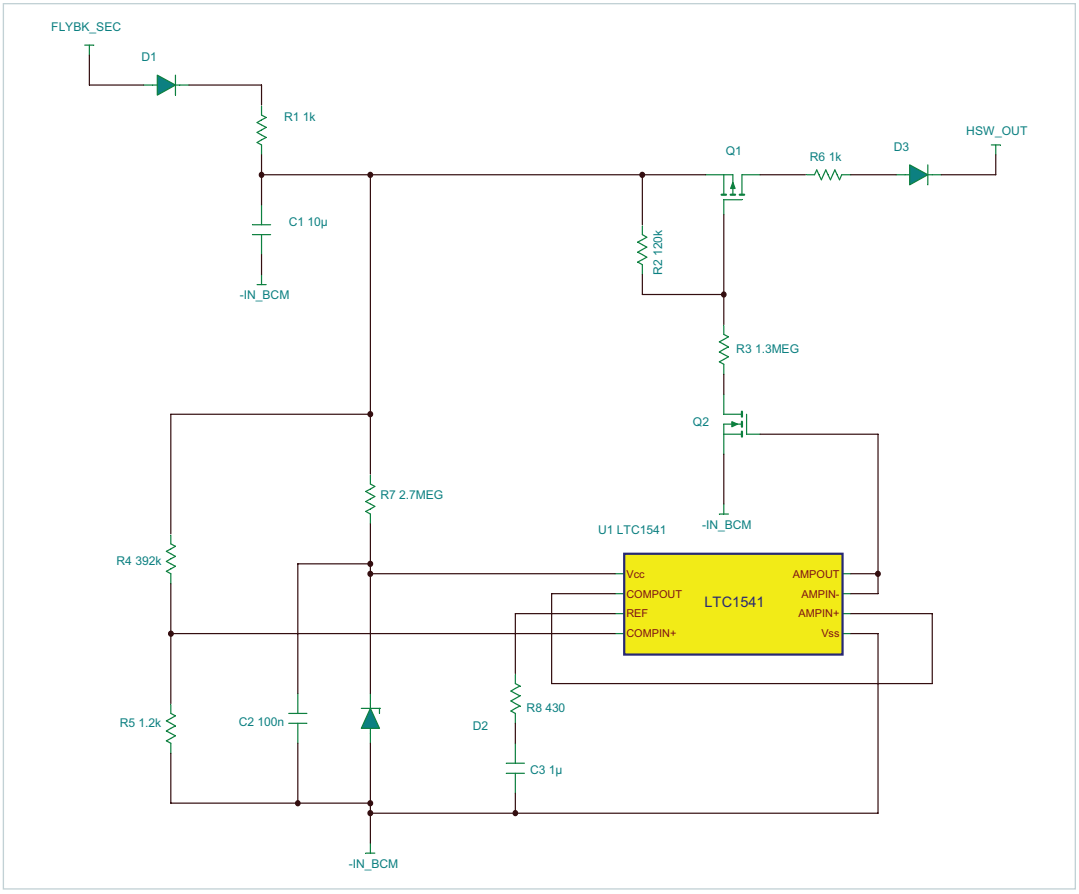
The threshold is easily calculated with the following equation

Equation 1

$$V_{threshold} = \left(\frac{R4 + R5}{R5}\right) \bullet V_{ref}$$

In the example schematic of Figure 5, $V_{threshold}$ is 328V, set with R4 = 392kΩ and R5 = 1.2kΩ. In the LTC1541 comparator, the reference voltage is $1.2V_{DC}$.

Figure 5
HUB and HSW assembly for UR option (see Table 1)

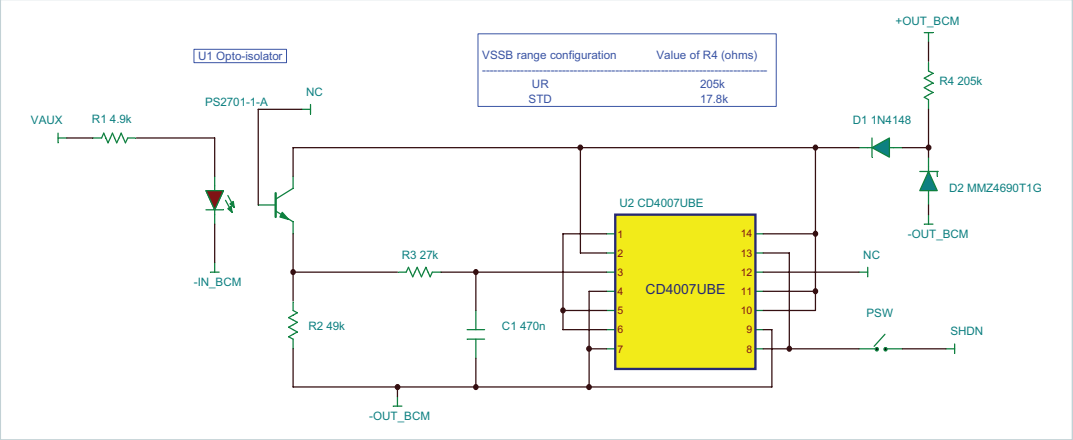


Command and Control Circuit

The Command and Control circuit includes the EOS (End of start up) control signaling and the opto-isolator elements as shown in the block diagram of Figure 1. The circuitry is shown in Figure 6.

The start up process starts with the closure of a manual SPST switch PSW. On closure of PSW, the start up regulator is enabled via the pulling down of the SHDN signal line. The BCM® presents a 3V positive logic signal pulse and step, each of these gets transmitted through the opto-isolator and filtered with the R3-C1 network, leaving only the positive step signal. The processed step signal, buffered by the CD4007UBE, turns off the DC start up regulator stage. PSW can be replaced with a simple transistor.

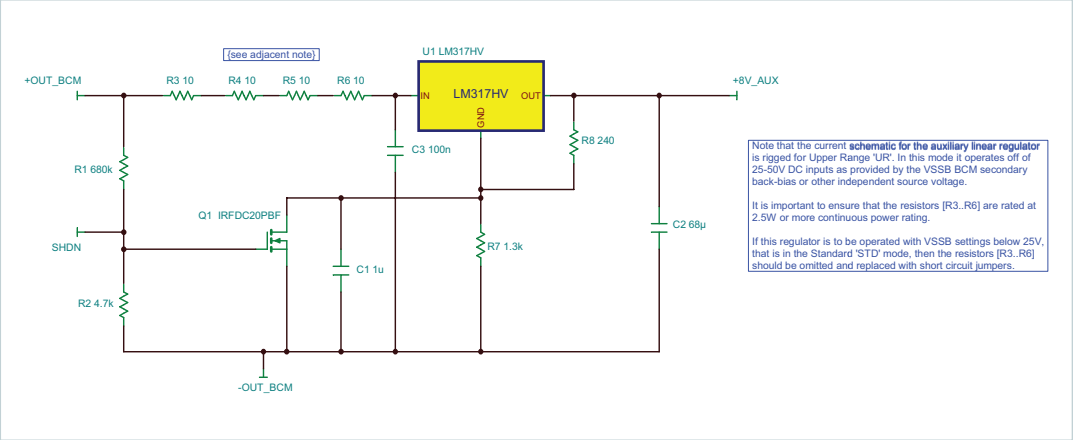
Figure 6
Command and Control Logic assembly for UR option (see Table 1)



Auxiliary DC Regulator

A DC regulated low-voltage source has been contrived. It preserves the use of the same flyback power train with bias voltages of between 10.5V and 55V. Refer to Figure 7 for the schematic. This produces $8V_{DC}$ at a maximum current of 500mA. The SHDN terminal is driven by the command and control circuit to turn off the auxiliary regulator after reverse priming has been accomplished. The LM317HV is thermally limited. With bias voltages in excess of $25V_{DC}$ applied to it, it is necessary to insert power resistors ahead of the regulator's $+V_{IN}$ terminal. These four power limiting resistors should not be incorporated into the start up regulator if the applied voltage from the secondary bias source is less than $25V_{DC}$.

Figure 7
Auxiliary DC regulator



Summary

A reverse primer circuit, initially proposed for HV ChiP BCM®s with Analog Control, has been presented. It is adaptable to the needs of starting up other SACs in the Vicor portfolio, such as VIC VTM™s, with slight modifications. Other Configurations may be available for this. Please contact Vicor Applications Engineering for further details.

Disclaimer

It should be noted that only reversible BCMs and VTMs have been formally qualified by Vicor for applications involving continuous reverse or bi-directional duties. Please note that Vicor outlines its Warranty Policy on each of its products' datasheets.

References

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5. "Bidirectional DC/DC conversion enables efficient back-up power configurations" G. Profit EDN Europe Apr. 29, 2014
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Appendix

Tables

Table A1
ChiP HV BCM Part Numbers in the product portfolio, current as of January 2017

Part Number	Vin (V)	Vout (V)	Current (A)	Package	Control Interface
BCM6123xD1E5116yzz »	260 – 410	32.5 – 51.3	16.9	6123 ChiP	Analog or Digital
BCM6123xD1E5126yzz »	260 – 410	32.5 – 51.3	25.7	6123 ChiP	Analog or Digital
BCM6123xD1E5135yzz »	260 – 410	32.5 – 51.3	35.0	6123 ChiP	Analog or Digital
BCM6123xD1E1368yzz »	260 – 410	8.1 – 12.8	68.0	6123 ChiP	Analog or Digital
BCM6123xD1E13A2yzz »	260 – 410	8.1 – 12.8	125.0	6123 ChiP	Analog or Digital

Oscillograms

Figure A1
Flyback power train, 1.5ms after PSW engagement. Primary and secondary inductor currents are shown along with input and output voltage waveforms.

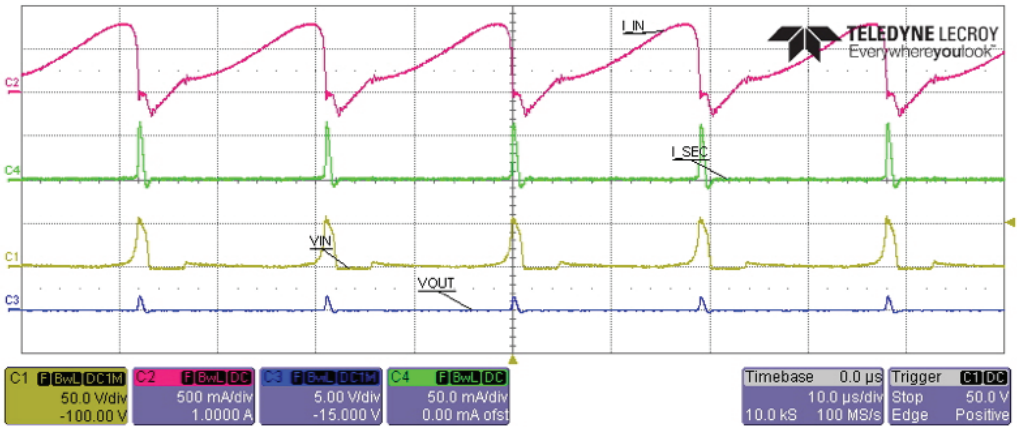
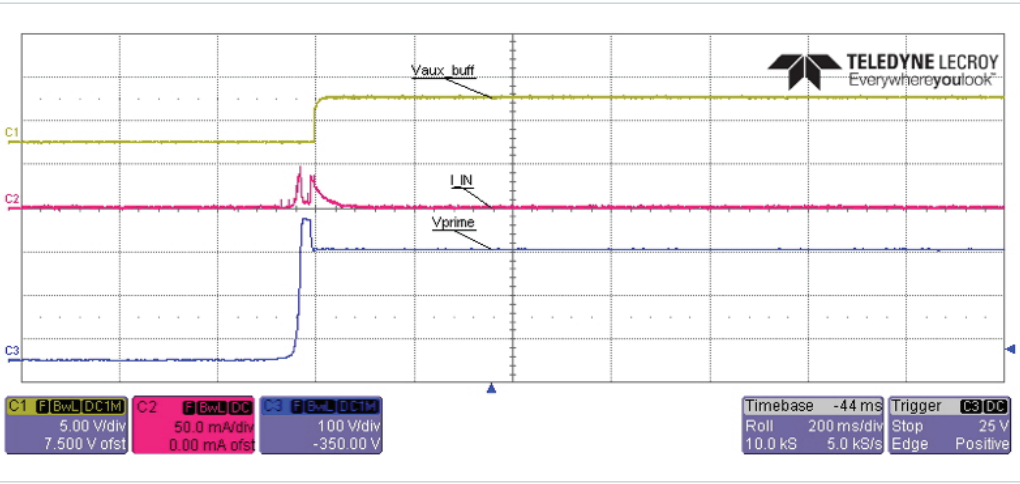


Figure A2
start up signaled with buffered VAUX EOS signal for BCM6123TD1E13A3T0R biased with minimal VSBB potential.



Note: There are two current pulses in the red trace. The first one is associated with current delivery to the BCM® from the HUB to start the BCM up. The BCM input voltage peaks at it gets 330V set across its input power port. The BCM input comes up to this imposed level, and then settles. Prior to this test, the VSBB voltage was adjusted to lowest setting, which is 8.1V_{DC}. The BCM reflects 260V onto the primary port, this voltage being at a level that permits another small pulse of current to be delivered by HUB which is still receiving charge from the flyback. At the instant that VAUX transitions for the second and final time, charge transfer from the primer to the BCM is terminated.

Partitioned BoM for BCM Reverse Primer Circuit

Flyback Converter Block (Pulse Generator + Flyback Power Train)

Pulse Generator

Designator	Description	Manufacturer	Manufacturer Part Number
U1	IC CMOS DUAL COMP PR W INV 14-PIN	TEXAS INSTRUMENTS	CD4007UBE
C1	CAP X7R 390pF 1% 50V		
R1	RES 68.0kΩ 1%		
R2	RES 8.2kΩ 1%		

Flyback Power Train

Designator	Description	Manufacturer	Manufacturer Part Number
Q1	MOSFET N-CH 600V 11A TO220-3	INFINEON	SPA11N60C3XKSA1
T1	UNIV OFFLINE XFMR 1.25mH, 4kV	WURTH ELECTRONIK	760871135
R3	RES 144Ω 1%		
R4	RES 61.8kΩ 1%		
RS_N	RES 390Ω 1%	Change as needed	
CS_N	CAP X7R 390pF 10% 50V	Change as needed	
DS	DIODE GEN PURP 600V 3A SMC	ON SEMI	ES3J

HUB (Hold-Up Capacitor) and HSW (HUB Switch)

Designator	Description	Manufacturer	Manufacturer Part Number
U1	IC µPWR OPAMP, COMP, REF 8-PIN SO	LINEAR TECH CORP	LTC1541IS8#PBF
Q1	MOSFET P-CH 500V 0.1A TO92-3	MICROCHIP	VP2450N3-G
Q2	MOSFET N-CH 600V 320mA 4-PIN DIP	VISHAY SILICONIX	IRFDC20PBF
D1, D3	DIODE GEN PURP 600V 3A SMC	ON SEMI	ES3J
D2	DIODE ZENER 5.6V 5% 50µA	ON SEMI	MMSZ4690T1G
C1	CAP ALEL 10µF 10% 450V		
C2	CAP X7R 100nF 10% 50V		
C3	CAP FILM 1µF 10% 16V		
R1, R6	RES 1.0kΩ 1% 0.25W		
R2	RESISTOR 120.0kΩ 1%		
R3	RESISTOR 1.3MΩ 10%		
R4	RESISTOR 392.0kΩ 1%		
R5	RESISTOR 1.2kΩ 1%		
R7	RESISTOR 2.7MΩ 10%		
R8	RESISTOR 430Ω 1%		

Command and Control Circuit

Designator	Description	Manufacturer	Manufacturer Part Number
U1	OPTO-ISOLATOR 3.75kV TRANS 4-SMD	CEL	PS2701-1-A
U2	IC CMOS DUAL COMP PR W INV 14-PIN	TEXAS INSTRUMENTS	CD4007UBE
D1	DIODE GEN PURP 100V 200mA DO35	ON SEMI	1N4148TA
D2	DIODE ZENER 5.6V 5% 50µA	ON SEMI	MMSZ4690T1G
C4	CAP X7R 470nF 16V		
R1	RES 4.9kΩ 1%		
R2	RES 49kΩ 1%		
R3	RES 27kΩ 1%		
R4	RES 205kΩ 1%	Use for 'UR' config	
	RES 17.8kΩ 1%	Use for 'STD' config	
SW1	SPST SWITCH		

Auxiliary Linear Regulator

Designator	Description	Manufacturer	Manufacturer Part Number
U1	IC REG LDO ADJ 1.5A TO220-3	TEXAS INSTRUMENTS	LM317HVT/NOPB
Q1	MOSFET N-CH 600V 320mA 4-DIP	VISHAY SILICONIX	IRFDC20PBF
C1	CAP FILM 1.0µF 16V		
C2	CAP ALEL 68µF 63V		
C3	CAP X7R 0.1µF 100V		
R1	RES 680kΩ 1%		
R2	RES 4.7kΩ 1%		
R7	RES 1.3kΩ 1%		
R8	RES 240Ω 1%		
R3, R4, R5, R6	RES 10Ω 2.5W 10%	Use for 'UR' config	
	RES ZERO Ω JUMPER	Use for 'STD' config	