PI2061

Cool-Switch® Series

High Side High Voltage Load Disconnect Switch Controller IC

Description

The PI2061 is a high-speed electronic circuit breaker controller IC designed for use with N-channel MOSFETs in high side load disconnect switch solutions for medium voltage applications. The PI2061 Cool-Switch® controller enables an extremely low power loss solution with fast dynamic response to an over current fault or EN Low conditions.

Once enabled, the PI2061 monitors the MOSFET current through a sense resistor. If an over current level is sensed, the switch is quickly latched off to prevent the power source from being overloaded. Bringing the EN pin low will reset the over current latch allowing retry. To avoid false tripping by the in-rush current, the over current level is approximately doubled during startup, until SN approaches about 0.8V below VC. The PI2061 has an internal charge pump to drive the gate of a high side N-Channel MOSFET above the VC input. There is an internal shunt regulator that regulates the VC input with respect to the SGND pin for applications higher than 11 volts.

Features

- Programmable latching over-current detection
- Fast 120ns disconnect response to a load short
- Fast disable via EN pin, typically 200ns.
- 4A gate discharge current
- Internal charge pump
- Fault status indication

Applications

- Telecom System, ≤80V operation & 100V/100ms Transient
- N+1 Redundant Power Systems
- Servers & High End Computing
- High Side Circuit Breaker and Load Disconnect

Package Information

The PI2061 is offered in the following package:

- 10 Lead 3mm x 3mm DFN package

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Typical Application:

![PI2061 Block Diagram](image)

Figure 1: PI2061 in High Side Disconnect switch application

![PI2061 Response Time](image)

Figure 2: PI2061 response time to output short fault condition

Not Recommended for New Designs
## Pin Description

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PGND</td>
<td>1</td>
<td><strong>Gate Driver Switch Return</strong>: This pin is the high current return path for the gate driver turn off switch. Connect this pin to the low side of VC bypass capacitor and SGND.</td>
</tr>
<tr>
<td>GATE</td>
<td>2</td>
<td><strong>Gate Drive Output</strong>: This pin drives the gate of the external N-channel MOSFET. Under normal operating conditions, the GATE pin pulls high to approximately 2*VC with respect to SGND pin. The controller turns the GATE off during an over-current fault that is above the overcurrent voltage threshold (166mV during power up and 70mV in steady state).</td>
</tr>
<tr>
<td>VC</td>
<td>3</td>
<td><strong>Controller Input Supply</strong>: This pin is the supply pin for the control circuitry and gate driver. Connect a 0.1μF capacitor between the VC pin and the SGND pin. Voltage on this pin is regulated to 11.7V with respect to SGND by an internal shunt regulator. Connect a bias resistor (R_{VC}) between the VC pin and the supply input as shown in Figure 1.</td>
</tr>
<tr>
<td>SGND</td>
<td>4</td>
<td><strong>VC Return</strong>: This pin is the return (ground) for the control circuitry. Connect this pin to the low side of the VC bypass capacitor and high side of the R_{PG} resistor as shown in Figure 1.</td>
</tr>
<tr>
<td>EN</td>
<td>5</td>
<td><strong>Enable</strong>: Pull this pin low with 8μA or more to disable the gate driver and reset the latch. Tie this pin to VC if the Enable/disable feature is not used.</td>
</tr>
<tr>
<td>SP</td>
<td>6</td>
<td><strong>Positive Sense Input &amp; Clamp</strong>: Connect SP pin to the positive side of the sense resistor. The magnitude of the voltage difference between SP and SN provides an indication of the current through the sense resistor.</td>
</tr>
<tr>
<td>SN</td>
<td>7</td>
<td><strong>Negative Sense Input &amp; Clamp</strong>: Connect SN pin to the negative side of the sense resistor. The magnitude of the voltage difference between SP and SN provides an indication of the load current through the sense resistor.</td>
</tr>
<tr>
<td>NC</td>
<td>8, 10</td>
<td><strong>No Connect</strong>: Leave pins unconnected</td>
</tr>
<tr>
<td>FT</td>
<td>9</td>
<td><strong>Fault Status Output</strong>: This open collector pin transitions to high resistance to indicate a fault. When the controller input voltage is in under voltage, VC - SGND &lt; 7V this pin is high resistance as well. When the part is in a normal operating condition and gate driver is enabled this pin is low resistance.</td>
</tr>
</tbody>
</table>

### Package Pin-Outs

![Package Pin-Outs Diagram](image-url)

10 Lead DFN (3mm x 3mm)
Top view
# Absolute Maximum Ratings

*Note: All voltage nodes are referenced to SGND*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VC Supply</td>
<td></td>
<td>-0.3V</td>
<td>0.3V</td>
<td>17.3V</td>
<td>V</td>
<td>No VC limiting Resistor</td>
</tr>
<tr>
<td>SP, SN, FT, EN</td>
<td></td>
<td>-0.3V</td>
<td>0.3V</td>
<td>17.3V</td>
<td>V</td>
<td>VC = 10.5V, SP=SN=VC</td>
</tr>
<tr>
<td>GATE</td>
<td></td>
<td>-0.3V</td>
<td>0.3V</td>
<td>24V</td>
<td>A</td>
<td>VC = 8.5V, SP=SN=SGND</td>
</tr>
<tr>
<td>PGND</td>
<td></td>
<td>-0.3V</td>
<td>0.3V</td>
<td>3V</td>
<td>A</td>
<td>Value is always held at VG max</td>
</tr>
<tr>
<td>SGND</td>
<td></td>
<td></td>
<td></td>
<td>40mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td></td>
<td></td>
<td></td>
<td>-65°C</td>
<td>150°C</td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td></td>
<td></td>
<td></td>
<td>-40°C</td>
<td>140°C</td>
<td></td>
</tr>
<tr>
<td>Soldering Temperature for 20 seconds</td>
<td></td>
<td></td>
<td></td>
<td>260°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Rating</td>
<td></td>
<td></td>
<td></td>
<td>2kV</td>
<td>HBM</td>
<td></td>
</tr>
</tbody>
</table>

## Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC=EN=10.5V, C_{VC}=0.1µF, C_{GATE,PGND}=1nF, SGND=PGND

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VC Supply</td>
<td></td>
<td>8.5</td>
<td>10.5</td>
<td></td>
<td>V</td>
<td>No VC limiting Resistor</td>
</tr>
<tr>
<td>Operating Supply Range</td>
<td>V_{VC,SGND}</td>
<td>8.5</td>
<td>10.5</td>
<td></td>
<td>V</td>
<td>VC = 10.5V, SP=SN=VC</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>I_{VC}</td>
<td>1.7</td>
<td>2.1</td>
<td></td>
<td>mA</td>
<td>VC = 8.5V, SP=SN=SGND</td>
</tr>
<tr>
<td>Quiescent Current Start Up</td>
<td>I_{VCSU}</td>
<td>2.0</td>
<td>2.5</td>
<td>3.0</td>
<td>mA</td>
<td>Value is always held at VG max</td>
</tr>
<tr>
<td>VC Clamp Voltage</td>
<td>V_{VC,CLM}</td>
<td>11</td>
<td>11.7</td>
<td></td>
<td>V</td>
<td>I_{VC}=3mA</td>
</tr>
<tr>
<td>VC Clamp Series Resistance</td>
<td>R_{VC}</td>
<td></td>
<td></td>
<td>10</td>
<td>Ω</td>
<td>Delta I_{VC}=10mA</td>
</tr>
<tr>
<td>VC Under-Voltage Rising Threshold</td>
<td>V_{VCUR}</td>
<td>6.2</td>
<td>7.32</td>
<td>8.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VC Under-Voltage Falling Threshold</td>
<td>V_{VCUF}</td>
<td>6</td>
<td>7.00</td>
<td>7.9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VC Under-Voltage Hysteresis</td>
<td>V_{VCUH}</td>
<td>240</td>
<td>320</td>
<td>400</td>
<td>mV</td>
<td></td>
</tr>
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</table>

### DIFFERENTIAL AMPLIFIER AND COMPARATORS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Mode Input Voltage</td>
<td>V_{CM}</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Differential Operating Input Voltage</td>
<td>V_{SP,SN}</td>
<td></td>
<td></td>
<td>250</td>
<td>mV</td>
<td>SP-SN</td>
</tr>
<tr>
<td>SP Input Bias Current</td>
<td>I_{SP}</td>
<td>15</td>
<td>25</td>
<td>35</td>
<td>µA</td>
<td>SP=SN=VC</td>
</tr>
<tr>
<td>SN Input Bias Current</td>
<td>I_{SN}</td>
<td>25</td>
<td>37</td>
<td>50</td>
<td>µA</td>
<td>SP=SN=VC</td>
</tr>
<tr>
<td>DBST Forward Voltage</td>
<td>V_{DBST}</td>
<td>0.87</td>
<td>1.0</td>
<td></td>
<td>V</td>
<td>I_{SN}=3mA</td>
</tr>
<tr>
<td>Low Range Overcurrent Threshold</td>
<td>V_{OC,THL}</td>
<td>63</td>
<td>70</td>
<td>77</td>
<td>mV</td>
<td>VC-SN=0V</td>
</tr>
<tr>
<td>Low Range Overcurrent Turn-off Time</td>
<td>T_{OC-OFF}</td>
<td>120</td>
<td>200</td>
<td></td>
<td>ns</td>
<td>SP_SN=0V to 200mV step to 90% of VG max, SN=VC</td>
</tr>
<tr>
<td>High Range Overcurrent Threshold</td>
<td>V_{OC,THH}</td>
<td>133</td>
<td>166</td>
<td>200</td>
<td>mV</td>
<td>VC-SN=6V</td>
</tr>
<tr>
<td>Overcurrent Hysteresis</td>
<td>V_{OC-HY}</td>
<td>9</td>
<td>13</td>
<td>17</td>
<td>mV</td>
<td></td>
</tr>
</tbody>
</table>
### Electrical Specifications

Unless otherwise specified: $-40^\circ C < T_J < 125^\circ C$, $VC=EN=10.5V$, $C_{VC}=0.1\mu F$, $C_{GATE\_PGND}=1nF$, $SGND=PGND$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DIFFERENTIAL AMPLIFIER AND COMPARATORS</strong> (continued)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over Current Range switch over Threshold</td>
<td>$V_{SOTH}$</td>
<td>0.5</td>
<td>0.8</td>
<td>1</td>
<td>V</td>
<td>VC-SN</td>
</tr>
<tr>
<td>Over Current Range switch over delay$^1$: Low to high threshold</td>
<td>$T_{SOL2H}$</td>
<td>100</td>
<td>170</td>
<td>300</td>
<td>ns</td>
<td>VC-SN= -0.7V~1.7V</td>
</tr>
<tr>
<td>Over Current Range switch over delay$^1$: High to low threshold</td>
<td>$T_{SOH2L}$</td>
<td>80</td>
<td>125</td>
<td>190</td>
<td>ns</td>
<td>SN-VC= -1.7V~0.7V</td>
</tr>
<tr>
<td><strong>GATE DRIVER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Source Current</td>
<td>$I_{G_SC}$</td>
<td>-15</td>
<td>-10</td>
<td>µA</td>
<td></td>
<td>$V_G=V_{G_Hi}$, $I_{VC}=3mA$</td>
</tr>
<tr>
<td>Pull Down Peak Current to PGND$^2$</td>
<td>$I_{G_PD}$</td>
<td>1.5</td>
<td>4.0</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pull-down Gate Resistance to PGND$^2$</td>
<td>$R_{G_PD}$</td>
<td>0.3</td>
<td></td>
<td>Ω</td>
<td></td>
<td>$V_G = 1.5V @ 25^\circ C$</td>
</tr>
<tr>
<td>AC Gate Pull-down Voltage to PGND$^2$</td>
<td>$V_{G_PGND}$</td>
<td>0.2</td>
<td></td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Gate Pull-down Voltage</td>
<td>$V_{G_SGND}$</td>
<td>0.8</td>
<td>1.2</td>
<td>V</td>
<td></td>
<td>$I_g=100mA$, in OC Fault</td>
</tr>
<tr>
<td>Gate Drive Voltage to VC</td>
<td>$V_{G_Hi}$</td>
<td>7.0</td>
<td>8.0</td>
<td>11</td>
<td>V</td>
<td>$I_g=10\mu A$, $I_{VC}=3mA$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
<td>9.0</td>
<td>11</td>
<td>V</td>
<td>$I_g=2\mu A$, $I_{VC}=3mA$</td>
</tr>
<tr>
<td>Gate Fall Time</td>
<td>$t_{G_F}$</td>
<td>10</td>
<td>25</td>
<td>ns</td>
<td></td>
<td>90% to 10% of $V_G$ max.</td>
</tr>
<tr>
<td>Gate Voltage @ VC=4.5V</td>
<td>$V_{G_UVLO}$</td>
<td>0.7</td>
<td>1</td>
<td>V</td>
<td></td>
<td>$I_g=10\mu A$, SP= SN=open</td>
</tr>
<tr>
<td><strong>Enable (EN)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Threshold Voltage to VC pin</td>
<td>$V_{VC_EN}$</td>
<td>0.70</td>
<td>1.35</td>
<td>1.80</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Disable pull down current</td>
<td>$I_{dis}$</td>
<td>8</td>
<td>15</td>
<td>22</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td><strong>Fault Status: FT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FT Output Low Voltage</td>
<td>$V_{FT}$</td>
<td>0.2</td>
<td>0.5</td>
<td>V</td>
<td></td>
<td>$I_{FT}=200\mu A$, $VC&gt;8.5V$</td>
</tr>
<tr>
<td>FT Output High Leakeage Current</td>
<td>$I_{FT}$</td>
<td>10</td>
<td></td>
<td>µA</td>
<td></td>
<td>$V_{FT}=14V$</td>
</tr>
<tr>
<td>FT Delay time</td>
<td>$T_{FT-DLY}$</td>
<td>2.5</td>
<td>5.5</td>
<td>12</td>
<td>µs</td>
<td>$V_{SP_SN} = 0$~200mV step to 10% of $V_{FT}$ max, SN=VC</td>
</tr>
</tbody>
</table>

**Note 1:** These parameters are not production tested but are guaranteed by design, characterization, and correlation with statistical process control.

**Note 2:** Current sourced by a pin is reported with a negative sign.
Functional Description:
The PI2061 Cool-Switch is designed to drive an N-channel MOSFET in a high side Circuit Breaker application. As shown in Figure 1, the load current is sensed through the sense resistor (Rs). At power up the controller has a higher threshold voltage compared to steady state operation to allow capacitive load charging without nuisance tripping of the breaker.

Differential Amplifier:
The PI2061 integrates a high-speed fixed offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin and Sense Negative (SN) pin voltage with high accuracy. The amplifier output is connected to the control logic that determines the state of the fault latch. To avoid tripping the breaker due to load capacitance during initial power up a higher threshold is used. The amplifier will detect if the drop across the sense resistor reaches 166mV and discharge the gate of the MOSFET if detected. Once the load voltage approaches the input potential the threshold is lowered to 70mV. This allows for capacitive load charging and continuous current sensing without the use of a fixed sense blanking timer where excessive currents may develop glitching the input bus prior to breaking.

VC Voltage Regulator and MOSFET Drive:
The biasing scheme in the PI2061 uniquely enables the gate control relative to SGND and PGND pins via the resistor $R_{PG}$ shown in Figure 1. The VC input provides power to the control circuitry, the charge pump and the gate driver. An internal regulator clamps the VC voltage to 11.7V with respect to SGND.

The VC pin is connected through an external resistor to the input power source and drain of the MOSFET. VC switches over to the load potential once the gate drive is enabled and over current condition is not present.

The internal regulator circuit has a comparator to monitor VC voltage and pulls the gate low when VC to SGND is lower than the VC Under-Voltage Threshold. As shown in Figure 1 the lower bias resistor, $R_{PG}$ is placed between the SGND connection and the system ground.

Gate Driver:
The PI2061 has an integrated charge pump that approximately doubles the regulated VC with respect to SGND enhancing the N-Channel MOSFET gate to source voltage.

The internal gate driver controls the N-channel MOSFET such that in the on state, the gate driver applies current to the MOSFET gate driving it to bring the load up to the input voltage and into the $R_{DS(on)}$ condition.

When an over current condition is sensed the gate driver pulls the gate low to PGND and discharges the MOSFET gate with 4A peak capability. A Schottky diode (D1 in Figure 1) from PGND to the MOSFET source is required to direct the Gate high discharge current into the Source.

The PI2061 applies high gate discharge current for fast MOSFET turn off when a fault condition occurs to prevent system disruption. Fast MOSFET turn off may produce high voltage ringing due to parasitic inductance. To prevent negative peaks at SN from injecting substrate current, Schottky diode D2 (from SGND/PGND to SN pin as shown in Figure 1) is required.

Enable Input: (EN)
This input provides control of the switch state enabling and disabling with low current level signals. The active high feature allows pulling/sinking a low current from this input to disable the breaker. System control can disable the switch and reset the over current latch by pulling this pin to a logic low state.

Once enabled, the Gate pin will charge the MOSFET gate to turn the load on. The load voltage will rise, reach the input voltage and the device will sense the current continuously once the POR interval has cleared relative to the VC to SGND potential. The disable control with this input is very fast, turning the switch off in typically 200ns. The response to open during an over current event is typically 120ns and the switch will latch off until reset by bringing this input low or recycling of the input power.

Fault Status: (FT)
This open collector pin transitions to high resistance after the Fault Status is delayed for 5μs when an over-current fault or disable signal occurs. When the controller input voltage is in under voltage, (VC - SGND < 7V) this pin is high resistance as well. When the part is in a normal operating condition and gate driver is enabled this pin is low resistance. In high voltage applications this output must be translated to the system return with external circuitry. Leave this pin open if unused.

Not Recommended for New Designs
Figure 3: PI2061 Block Diagram

Figure 4: PI2061 Timing Diagram, referenced to Figure 1.
Figure 5: PI2061 State Diagram
Typical Characteristics:

**Figure 6:** Controller quiescent current vs. temperature.

**Figure 7:** VC Under-Voltage Rising threshold vs. temperature.

**Figure 8:** Gate source current vs. temperature.

**Figure 9:** Gate drive voltage to VC vs. temperature.

**Figure 10:** Low Range Overcurrent Turn-off time vs. temperature.

**Figure 11:** Low Range Overcurrent Threshold vs. temperature.

Not Recommended for New Designs
Application Information

The PI2061 Cool-Switch is a wide input voltage high side load disconnect switch.

This section describes in detail the procedure to follow when designing with the PI2061 load disconnect switch.

Biasing sequence Functionality

When Vin is applied and the load is at zero volts, the VC capacitor will charge via current flowing through RVC, D1, load resistance and RPG. If the load resistance is much lower than RPG, most of the charge and bias current flows through the load.

As VC to SGND voltage rises above the Under-Voltage Rising Threshold (V_{VCUR}) while the EN pin is High, the controller will charge the MOSFET gate and monitor the voltage across the sense resistor (V_{SP-SN}). As the MOSFET turns on, the load voltage (Vout) will rise until the MOSFET is in R_{DS(on)} and Vload=Vin. If the voltage across the sense resistor (V_{SP-SN}) is higher than the High Range Overcurrent Threshold (V_{OC-THH} 166mV) while the load rises, the gate will be discharged to PGND and latch off; otherwise Vout will keep rising, D1 becomes reverse biased and the controller bias current returns to ground through RPG.

When Vout reaches the Over Current Range switch over threshold, the over current threshold switches to the Low Range Over Current threshold (V_{OC-THL} 70mV). VC will be biased from Vout through the SN pin when Vout is a diode drop (D_{BST}) above VC as the load reaches Vin.

Upper and lower bias resistors should be selected to keep PI2061 bias voltage in regulation.

Upper Side Bias Resistor selection: RVC

RVC is placed between Vin and VC to limit the current into the clamp under a shorted load condition. This will allow VC to regulate with respect to SGND/PDND node when the MOSFET is in off condition and SGND/PGND node is pulled low via D1, Rs and low load resistance.

The RVC resistor can be calculated using the following expression:

And RVC maximum power dissipation is:

And RPG maximum power dissipation is:

Where:

- Boot Strap diode minimum forward voltage, use 0.8V
- Boot Strap diode minimum forward voltage, use 1.0V
- VC maximum quiescent current, use 2.1mA

RVC and RPG calculation example

Vin (minimum) = 40V and Vin (maximum) = 50V

Note that in the case of a light load while the PI2061 is disabled, a voltage will appear at Vout due to the resistance between the VC pin and the SP and SN pins. The approximate value will be:

Where:

- Output load resistance when the load is inactive
Schottky Diodes Selection: D1 and D2
Diode D1 (See Figure 1 & Figure 14.) must be a low reverse leakage Schottky diode capable of supporting 4A of peak gate discharge current for 10ns. Diode D2 must be a low reverse leakage Schottky diode capable of supporting 1A peak. Both diodes will have a reverse voltage of 13V during normal operation.

Recommended diode for D1 and D2: PMEG4005EJ from NXP

Sense Resistor Selection: Rs
In typical load switch application the sense resistor is based on minimum trip current to allow maximum normal load current without interruption. Calculate Rs value at minimum Low Range Overcurrent Threshold voltage ($V_{OC-THL}$):

Where:
- $V_{OC-THL}$: Minimum Low Range Overcurrent Threshold voltage, 63mV
- $I_{THL}$: Required minimum trip current

Enable Input Circuit: EN
EN pin can be tied directly to VC OR LEFT FLOATING if PI2061 should be enabled when the power is applied. If the user wants to control the device enable function, then EN pin can be pulled low with a resistor and signal FET, signal transistor or open collector logic as shown in Figure 12. Note that the enable control signal phase must be inverted.

Use an enable resistor ($R_{EN}$) value between 300kΩ and 400kΩ with voltage rating that meets maximum input voltage.

Fault Indication: FT
FT is an open collector output and its return is referenced to SGND. When the SGND pin is floating on a bias resistor ($R_{PG}$) or in a constant current circuit, a level shift circuit can be added to create an output referenced to the system ground. See Figure 13.

Alternative Bias Circuit: Constant current circuit for high voltage application.
In a wide operating input voltage range the size of $R_{VC}$ and $R_{PG}$ may be become large to support power dissipation. A simple constant current circuit, shown in Figure 14 can be used instead of $R_{VC}$ and $R_{PG}$ to allow the circuit to operate between 18V and 80V (100V/100ms transient) with low power dissipation components. Please refer to Picor application notes for more details on how to design a floating bias with the constant current circuit.
N-Channel MOSFET Selection:
Several factors affect MOSFET selection including cost and following ratings; on-state resistance ($R_{DS(on)}$), DC current, short pulse current, avalanche, power dissipation, thermal conductivity, drain-to-source breakdown voltage ($BV_{DSS}$), gate-to-source voltage ($V_{GS}$), and gate threshold voltage ($V_{GSS(TH)}$).

The first step is to select a suitable MOSFET based on the $BV_{DSS}$ requirement for the application. The $BV_{DSS}$ voltage rating should be higher than the applied $Vin$ voltage plus expected transient voltages. Stray parasitic inductance in the circuit can also contribute to significant transient voltage condition, particularly during MOSFET turn-off after an over current fault has been detected.

In a disconnect switch application when the output is shorted, a large current is sourced from the power source through the MOSFET. Depending on the input impedance of the system, the current may get very high before the MOSFET is turned off. Make sure that the MOSFET pulse current capability can withstand the peak current. Also, such high current conditions will store energy even in a small parasitic inductance. The PI2061 has a very fast response time to terminate a fault condition achieving 120ns typical and 200ns maximum. This fast response time will minimize the peak current to keep stored energy and MOSFET avalanche energy very low to avoid damage (electrical stress) to the MOSFET.

Peak current during output short is calculated as follows, assuming that the input power source has very low impedance and it is not a limiting factor:

$$I_{peak} = \frac{V_{in}}{R_{DS(on)}}$$

Where:
- $I_{peak}$: Peak current in the MOSFET right before it is turned off.
- $V_{in}$: Input voltage at MOSFET drain before output short condition occurred.
- $R_{DS(on)}$: Over current turn-off time. This will include PI2061 delay and the MOSFET turn off time.
- $L$: Circuit parasitic inductance

The MOSFET avalanche energy during an input short is calculated as follows:

$$E_{avalanche} = \frac{1}{2}I_{peak}^2 \cdot BV_{DSS}$$

Where:
- $E_{avalanche}$: Avalanche energy
- $BV_{DSS}$: MOSFET breakdown voltage

MOSFET $R_{DS(on)}$ and maximum steady state power dissipation are closely related. Generally the lower the MOSFET $R_{DS(on)}$ the higher the current capability and the lower the resultant power dissipation for a given current. This leads to reduced thermal management overhead, but will ultimately be higher cost compared to higher $R_{DS(on)}$ parts. It is important to understand the primary design goal objectives for the application in order to effectively trade off the performance of one MOSFET versus another.

Power dissipation in load switch circuits is derived from the total drain current and the on-state resistance of the selected MOSFET.

MOSFET power dissipation:

$$P_{dissipation} = I_{DS} \cdot R_{DS(on)}$$

Where:
- $I_{DS}$: MOSFET Drain Current
- $R_{DS(on)}$: MOSFET on-state resistance

Note:
In the calculation use $R_{DS(on)}$ at maximum MOSFET temperature because $R_{DS(on)}$ is temperature dependent. Refer to the normalized $R_{DS(on)}$ curves in the MOSFET manufacturer’s datasheet. Some MOSFET $R_{DS(on)}$ values may increase by 50% at 125°C compared to values at 25°C.

The Junction Temperature rise is a function of power dissipation and thermal resistance.

$$\Delta T = \frac{P_{dissipation}}{h_{JA}}$$

Where:
- $\Delta T$: MOSFET Junction-to-Ambient thermal resistance
Typical Application Example 1:
12V Load Switch

Requirement:
Input Bus Voltage = 12V (±10%, 10.8V to 13.2V)
Maximum Load Current = 10A
Minimum Trip current = 12A
Maximum Ambient Temperature = 75°C

Solution:
PI2061 with a suitable external MOSFET should be used, configured as shown in the circuit schematic in

Select a suitable N-Channel MOSFET: Most industry standard MOSFETs have a $V_{GS}$ rating of +/-12V or higher. Select an N-Channel MOSFET with a low $R_{DS(on)}$ which is capable of supporting the full load current with some margin, so a MOSFET capable of at least 18A in steady state is reasonable. An exemplary MOSFET having these characteristic is the Si4630DY from Siliconix.

From Si4630DY datasheet:
- N-Channel MOSFET
- $V_{DS}= 25V$
- $I_{D} = 32A$ continuous drain current
- $I_{D}(Pulse) = 70A$ Pulsed drain current
- $V_{GS}(MAX)=±16V$
- $R_{ThA}= 80°C/W$ under Steady State condition
- $R_{DS(on)}=2.2mΩ$ typical and 2.7mΩ maximum at $I_{D}=20A$, $V_{GS}=10V$, $T_{J}=25°C$

Select Sense Resistor:

$R_s$ power dissipation at maximum operating current

Maximum trip current

Power dissipation:

$R_{DS(on)}$ is 2.7mΩ maximum at 25°C & 10 V$_{GS}$ and will increase as the temperature increases. Add 40°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 115°C (75°C + 40°C) $R_{DS(on)}$ will increase by 37%.

Maximum Junction temperature

---

VC Bias: Vin maximum input is 13.2V, this is higher than the 11V VC minimum Clamp Voltage ($V_{VC-SGND}$) minimum, but the minimum input voltage is greater than $V_{VC-SGND}$ minimum. Use 300Ω resistor for each $R_{VC}$ and $R_{PG}$ to minimize regulator clamp current.

Power dissipation of $R_{VC}$ and $R_{PG}$:

Both resistors have very low power dissipation, less than 50mW. Any package size resistor, 0201 (0603 metric) or larger, can be used.

EN:
Tie EN pin to VC since Enable function is always on.

FT:
Fault function is not required, leave fault pin unconnected.

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Figure 15: PI2061 in 12V Bus high side load switch application.
Typical application Example 2:

Requirement:
+48V Load Switch with Enable Function
Bus Voltage = +48V (+36V to +55V)
Maximum Load Current = 5A
Minimum Trip current = 6A
Maximum Ambient Temperature = 60°C

Solution:
PI2061 with a suitable MOSFET should be used and configured as shown in Figure 16.

Select a suitable N-Channel MOSFET: Select a MOSFET with voltage rating higher than the input voltage, Vin, plus any expected transient voltages, with a low R_{DS(on)} that is capable of supporting the full load current with margin. For instance, a 100V rated MOSFET with 10A current capability is suitable. An exemplary MOSFET having these characteristic is IRF7853Pbf from International Rectifier.

From the IRF7853Pbf datasheet:
- N-Channel MOSFET
  - V_{GS} = 100V
  - I_D = 8.3A maximum continuous drain current at 25°C
  - I_{D-PULSE} = 66A pulsed drain current
  - V_{GS(MAX)} = ±20V
  - R_{DUA} = 50°C/W on 1in² copper, t ≤ 10seconds
  - R_{DUA} for continuous operation not provided
  - R_{DS(on)}=14.4mΩ typical at V_{GS}=10V, T_J=25°C
  - R_{DS(on)}=18mΩ maximum at V_{GS}=10V, T_J=25°C

Select Sense Resistor:
Rs power dissipation at maximum operating current

Maximum trip current

Power dissipation:
R_{DS(on)} is 18mΩ maximum at 25°C & 10 V_{GS} and will increase as the temperature increases. Add 20°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 80°C (60°C + 20°C) R_{DS(on)} will increase by 40%.

at maximum at 80°C

Recommended Schottky: PMEG4005EJ from NXP or equivalent

Not Recommended for New Designs
Enable Input Circuit: EN
Pull EN pin to ground (return) to disable. This can be accomplished with a signal transistor (Q1) in open collector configuration and a pull-up resistor \( R_{EN} \).

A 5% 360kΩ resistor can be used to pull down on EN pin. Note that the control signal phase is inverted.

Figure 16: PI2061 in high side +48V application, VC is biased through a bias resistor

Layout Recommendation:
Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for the PI2061 is shown in Figure 17.

- Use a solid ground (return) plane to reduce circuit parasitics.
- Connect Rs terminal at SP pin side, D1 cathode and all MOSFET source pins together with a wide trace to reduce trace parasitics and to accommodate the high current output. Connect Rs terminal at SN pin side to the load with a wide trace. Also connect all MOSFET drain pins together with a wide trace to accommodate the high current input.
- Kelvin connect SP pin and SN pin to Rs terminals.
- The VC bypass capacitor should be located as close as possible to the VC and SGND pins. Place the PI2061 and VC bypass capacitor on the same layer of the board. The VC pin and \( C_{VC} \) PCB trace should not contain any vias.
- Dedicate a small copper area on lower layer underneath the controller for PGND and SGND to make a single point connection and simplify layout interconnect. Make sure that Vin to Vout current return path is solid underneath the MOSFET (M1) and the sense resistor (R1).
- Make sure D1 and D2 connecting traces are very short to reduce parasitic inductance that might produce voltage drop due MOSFET fast turn off.
- Use 1oz of copper or thicker if possible to reduce trace resistance and power dissipation.

Figure 17: PI2061 layout recommendation
NOTES:
1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity does not exceed .05mm
3. Package is variation of JEDEC MO-229
4. Warpage does not exceed .05mm

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Transport Media</th>
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<tr>
<td>PI2061-00-QEIG</td>
<td>3mm x 3mm 10 Lead DFN</td>
<td>T&amp;R</td>
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Vicor Corporation
25 Frontage Road
Andover, MA 01810
USA

Picor Corporation
51 Industrial Drive
North Smithfield, RI 02896
USA

Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com
Tel: 800-735-6200
Fax: 978-475-6715