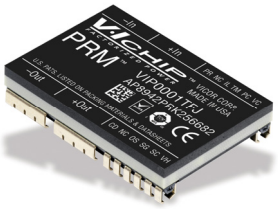
PRM™

Regulator



FEATURES

- 45V (38 to 55 V_{IN}), non-isolated ZVS buck-boost regulator
- 5 to 55 V adjustable output range
- Building block for high efficiency DC-DC systems
- 400W Output Power in 1.11 in^2 footprint
- 97% typical efficiency, at full load
- 1,360 W/in^3 (83 W/cm^3) Power Density
- Enables a 48 V to 1.5 V, 230 A isolated, regulated solution with total footprint of 3.3in^2 (21cm^2)
- Flexible “Remote Sense” architecture optimizes regulation / feedback loop design to fit application requirements
- Current Feedback signal allows dynamic adjustment of current limit setpoint
- 3.61 MHrs MTBF (MIL-HDBK-217Plus Parts Count)

TYPICAL APPLICATIONS

- High Efficiency Server Processor and Memory Power
- High Density ATE system DC-DC power
- Telecom NPU and ASIC core power
- LED drivers
- High Density Power Supply DC-DC rail outputs
- Non-isolated power converters

DESCRIPTION

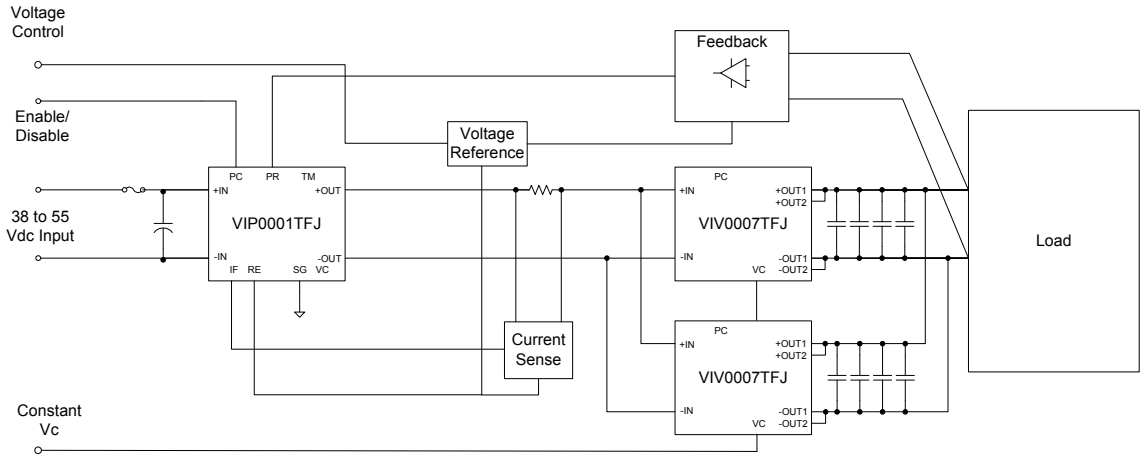
The V•I Chip PRM™ Regulator is a high efficiency converter, operating from a 38 to 55 Vdc input to generate a regulated 5 to 55 Vdc output. The ZVS Buck – Boost topology enables high switching frequency (~1 MHz) operation with high conversion efficiency. High switching frequency reduces the size of reactive components enabling power density up to 1,360 W/in^3.

The full V•I Chip package is compatible with standard pick-and-place and surface mount assembly processes with a planar thermal interface area and superior thermal conductivity.

In a Factorized Power Architecture™ system, the VIP0001TFJ and downstream VTM™ transformer minimize distribution and conversion losses in a high power solution.

An external control loop and current sensor maintain regulation and enable flexibility both in the design of voltage and current compensation loops to control of output voltages and currents.

48 V to 1.5 V, 230A Voltage Regulator



1.0 ABSOLUTE MAXIMUM RATINGS

The ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. All voltages are specified relative to SG unless otherwise noted. Positive pin current represents current flowing out of the pin.

	Min	Max	Unit
PR	-0.3	10.5	V
		±10	mA
PC	-0.3	5.7	V
		±10	mA
TM	-0.3	5.7	V
		±1	mA
+IN to –IN	-1	62	V
VS	-0.5	10.5	V
		±100	mA
SG		±100	mA
IF	-0.5	5.7	V
RE	-0.3	5	V
VC to –OUT	-0.5	18	V
		±1.8	A
+OUT to –OUT	-1	62	V
Output Current		±11	A
Operating Analog IC Junction Temperature	-40	125	°C
Storage Temperature	-40	125	°C

2.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions, T_J = 25 ºC and output voltage from 20V to 55V, unless otherwise noted. **Boldface specifications apply over the temperature range of -40 ºC < T_J < 125 ºC (T-grade).**

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
POWER INPUT SPECIFICATION						
Input Voltage range	V_{IN}		38	45	55	V
V_{IN} Slew Rate	dV_{IN}/dt	0 < V_{IN} < 18 V	0.001		1000	V/ms
No Load Power Dissipation	P_{NL}	PC High, V_{IN} = 45 V		2.4	4	W
Input Quiescent current	I_{QC}	PC Low, V_{IN} = 45 V		4.5	8.5	mA
Input Current	I_{IN_DC}	I_{OUT} = 8.33A, V_{IN} = 38 V, V_{OUT} = 48 V		10.9	11.0	A
Input Capacitance (Internal)	C_{IN_INT}	Effective value, V_{IN} = 45 V (see Fig. 20)		4		µF
Input Capacitance (Internal) ESR	R_{Cin}			1.5		mΩ
POWER OUTPUT SPECIFICATION						
Output Voltage range	V_{OUT}		5	48	55	V
Output Current	I_{OUT}	See Fig.16, SOA			8.33	A
Output Power	P_{OUT}	See Fig.16, SOA			400	W
Output Turn-ON Delay	T_{ON}	From V_{IN} applied, PC floating From PC pin release, V_{IN} applied, T_{OFF} expired		20		µs
Current Sharing accuracy	I_{OUT_PS}	Equal input, output and PR voltage at full load; V_{IN} = 45 V, V_{OUT} = 48 V, exclusive of current limit			±10	%
		Equal input, output and PR voltage at full load; Over line, trim, and temperature; exclusive of current limit			See sec 10.6	%
Efficiency	η	Nominal line, full load, V_{OUT} = 48V	96.5	97.4		%
		50% load and V_{OUT} = 48 V; over temperature	94.8			%
		50% load; over temperature	90.0			%
Output Discharge current	I_{OD}	Section 4.0		13		mA
Output Voltage Ripple	V_{OUT_PP}	C_{OUT_EXT} = 0 F, I_{OUT} = 8.33 A, V_{IN} = 45 V, V_{OUT} = 48 V, 20 MHz BW		960	1500	mV
Output Inductance (Parasitic)	L_{OUT_PAR}	Frequency @ 1 MHz, Simulated J-Lead model		1.9		nH
Output Capacitance (Internal)	C_{OUT_INT}	Effective value, V_{OUT} = 48 V (see Fig. 20)		4		µF
Output Capacitance (Internal) ESR	R_{Cout}			1.5		mΩ
POWERTRAIN PROTECTIONS						
Input Undervoltage Turn-ON	V_{IN_UVLO+}	Instantanous powertrain shutdown, latched after T_{BLNK}		35.75	37.13	V
Input Undervoltage Turn-OFF	V_{IN_UVLO-}		31.97	33.56		V
Input Overvoltage Turn-ON	V_{IN_OVLO+}	Instantanous powertrain shutdown, latched after T_{BLNK}	55.91	57.24		V
Input Overvoltage Turn-OFF	V_{IN_OVLO-}			58.44	59.91	V
Overcurrent (IF) and Input Over/Undervoltage Blanking Time	T_{BLNK}		50	120	150	µs
Output Overvoltage Threshold	V_{OUT_OVLO+}	Instantaneous, latched shutdown	55.25	56.57	59.04	V
Thermal Shutdown Setpoint	T_{J_OTP}	Instantaneous, latched shutdown; guaranteed by design, not production tested; V_{TM} = 4.03V	130			°C
Overtemperature, Output Overvoltage and PC Shutdown Response Time	T_{PROT}			2		µs
Short Circuit Vout Threshold	V_{SC_VOUT}			3.0		V
Short Circuit Vout Recovery Threshold	V_{SC_VOUTR}			4.0		V
Short Circuit Vpr Threshold	V_{SC_VPR}			7.2		V
Short Circuit Vpr Recovery Threshold	V_{SC_VPRR}			7.1		V
Short Circuit Timeout	T_{SC}	Short Circuit fault latched after V_{SC_VOUT} and V_{SC_VPR} thresholds persist for this time		20		ms
Short Circuit Recovery Time	T_{SCR}			0.1		ms
Output Power Limit	P_{PROT}		400			W

3.0 SIGNAL CHARACTERISTICS

Specifications apply over all line and load conditions, T_J = 25 ºC and Output Voltage from 20V to 55V, unless otherwise noted.
Boldface specifications apply over the temperature range of -40 ºC < T_J < 125 ºC (T-grade).

Primary Control — **PC**

- The PC pin enables and disables the PRM; When held below ~2.4 V the PRM will be disabled.
- In PRM array configurations, PC pins should be connected in order to synchronize startup.
- PC pin is 5 V during normal operation.
- It is a weak pull-down during any fault mode excluding short circuit. PC is a strong pull-down to SG if a Short Circuit fault is latched.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Regular Operation	PC Voltage	V_{PC}		4.7		5.3	V
		PC Available Current	I_{PC_OP}		1.8			mA
	Startup	PC Source Current	I_{PC_EN}	After T_{OFF}		90		µA
		Minimum Time to Start	T_{OFF}	Section 5.0	10.0	18.0	30.0	ms
Digital Input / Output	Startup	PC Enable Threshold	V_{PC_EN}			2.50	3.20	V
	Standby	PC Disable Threshold	V_{PC_DIS}		1.75	2.40		V
		PC Resistance (External)	R_{PC_EXT}	Max Resistance to SG required to disable the PRM	300			Ω
Digital Output [Short Circuit Fault]	Fault	PC Sink Current to SG	I_{PC_SC}	Short circuit, PC Voltage 1 V or above		25		mA
Digital Output [All other Faults]	Fault	PC Sink Current to ~1V	I_{PC_FAULT}	Tempature, Over- and under-Voltage, Overcurrent		10		µA

Voltage Source — **VS**

- Intended to power feedback components and/or auxiliary circuits.
- 9 V, 5mA regulated voltage source
- With > 5% output load, VS ripple typically 100mV

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Regular Operation	VS Voltage	V_{VS}		8.55	9.00	9.45	V
		VS Available Current	I_{VS}		5			mA
		VS Voltage Ripple	V_{VS_PP}	Iout = 0A, Cvs_ext=0. Maximum specification includes powertrain operation in burst mode.		100	400	mV
	Transition	VS Capacitance (External)	C_{VS_EXT}				0.04	µF
		VS Fault Response Time	T_{FR_VS}	From fault recognition to VS = 1.5 V		30		µs

Reference Enable — **RE**

- RE signals succesfull startup and powertrain ready to operate
- Intended to power and enable the feedback circuit reference
- 3.3V, 8mA regulated voltage source

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Regular Operation	RE Voltage	V_{RE}		3.0	3.3	3.6	V
		RE Available Current	I_{RE}		8.0			mA
		RE Regulation	$\%_{RE}$	across load and temperature		±2.5		%
		RE Voltage Ripple	V_{RE_PP}	in burst mode		100		mV
	Transition	PC to RE Delay	T_{PC_RE}	Fault detected		100		µs
		RE Capacitance (External)	C_{RE_EXT}				0.1	µF
		VS to RE Delay	T_{VS_RE}	VS = 8.1 V to RE high, $V_{IN} > V_{IN\_UVLO-}$		1		ms

Control Node — **PR**

- Modulator control node input
- 0.5mA constant current sink when externally driven
- 0.79V, up to 2mA voltage source when externally pulled low

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input	Regular Operation	PR Voltage Active Range	V_{PR}		0.79		7.40	V
		PR Source Current	I_{PR}	$V_{PR} \leq 0.79V$			2	mA
		PR Sink Current	I_{PR_Low}	$V_{PR} > 0.79V$	250	500	750	µA
		PR Resistance to SG	R_{PR}			93.3		kΩ

Current Feedback — **IF**

- A voltage proportional to the PRM output current must be supplied externally to the IF pin in order for the device to properly protect overcurrent events and to enable output current limit (clamp)
- Overcurrent protection trip will cause instantaneous powertrain disable, latched after T_{BLNK}

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input	Regular Operation	Current Limit (clamp) Threshold	V_{IF_IL}	V_{IN} = 45 V; T_J = 25 °C	1.90	2.00	2.10	V
		Overcurrent Protection Threshold	V_{IF_OC}	Not Production Tested; Guaranted by Design; T_J = 25 °C	2.58	2.69	2.80	
		IF Input Impedance	R_{IF}		2.11	2.13	2.15	kΩ
		Current Limit Bandwidth	BW_{IL}			2		kHz

Temperature Monitor	TM

• The TM pin monitors the internal temperature of the PRM analog control IC to within ±5 °C.
• Room temperature setpoint is ~ 3 V, approximate gain is 10 mV/°C.
• "Power Good" flag to verify that the PRM is operating

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Regular Operation	TM Voltage	V_{TM}	Full temperature range	2.12		4.04	V
		TM Voltage reference	V_{TM_AMB}	T_J = 27 °C	2.94	3.00	3.06	V
		TM Voltage Ripple	V_{VS_PP}	powertrain in burst mode		200		mV
		TM Available Current	I_{TM}		100			µA
		TM Gain	A_{TM}			10		mV/°C
Digital Output [Fault Flag]	Fault or Standby	TM Disabled Current	I_{TM_DIS}	DC state with TM Voltage +/- 0.5V. This is a high impedance state.		0.0		mA

Signal Ground	SG

• All control signals must be referenced to this pin, with the exception of VC
• SG is internally connected to -IN and -OUT

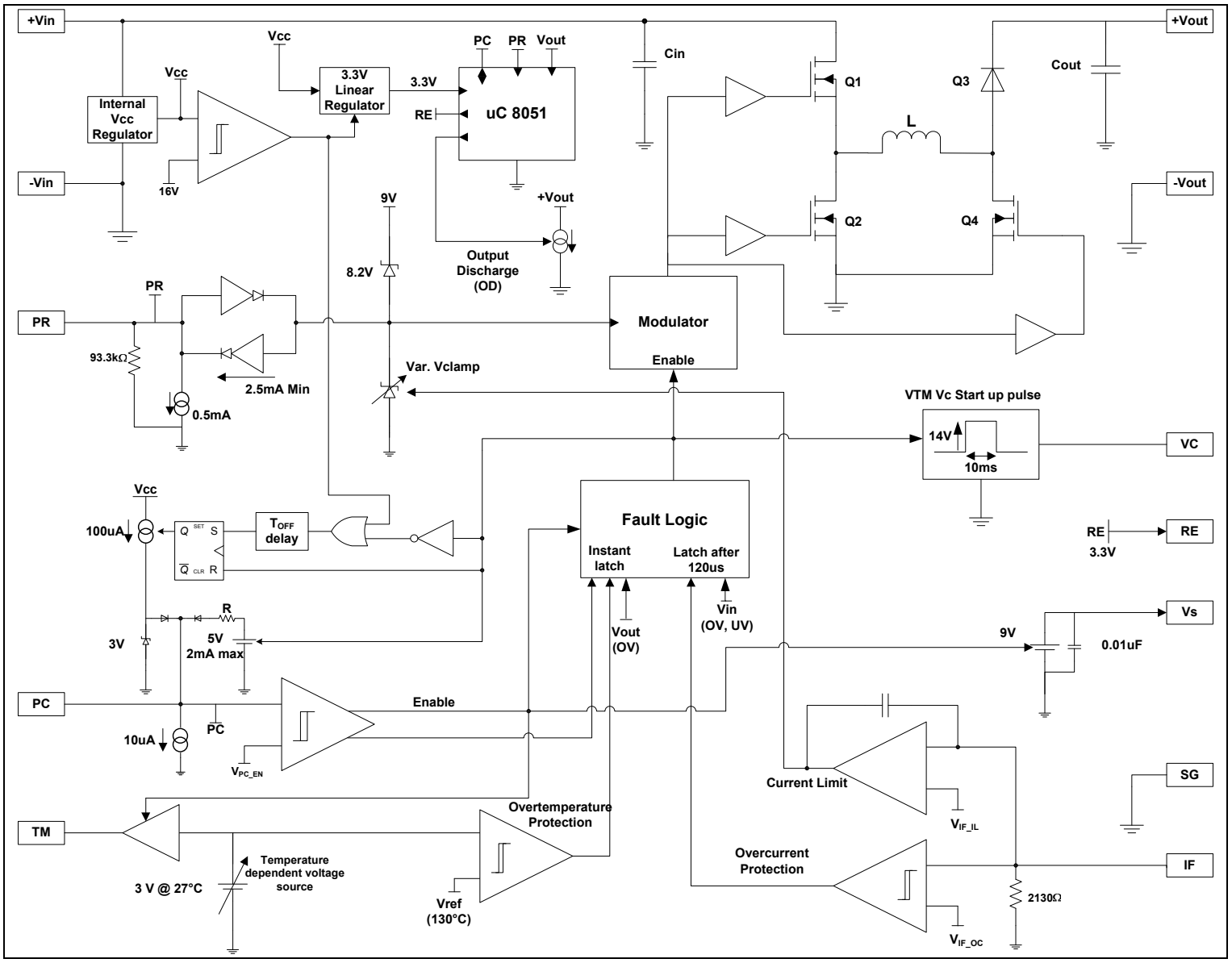
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input / Output	Any	Maximum Allowable Current	I_{SG}		-100		100	mA

VTM Control	VC

• Used to synchronize start up of downstream VTM converter.
• 14V nominal, 10ms voltage pulse
• If not used, must be resistively terminated to -OUT

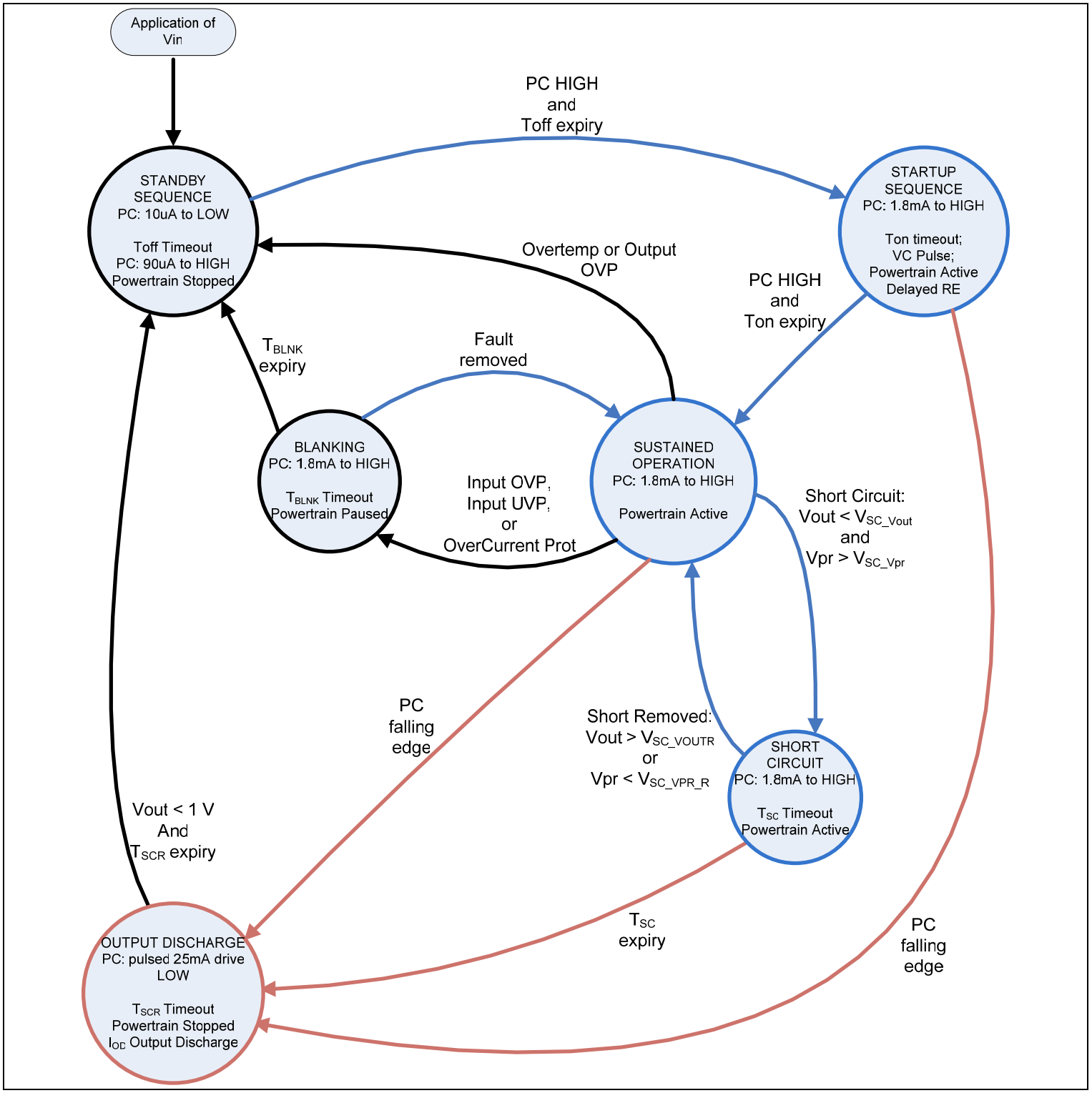
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Startup	VC Voltage	V_{VC}	R_{VC} = 68Ω	13			V
		VC Current Limit	I_{VC}	V_C = 14 V, V_{IN} > 20 V	200	500		mA
		VC duration	T_{VC}		7	10	16	ms
		VC Slew Rate	dVC/dt	R_{VC} = 1kΩ		20		V/µs

4.0 FUNCTIONAL BLOCK DIAGRAM



5.0 HIGH LEVEL FUNCTIONAL STATE DIAGRAM

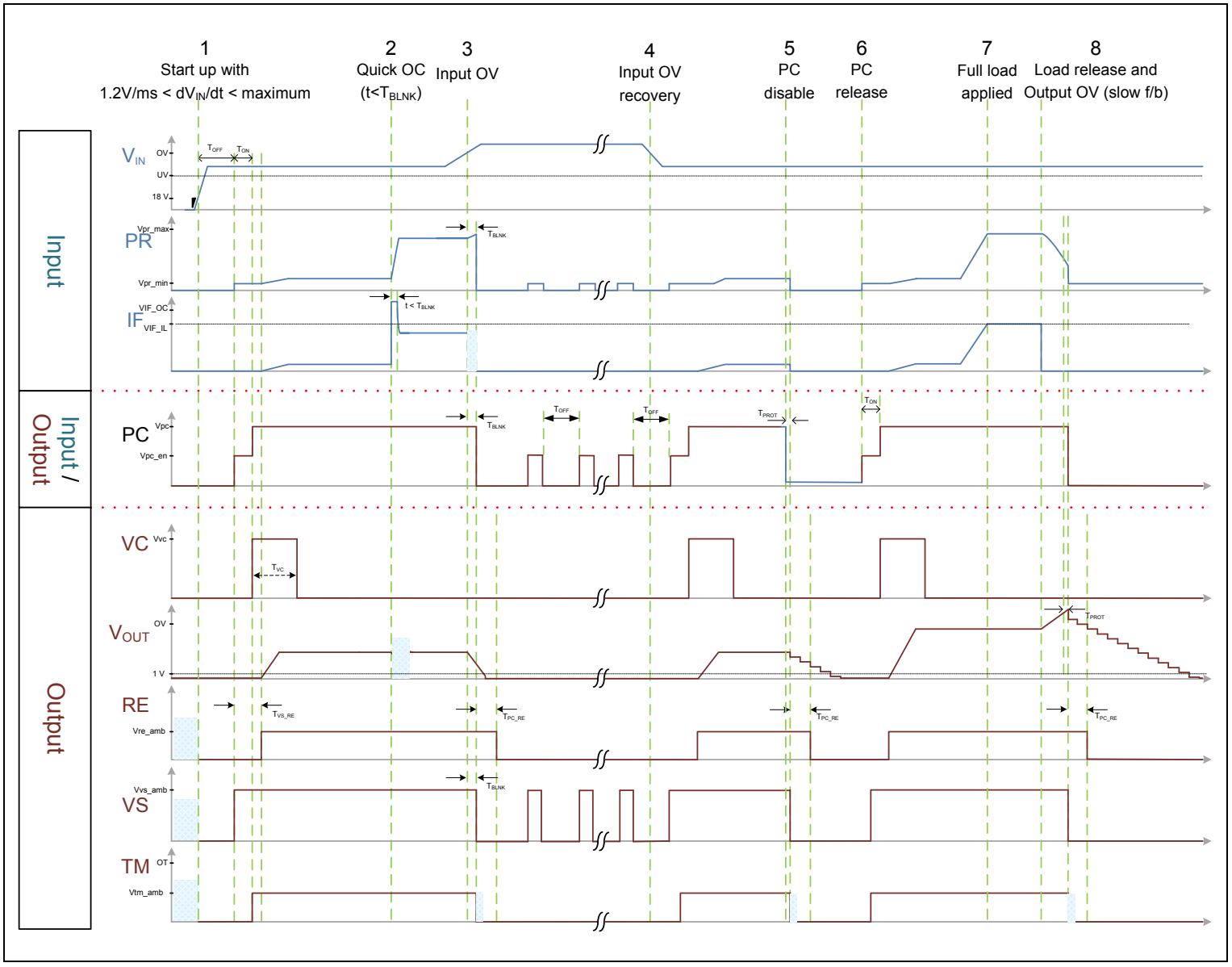
Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.

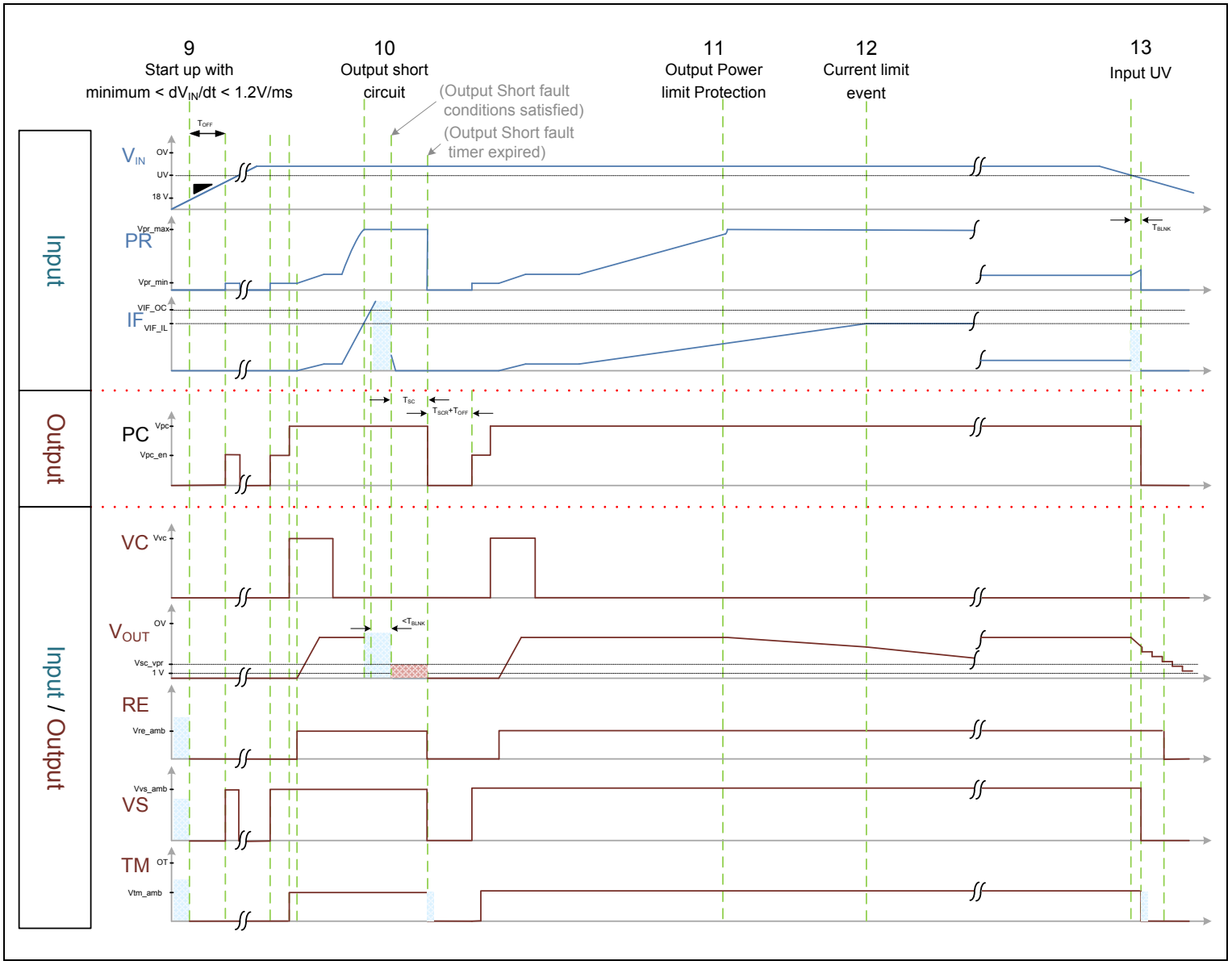


6.0 TIMING DIAGRAMS

Module Inputs are shown in blue; Module Outputs are shown in brown; Timing diagrams assumes the following:

- Single PRM (no array)
- VS powers error amplifier
- RE powers voltage reference and output current transducer
- I_{OUT} is sensed, scaled, and fed back to IF pin such that IF = 2.00 V at full load




9
Start up with
minimum < dVIN/dt < 1.2V/ms
10
Output short
circuit
(Output Short fault
conditions satisfied)
(Output Short fault
timer expired)
11
Output Power
limit Protection
12
Current limit
event
13
Input UV
Input
Output
Input / Output
VIN
OV
UV
18 V
TOFF
PR
Vpr_max
Vpr_min
TBLNK
IF
VIF_OC
VIF_IL
TSC
TSCR+TOFF
PC
Vpc
Vpc_en
VC
Vvc
VOUT
OV
Vsc_vpr
1 V
<TBLNK
RE
Vre_amb
VS
Vvs_amb
TM
OT
Vtm_amb

7.0 APPLICATIONS CHARACTERISTICS

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

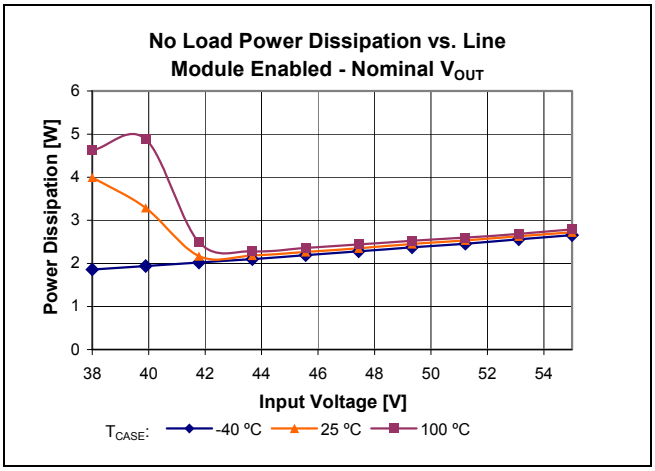


Figure 1 - No load power dissipation vs. V_{IN}, module enabled

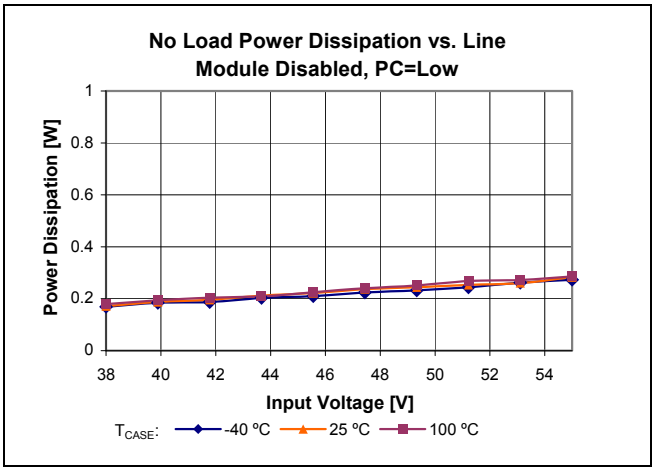


Figure 2 - No load power dissipation vs. V_{IN}, module disabled

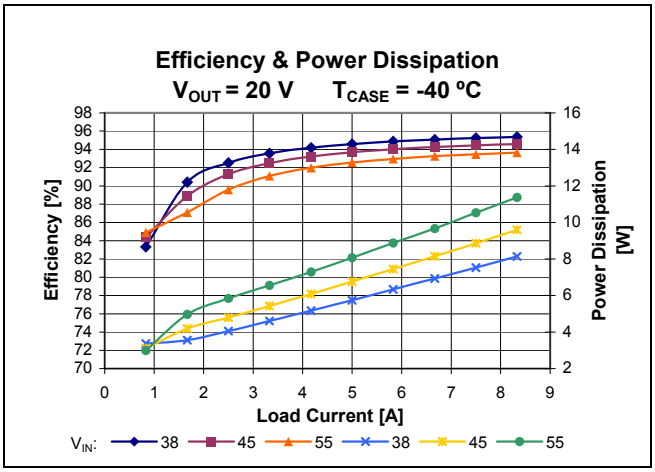


Figure 3 – Total efficiency and power dissipation vs. V_{IN} and I_{OUT}, V_{OUT}=20V, T_{CASE}=-40ºC

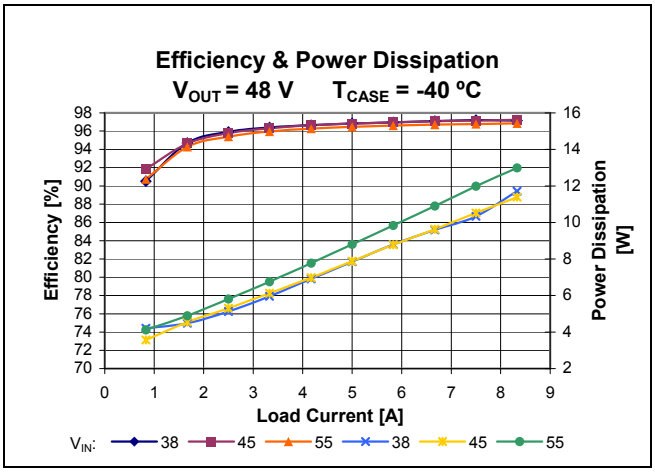


Figure 4 – Total efficiency and power dissipation vs. V_{IN} and I_{OUT}, V_{OUT}=48V, T_{CASE}=-40ºC

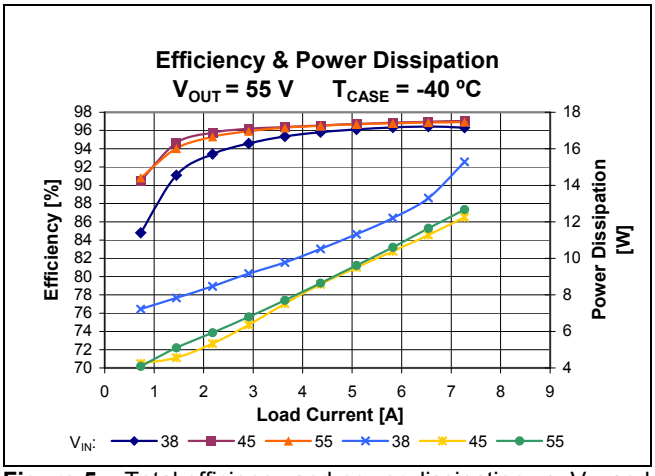


Figure 5 – Total efficiency and power dissipation vs. V_{IN} and I_{OUT}, V_{OUT}=55V, T_{CASE}=-40ºC

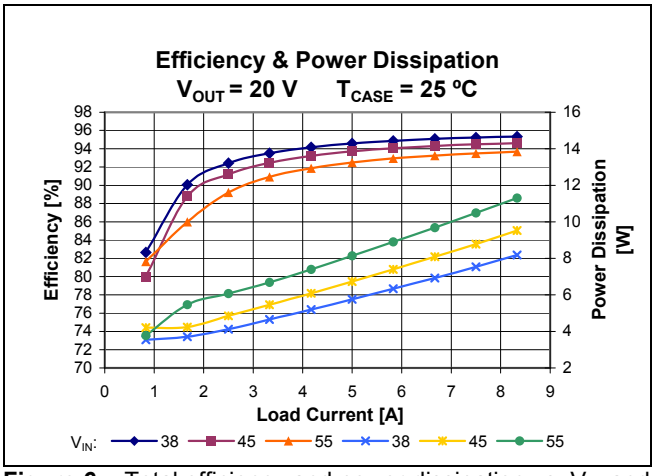


Figure 6 – Total efficiency and power dissipation vs. V_{IN} and I_{OUT}, V_{OUT}=20V, T_{CASE}=25ºC

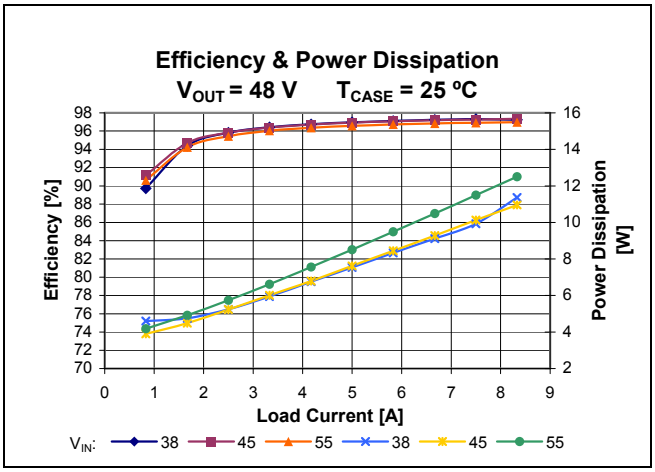


Figure 7 – Total efficiency and power dissipation vs. V_{IN} and I_{OUT}, V_{OUT}=48V, T_{CASE}=25ºC

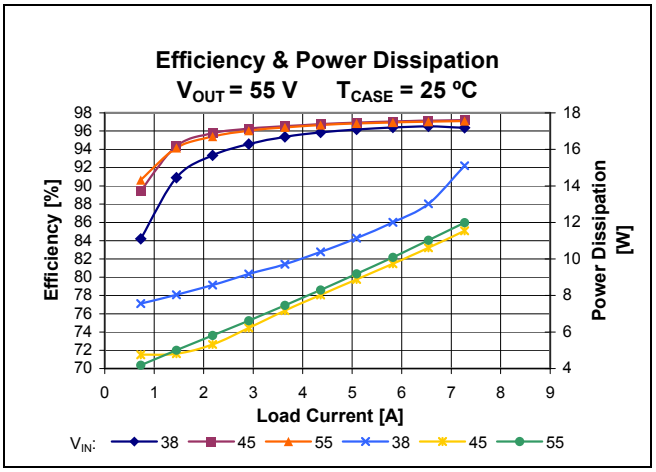


Figure 8 – Total efficiency and power dissipation vs. V_{IN} and I_{OUT}, V_{OUT}=55V, T_{CASE}=25ºC

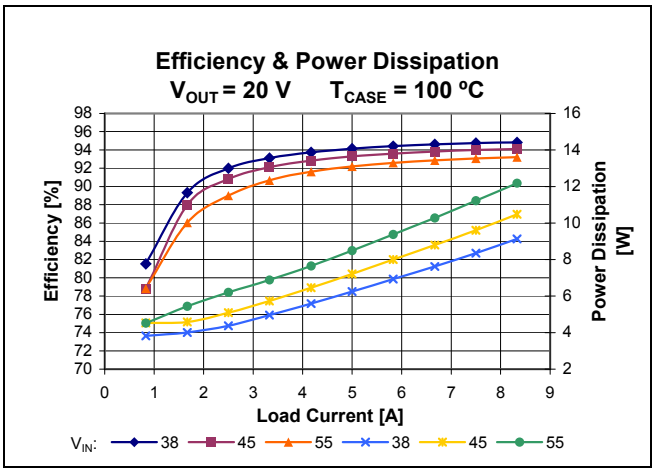


Figure 9 – Total efficiency and power dissipation vs. V_{IN} and I_{OUT}, V_{OUT}=20V, T_{CASE}=100ºC

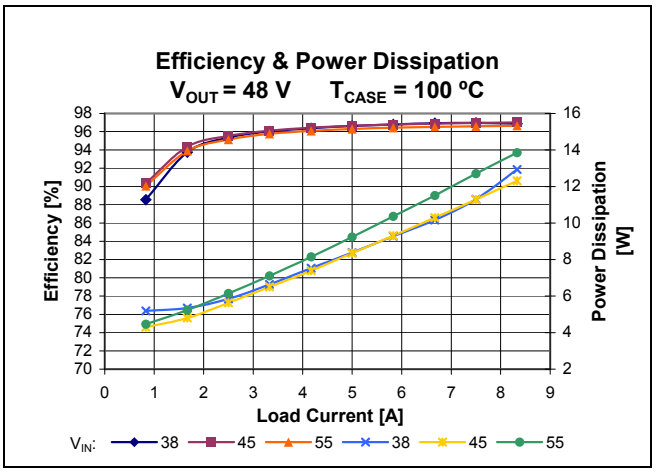


Figure 10 – Total efficiency and power dissipation vs. V_{IN} and I_{OUT}, V_{OUT}=48V, T_{CASE}=100ºC

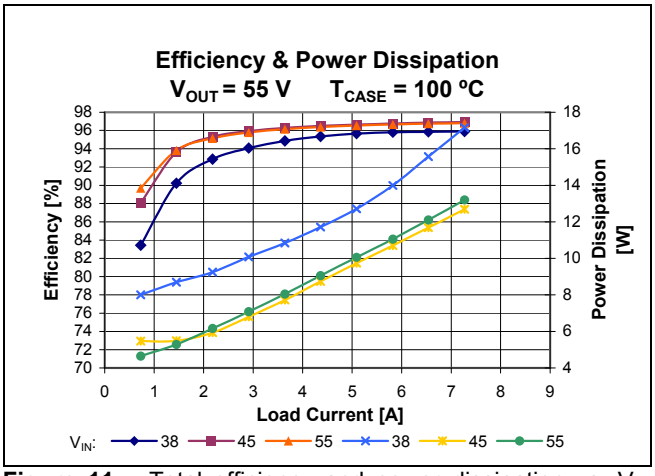


Figure 11 – Total efficiency and power dissipation vs. V_{IN} and I_{OUT}, V_{OUT}=55V, T_{CASE}=100ºC

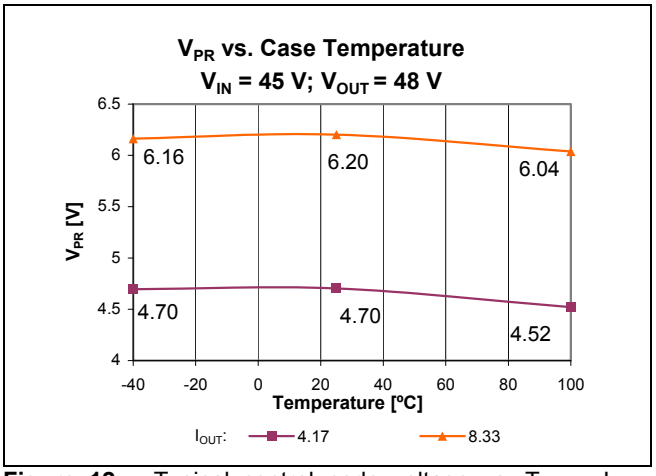


Figure 12 – Typical control node voltage vs. T_{CASE}, I_{OUT}; V_{IN}=45V, V_{OUT}=48V

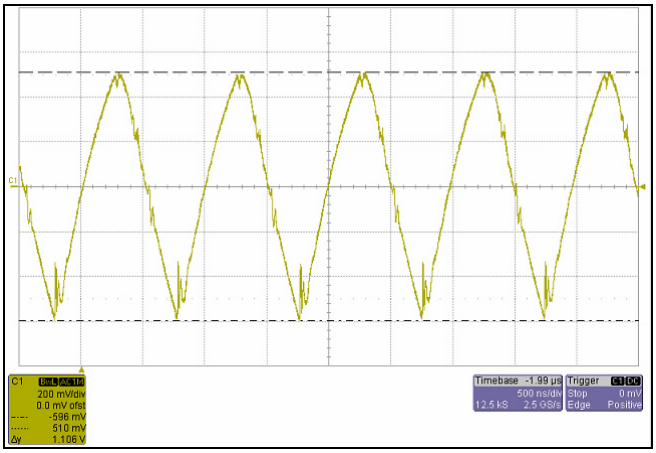


Figure 13 – Typical output voltage ripple waveform, T_{CASE}= 30ºC, V_{IN}=45V, V_{OUT}=48V, I_{OUT}=8.33A, no external capacitance.

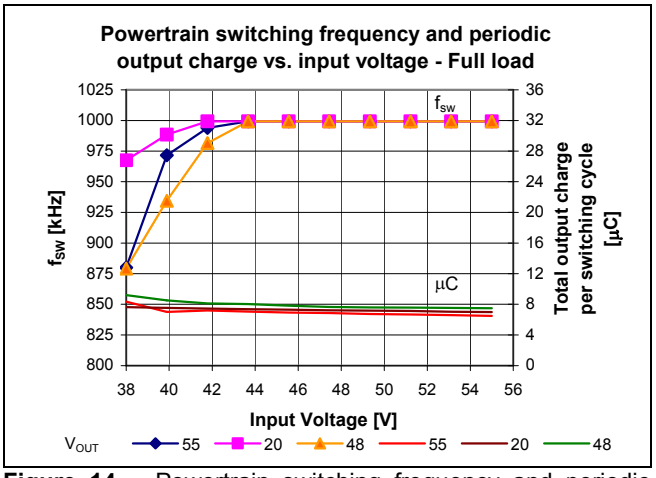


Figure 14 – Powertrain switching frequency and periodic output charge vs. V_{IN}, V_{OUT}; I_{OUT}=8.33A

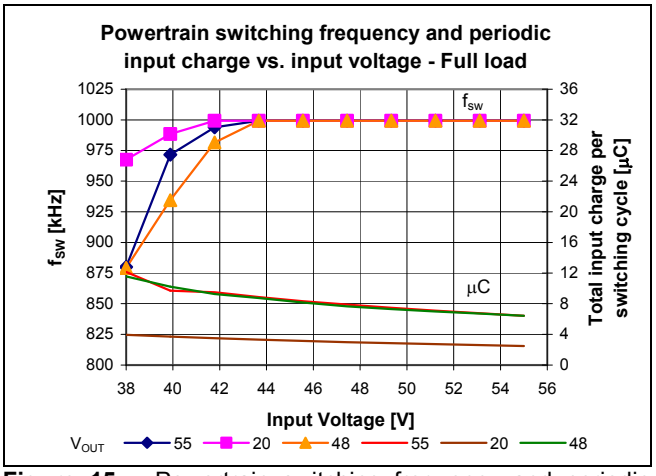


Figure 15 – Powertrain switching frequency and periodic input charge vs. V_{IN}, V_{OUT}; I_{OUT}=8.33A

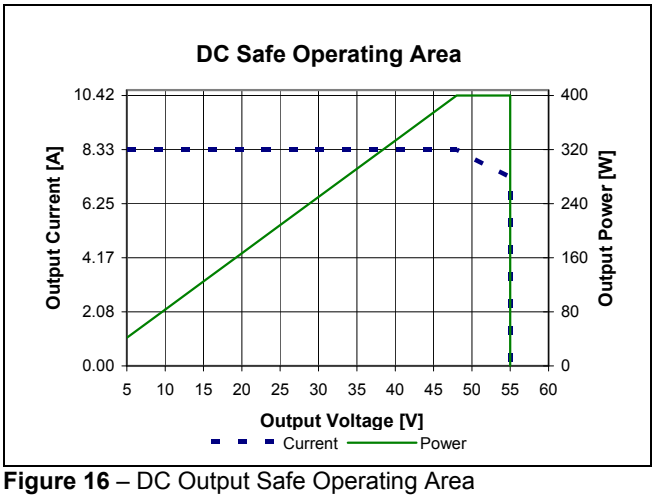


Figure 16 – DC Output Safe Operating Area

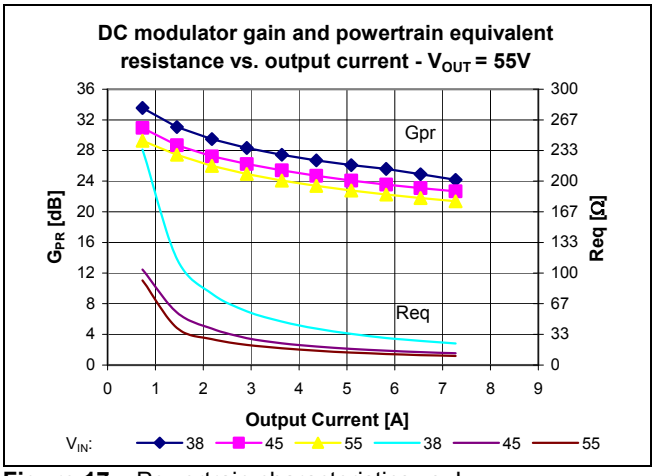


Figure 17 – Powertrain characteristics vs. I_{OUT}; Resistive load, V_{OUT}=55V, various V_{IN}

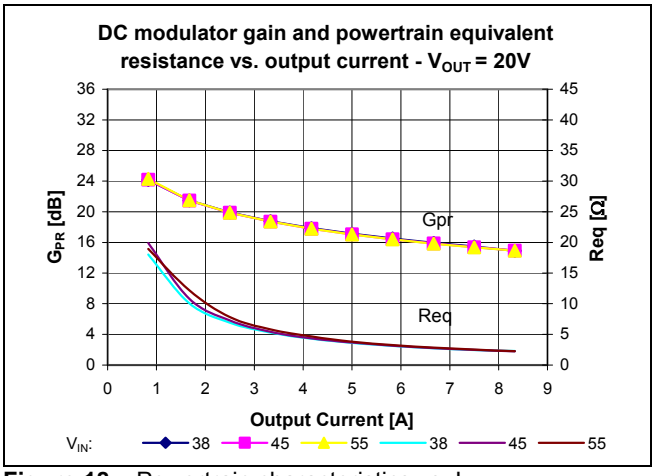


Figure 18 – Powertrain characteristics vs. I_{OUT}; Resistive load, V_{OUT}=20V, various V_{IN}

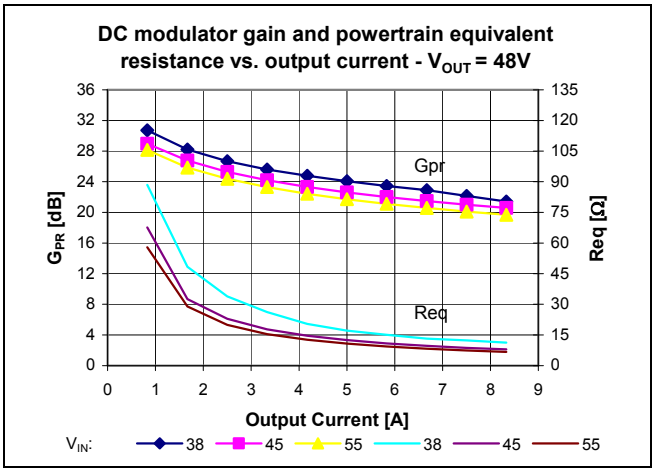


Figure 19 – Powertrain characteristics vs. I_{OUT}; Resistive load, V_{OUT}=48V, various V_{IN}

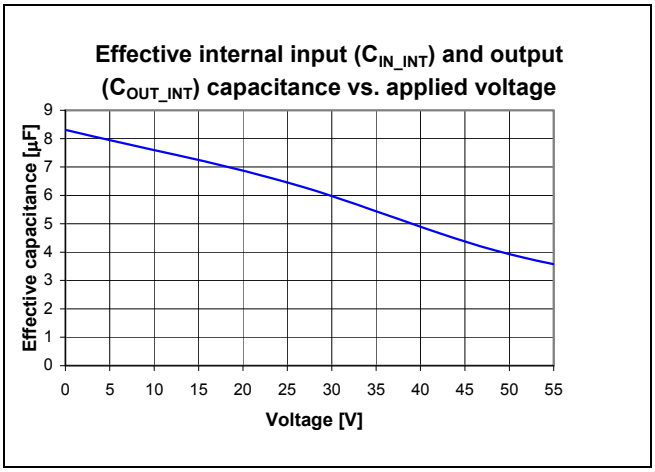


Figure 20 – Effective internal input and output capacitance vs. voltage – ceramic type

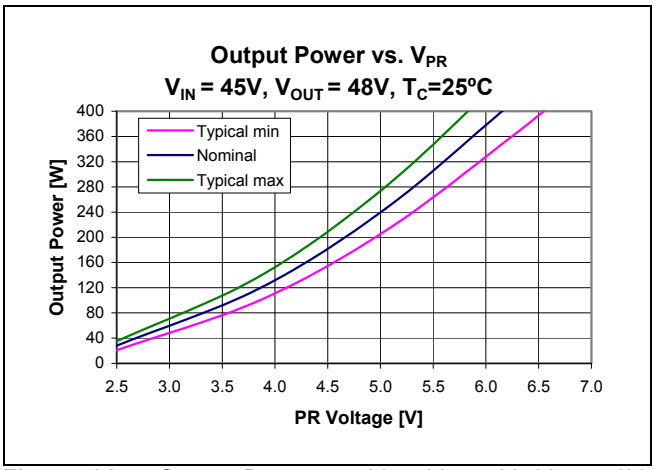


Figure 21 – Output Power vs. V_{PR}; V_{IN}=45V, V_{OUT}=48V, T_{CASE}=25ºC

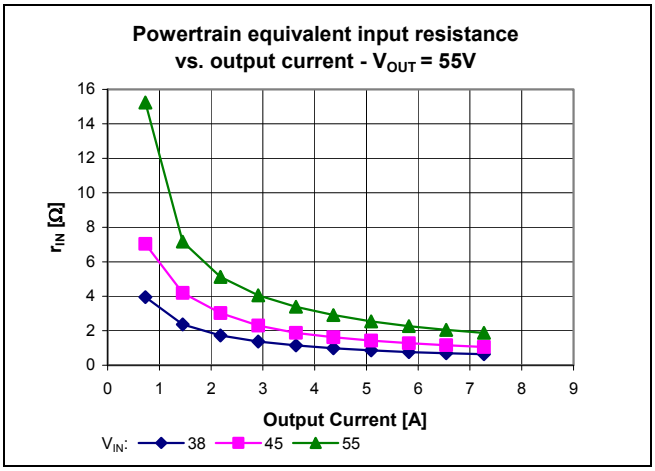


Figure 22 – Magnitude of powertrain dynamic input impedance vs. V_{IN}, I_{OUT}; V_{OUT}=55V

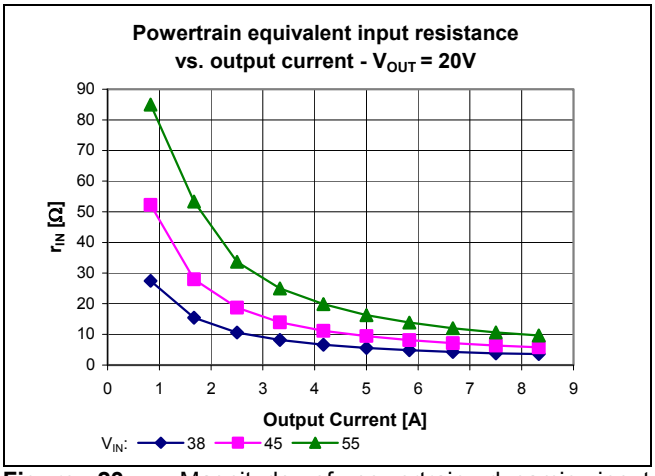


Figure 23 – Magnitude of powertrain dynamic input impedance vs. V_{IN}, I_{OUT}; V_{OUT}=20V

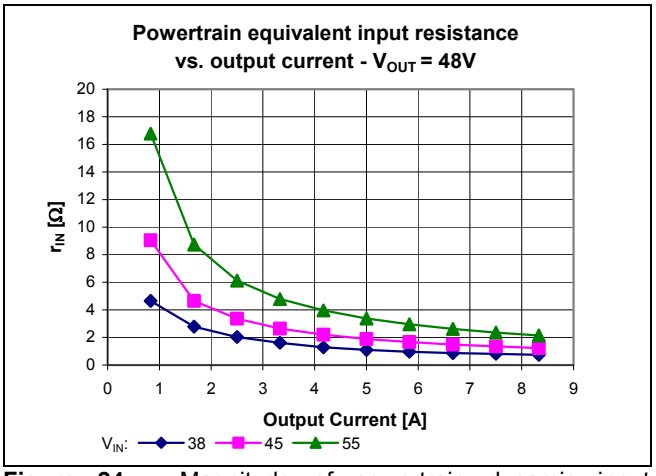


Figure 24 – Magnitude of powertrain dynamic input impedance vs. V_{IN}, I_{OUT}; V_{OUT}=48V

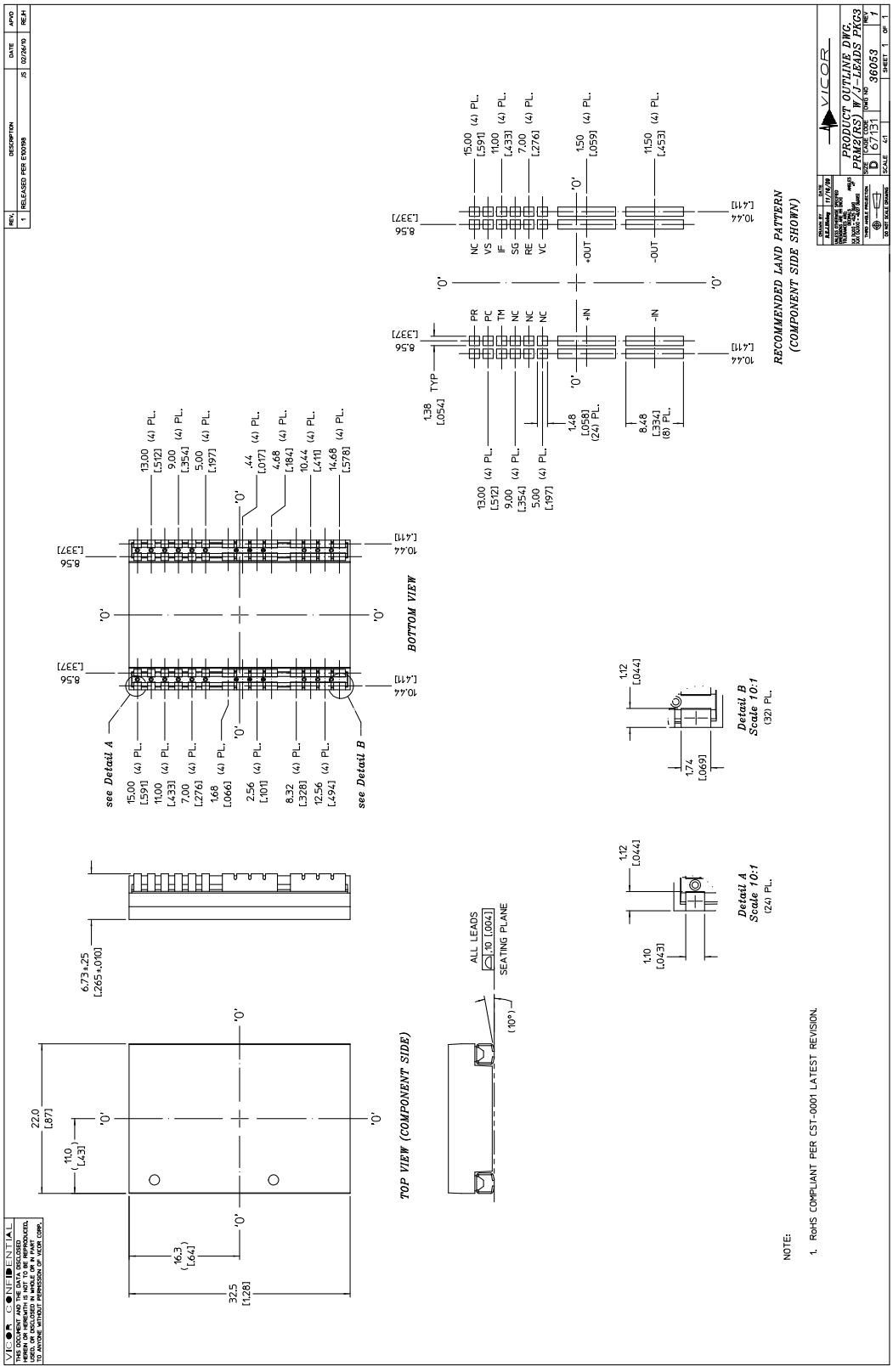
8.0 GENERAL CHARACTERISTICS

Specifications apply over all line and load conditions, T_J = 25 ºC and Output Voltage from 20V to 55V, unless otherwise noted.

Boldface specifications apply over the temperature range of -40 ºC < T_J < 125 ºC (T-grade).

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MECHANICAL						
Length	L		32.3 / [1.27]	32.5 / [1.28]	32.8 / [1.29]	mm / [in]
Width	W		21.8 / [0.86]	22.0 / [0.87]	22.3 / [0.88]	mm / [in]
Height	H		6.60 / [0.26]	6.73 / [0.26]	6.86 / [0.27]	mm / [in]
Volume	Vol	No Heatsink		4.81 / [0.29]		cm^3 / [in^3]
Weight	W			15		g
Lead Finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
THERMAL						
Operating and Storage Junction Temperature	T_J		-40		125	ºC
Operating Case Temperature	T_C		-40		100	ºC
Thermal Capacity				10		Ws/ºC
ASSEMBLY						
Peak Compressive Force Applied to Case (Z-axis)		Supported by J-Lead only			6	lbs
					5.41	lbs / in^2
Storage Temperature	T_{ST}		-40		125	ºC
Moisture Sensitivity Level		MSL 6, four hours out of bag maximum				
		MSL 5				
ESD Rating	ESD_{HBM}	Human Body Model, "JEDEC JESD 22-A114C.01"	1000			V
	ESD_{CDM}	Charged Device Model, "JEDEC JESD 22-C101D"	400			
SOLDERING						
Peak Temperature During Reflow		Under MSL 6 conditions above			245	ºC
		Under MSL 5 conditions above			225	ºC
Maximum Time Above [217] ºC					150	s
Peak Heating Rate During Reflow				1.5	2	ºC / s
Peak Cooling Rate Post Reflow				2.5	3	ºC / s
SAFETY						
MTBF		Telcordia Issue 2 - Method I Case 1; Ground Benign, Controlled		2.29		MHrs
		MIL-HDBK-217Plus Parts Count - 25C Ground Benign, Stationary, Indoors / Computer Profile		3.61		MHrs
Agency Approvals / Standards		$_cTUV_{US}$				
		CE Mark				
		ROHS 6 of 6				

9.0 PRODUCT OUTLINE DRAWING AND RECOMMENDED PCB FOOTPRINT



10.0 PRODUCT DETAILS AND DESIGN GUIDELINES

10.1 Control pins description and characteristics

Control node (PR) is the input to the control node which determines the powertrain timing and ultimately the module output power (Figure 21). An internal 0.5mA current sink is always active. The bi-directional buffer between PR and the control node has two states. In normal operation, PR will be above the 0.79V switching threshold, and will drive the control node through the buffer. An internal 7.4V clamp determines the maximum output power that can be requested of the modulator.
When PR falls below 0.79 V, the converter will stop switching. An internal circuit clamps the modulator input control node to 0.79 V, and a buffer will source up to 2.5 mA out of the pin at that clamp level. For this reason, the output impedance of the amplifier driving PR must be taken into account. A rail-to-rail operational amplifier with low output impedance is always recommended.
The powertrain small signal (plant) response consists of a single pole determined by the load resistance, the powertrain equivalent output resistance, and the total output capacitance (internal and external to the module). Both the modulator gain and the equivalent output resistance vary as a function of line, load and output voltage, as shown in Figures 17, 18 and 19. As the load increases, the powertrain pole moves to higher frequency. As a result, the closed loop crossover frequency will be the highest at full load and lowest at minimum load. Figure 25 shows a reference AC small-signal model.

Current feedback (IF) is the input for the module output overcurrent protection and current limit features (see functional block diagram in section 4.0). A voltage proportional to the powertrain output current must be applied to IF in order for overcurrent protection to operate properly.
If the IF voltage exceeds the IF pin's overcurrent protection threshold, the powertrain will stop switching. If the IF voltage falls below the overcurrent protection threshold within T_{BLANK} time, then the powertrain will immediately resumes switching. Otherwise a fault is latched.
The current limit threshold for the IF pin is set lower than the protection threshold. When the IF pin average voltage exceeds the current limit threshold, an internal integrator will activate a clamp amplifier which overrides the modulator input maximum level. This causes the powertrain to maintain a constant output current.
The bandwidth of this current limit integrator is significantly slower than that of the PR control node input. Therefore this current limit can not be used in lieu of properly compensating the (external) PR control loop to avoid exceeding maximum current or power ratings for the device.
If the IF pin is not driven, it must be resistively terminated to SG. A 1kΩ resistor to SG is recommended in this case.

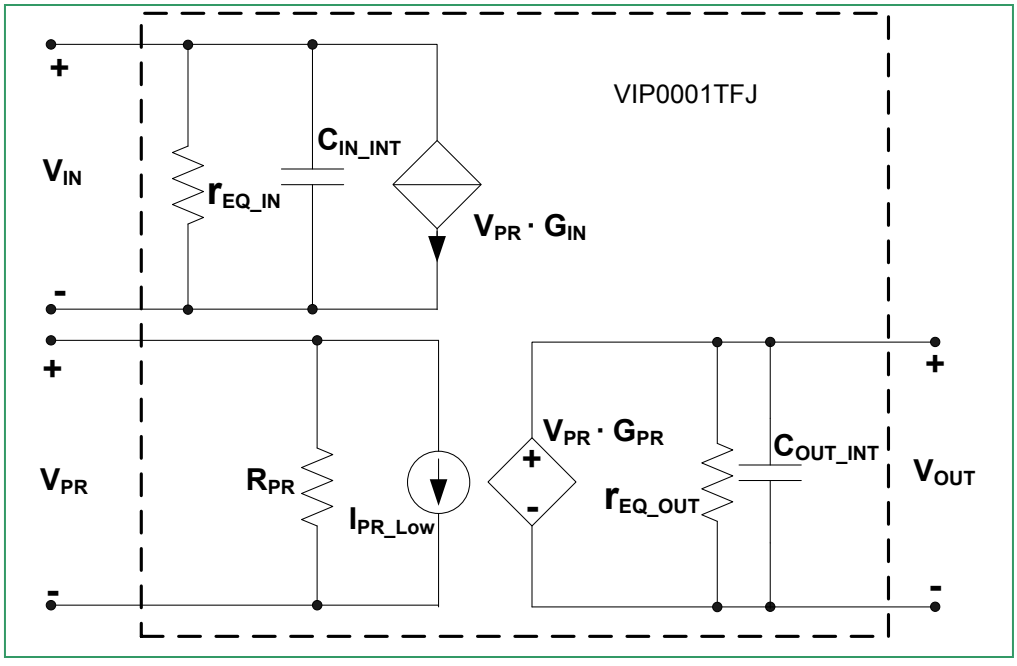


Figure 25 – VIP0001TFJ AC small signal model

VTM Control (VC) pin supplies an initial V_{CC} voltage to downstream VTMs, enabling them and synchronizing their startup with the PRM. The V_{CC} voltage is a pulse, typically 10ms duration at 14V.
If VC is not loaded by a VTM, it must be terminated with a 1kΩ resistor to –VOut.

Primary Control (PC) is both an input and an output. It can provide the following features:
• Delayed start: upon application of voltage (>UVLO) to the module power input and after T_{OFF}, the PC pin will source a constant 90µA current.
• Output disable: PC may be pulled down externally in order to disable the module. Pull down resistance should be less than 300 Ω to SG.
• Fault detection flag: The PC 5 V voltage source is internally turned off when a fault condition is latched. Note that aside from the Short Circuit fault condition, PC does not have significant current sinking capability. Therefore in the case of an array of PRMs with interconnected PC pins, PC does not in general reflect the fault state of all PRMs. The common PC line will not disable neighboring modules when a fault is detected except for a latched Output Short Circuit fault. Conversely any unit in the array latching a Short Circuit fault will disable the array for T_{SCR}.

Temperature Monitor (TM) pin outputs a voltage proportional to the absolute temperature of the converter analog control IC. It can be used to accomplish the following functions:
• Monitor the control IC temperature: The gain and setpoint of TM are such that the temperature, in Kelvin, of the PRM controller IC is equal to the voltage on the TM pin scaled by 100. (i.e. 3.0 V = 300 K = 27ºC).
• Closed loop thermal management at the system level (e.g. variable speed fans or coolant flow)
• Fault detection flag: The TM voltage source is turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of TM.

Reference Enable (RE) pin outputs a regulated 3.3V, 8mA voltage source. It is enabled only after successful startup of the PRM powertrain (see chapters 5.0 and 6.0.) RE is intended to power the output current transducer and also the voltage reference for the control loop. Powering the reference generator with RE helps provide a controlled startup, since the output voltage of the system is able to track the reference level as it comes up.

Voltage Source (VS) pin outputs a gated (e.g. mirrors PC status), non-isolated, regulated 9V, 5mA voltage source. It can be used to power external control circuitry; it always leads RE.

Signal Ground (SG) pin provides a Kelvin connection to the PRM's internal signal ground. It should be used as the reference for PR, TM, IF, and should return all PC, VS and RE pin currents. In array configurations with common ground control circuits, a series resistor (~1Ω) is recommended in order to decouple power and signal current returns.

10.2 Control circuit requirements and design procedure

The VIP0001TFJ is an intelligent powertrain module designed to fully exploit external output voltage feedback and current sensing sub-circuits. These two external circuits are illustrated in Figure 26, which shows an example of the PRM in a standalone application with local voltage feedback and high side current sensing.
In general, these circuits include a precision voltage reference, an operational amplifier which provides closed loop feedback compensation, and a high side current sense circuit which includes a shunt and current sense IC.

The following design procedures refer to the circuit shown in Figure 26.

10.2.1 Setting the output voltage level

The output voltage setpoint is a function of the voltage reference and the output voltage sense ratio. With reference to Fig. 26, R1 and R2 form the output voltage sensing divider which provides the scaled output voltage to the negative input of the error amplifier; a dedicated reference IC provides the reference voltage to the positive input of the error amplifier. Under normal operation, the error amplifier will keep the voltages at the inverting and non-inverting inputs equal, and therefore the output voltage is defined by:

$$V_{OUT} = V_{ref} \cdot \frac{R1 + R2}{R2}$$

Note that the component R1 will also factor into the compensation as described in a later section.

It is important to apply proper slew rate to the reference voltage rise when the control loop is initially enabled. The recommended range for reference rise time is 1 ms to 9 ms. The lower rise time limit will ensure optimized modulator timing performance during startup, and to allow the current limit feature (through IF pin) to fully protect the device during power-up. The upper rise time limit is needed to guarantee a sufficient factorized bus voltage is provided to any downstream VTM input before the end of the VC pulse.

10.2.2 Setting the output current limit and overcurrent protection level

The current limit and overcurrent protection set points are linked, and scale together against the current sense shunt, and the gain of the current sense amplifier. The output of the current sense IC provides the IF voltage which has V_{IF_IL} and V_{IF_OC} thresholds for the two functions respectively. The set points are therefore defined by:

$$I_{IL} = \frac{V_{IF\_IL}}{R_S \cdot G_{CS}}$$

and

$$I_{OC} = \frac{V_{IF\_OC}}{R_S \cdot G_{CS}}$$

where G_{CS} is the gain of the current sense amplifier.

10.2.3 Control loop compensation requirements

In order to properly compensate the control loop, all components which contribute to the closed loop frequency response should be identified and understood. Figure 25 shows the AC small signal model for the module. Modulator DC gain G_{PR} and powertrain equivalent resistance r_{EQ_OUT} are shown. These modeling parameters will support a design cut-off frequency up to 50kHz.
Standard Bode analysis should be used for calculating the error amplifier compensation and analyzing the closed loop stability. The recommended stability criteria are as follows:

1) Phase Margin > 45º : for the closed loop response, the phase should be greater than 45º where the gain crosses 0dB.
2) Gain Margin > 10dB : The closed loop gain should be lower than -10dB where the phase crosses 0º.
3) Gain Slope = -20dB/decade : The closed loop gain should have a slope of -20dB/decade at the crossover frequency.

The compensation characteristics must be selected to meet these stability criteria. Refer to Figure 27 for a local sense, voltage-mode control example based on the configuration in Figure 26. In this example, it is assumed that the maximum crossover frequency (F_{CMAX}) has been selected to occur between B and C. Type-2 compensation (Curve IJKL) is sufficient in this case.
The following data must be gathered in order to proceed:

- Modulator Gain G_{PR}: See Figures 17, 18, 19
- Powertrain equivalent resistance r_{EQ}: See Figures 17, 18, 19
- Internal output capacitance: see Figure 20
- External output capacitance value

In the case of ceramic capacitors, the ESR can be considered low enough to push the associated zero well above the frequency of interest. Applications with high ESR capacitor may require a different type of compensation, or cascade control.
The system poles and zeros of the closed loop can then be defined as follows:

- Powertrain pole, assuming the external capacitor ESR can be neglected:

$$R_{C_{OUT\_EXT}} << \frac{r_{EQ\_OUT} \cdot R_{LOAD}}{r_{EQ\_OUT} + R_{LOAD}}$$

- Main pole frequency:

$$F_P \approx \frac{1}{2\pi \cdot \frac{r_{EQ\_OUT} \cdot R_{LOAD}}{r_{EQ\_OUT} + R_{LOAD}} \cdot \left(C_{OUT\_INT} + C_{OUT\_EXT}\right)}$$

- Compensation Mid-Band Gain:

$$G_{MB} = 20 \log \frac{R_3}{R_1} \qquad [1]$$

- Compensation Zero:

$$F_{Z1} = \frac{1}{2\pi \cdot R_3 \cdot C_1} \qquad [2]$$

- Compensation Pole:

$$F_{P2} = \frac{1}{2\pi \cdot \frac{R_3 \cdot C_1 \cdot C_2}{C_1 + C_2}}$$

and for $F_{P2} >> F_{Z1}$ ($C_1 + C_2 \approx C_1$):

$$F_{P2} \approx \frac{1}{2\pi \cdot R_3 \cdot C_2} \qquad [3]$$

10.2.4 Midband Gain Design (R1,R3):

With reference to Figure 27: curve ABC is the:

- minimum output voltage in the application
- maximum input voltage expected in the application
- maximum load

PRM open loop response, and is where the maximum crossover frequency occurs. In order for the maximum crossover frequency to occur at the design choice F_{CMAX}, the compensation gain must be equal and opposite of the powertrain gain at this frequency. For stability purposes, the compensation should be in the Mid-band (J-K) at the crossover. Using Equation [1], the mid-band gain can be selected appropriately.

10.2.5 Compensation Zero Design (C1):

With reference to Figure 27: curve EFG is the:

- maximum output voltage in the application
- minimum input voltage expected in the application
- minimum load in the application

PRM open loop response, and is where the minimum crossover frequency F_{CMIN} occurs. Based on stability criteria, the compensation must be in the mid-band at the minimum crossover frequency, therefore F_{CMIN} will occur where EFG is equal and opposite of G_{MB}. C1 can be selected using Equation [2] so that F_{Z1} occurs prior to F_{CMIN}.

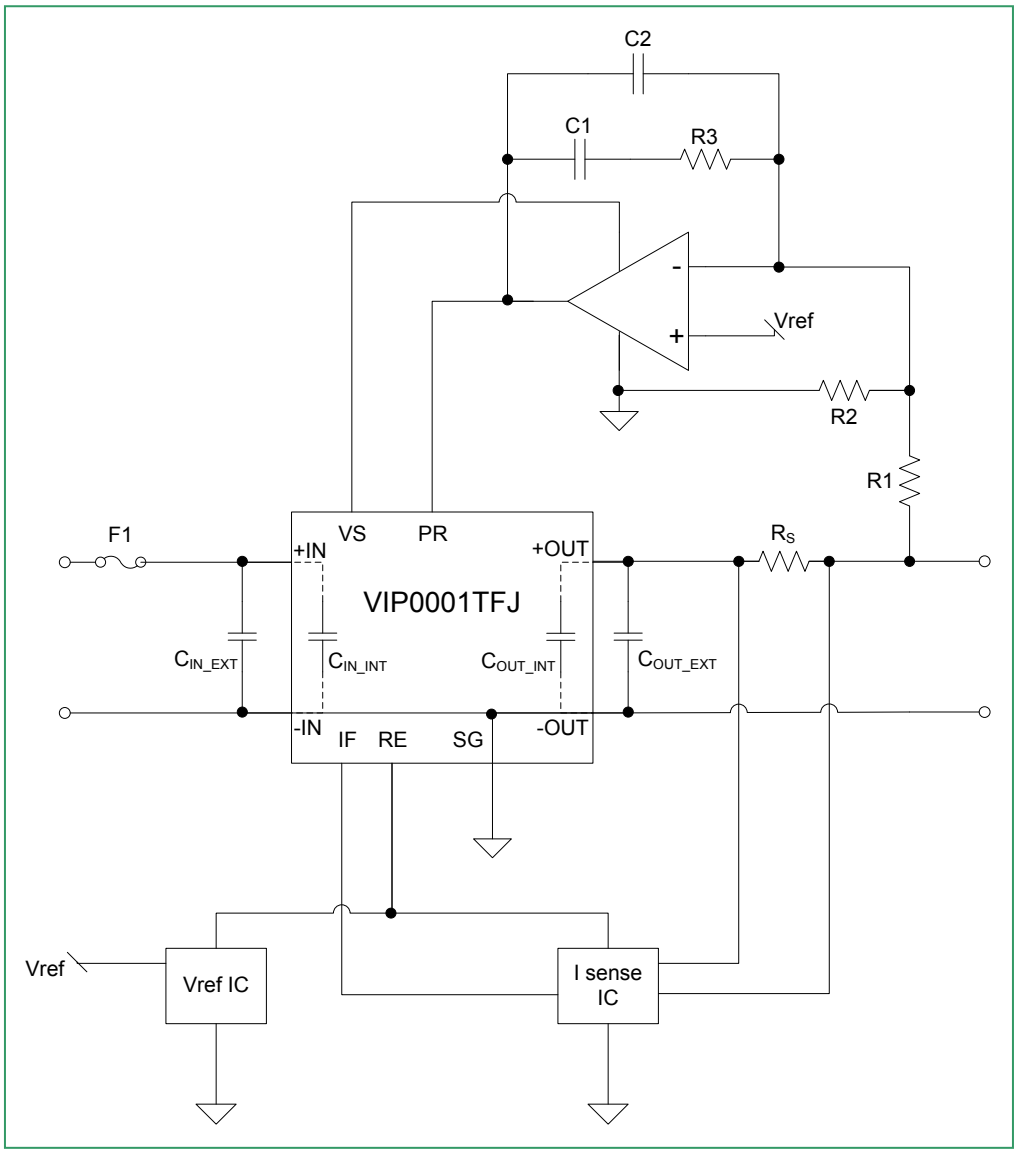


Figure 26 – Control circuit example

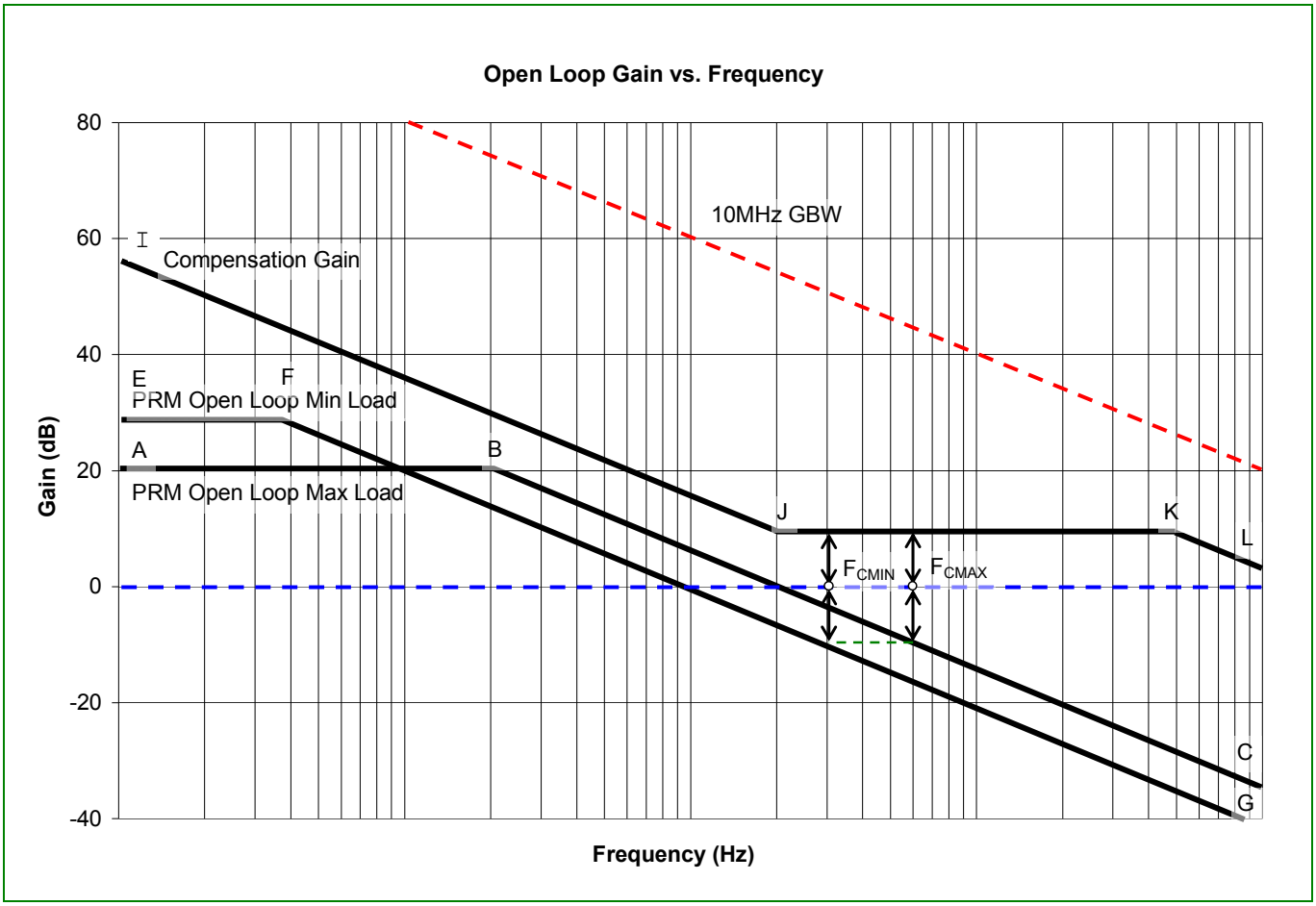


Figure 27 – reference asymptotic Bode plot for the considered system

10.2.6 High Frequency Pole Design (C2):

Using Equation [3], C2 should be selected so that F_{P2} is at least one decade above F_{CMAX} and prior to the gain bandwidth product of the operational amplifier (10MHz for this example). For applications with a higher desired crossover frequency the use of a high gain bandwidth product amplifier may be necessary to ensure that the real pole can be set at least one decade above the maximum crossover frequency.

10.2.7 Verifying Stability:

The preferred method for verifying stability is to use a network analyzer, measuring the closed loop response across various lines and load conditions.
In the absence of a network analyzer, a load step transient response can be used in order to estimate stability.
Figure 28 illustrates an example of a load step response. Equation [4] can be used to predict the phase margin based on the ratio of the "kick" to "droop" (as defined in Fig. 28).

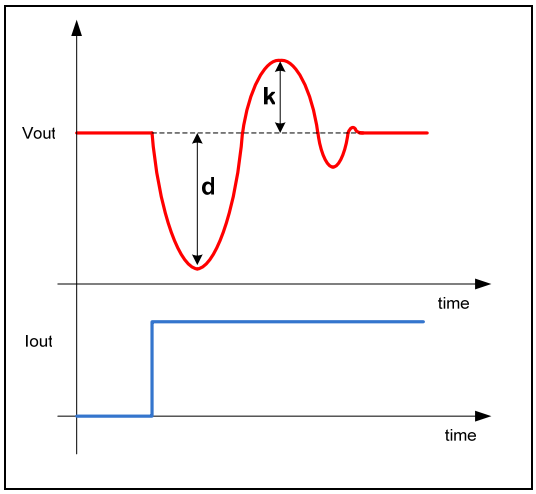


Figure 28 – load step response example and "droop" vs. "kick" definition

$$\Phi_m \approx 100\sqrt{\frac{\left(\ln\frac{k}{d}\right)^2}{\left(\ln\frac{k}{d}\right)^2+\pi^2}} \qquad [4]$$

10.3 Burst Mode Operation:

At light loads, the PRM will operate in a burst mode due to minimum timing constraints. An example burst operation waveform is illustrated in Figure 29.
For very light loads, and also for higher input voltages, the minimum time power switching cycle from the powertrain will exceed the power required by the load. In this case the external error amplifier will periodically drive PR below the switching threshold in order to maintain regulation. Switching will cease momentarily until the error amplifier once again drives PR voltage above the threshold.

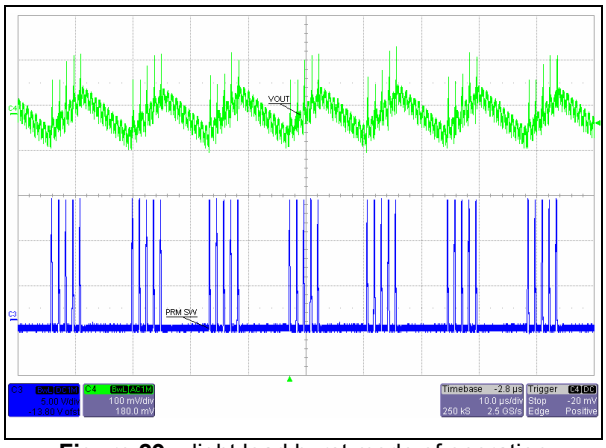


Figure 29 – light load burst mode of operation

Note that during the bursts of switching, the powertrain frequency is constant, but the number of pulses as well as the time between bursts is variable. The variability depends on many factors including input voltage, output voltages, load impedance, and external error amplifier output impedance.
In burst mode, the gain of the PR input to the plant which is modeled in the previous sections is time varying. Therefore the small signal analysis can not be directly applied to burst mode operation.

10.4 Input and Output filter design

Figures 14 and 15 provide the total input and output charge per cycle, as well as switching frequency, of the PRM at full load under various input and output voltages conditions.

Figure 20 provides the effective internal capacitance of the module. A conservative estimate of input and output peak-peak voltage ripple at nominal line and trim is provided by equation [5]:

$$\Delta V = \frac{Q_{TOT} - \frac{I_{FL}\cdot 0.4}{f_{SW}}}{C_{INT}+C_{EXT}} \qquad [5]$$

Q_{TOT} is the total input (Fig. 15) or output (Fig. 14) charge per switching cycle at full load, while C_{INT} is the module internal effective capacitance at the considered voltage (Fig. 20) and C_{EXT} is the external effective capacitance at the considered voltage.

10.5 Input filter stability

The PRM can provide very high dynamic transients. It is therefore very important to verify that the voltage supply source as well as the interconnecting line are stable and do not oscillate. For this purpose, the converter dynamic input impedance magnitude $\left|r_{EQ\_IN}\right|$ is provided in Figures 22, 23, 24. It is recommended to provide adequate design margin with respect to the stability conditions illustrated in 10.5.1 and 10.5.2 .

10.5.1 Inductive source and local, external input decoupling capacitance with negligible ESR (i.e.: ceramic type)

The voltage source impedance can be modeled as a series $R_{line}L_{line}$ circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{line} > \frac{L_{line}}{(C_{IN\_INT}+C_{IN\_EXT})\cdot\left|r_{EQ\_IN}\right|} \qquad [6]$$

$$R_{line} << \left|r_{EQ\_IN}\right| \qquad [7]$$

It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, [7]. However, R_S cannot be made arbitrarily low otherwise equation [6] is violated and the system will show instability, due to under-damped RLC input network.

10.5.2 Inductive source and local, external input decoupling capacitance with significant R_{CIN_EXT} ESR (i.e.: electrolytic type)

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor L_{line}. Notice that, the high performance ceramic capacitors C_{IN_INT} within the PRM should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be

$$\left|r_{EQ\_IN}\right| > R_{C_{IN\_EXT}} \qquad [8]$$

$$\frac{L_{line}}{C_{IN\_EXT} \cdot R_{C_{IN\_EXT}}} < \left|r_{EQ\_IN}\right| \qquad [9]$$

Equation [9] shows that if the aggregate ESR is too small – for example by using very high quality input capacitors (C_{IN_EXT}) – the system will be under-damped and may even become destabilized. Again, an octave of design margin in satisfying [8] should be considered the minimum.

10.6 Arrays

Up to ten PRMs of the same type may be placed in parallel to expand the power capacity of the system. The following high-level guidelines must be followed in order for the resultant system to start up and operate properly, and to avoid overstress or exceeding any absolute maximum ratings.

- –IN pins of all PRMs must be connected together. Both inductance and resistance from the common power source to each PRM should be minimized, and matched.
- Input voltage to all PRMs must be the same. Independent fuses for each PRM are recommended.
- PC pins must be connected together for synchronization and proper fault response.
- Reference supply to the control loop voltage reference and current sense circuitry must be enabled when all modules' RE pins have reached their operational voltage levels.
- There must be one single external voltage control loop. The control loop must drive each PR pin relative to each modules' SG pin, and the local PR voltage must be the same across all modules.
- Each PRM must have its own local current shunt and current sense circuitry to drive it's IF pin.
- The number of PRMs required to achieve a given array capacity must consider all sources of mismatch to avoid overstress of any PRM in the array. Imbalances in sharing are not only due to current sharing accuracy specifications, but also temperature differences among PRMs, Vin variations, and error terms in the buffering of the error amplifier output to the PR pins.
- Control loop compensation procedures above will hold for an array, in general, although many parameters must be scaled against the number of PRMs in the system.

Please contact Vicor Applications for assistance.

10.7 Input Fuse Recommendations

A fuse should be incorporated at the input to each PRM, in series with the +IN pin. A 15A or smaller input fuse (Littelfuse® NANO²® 451/453 Series, or equivalent) is required to safety agency conditions of acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application.

10.8 Layout considerations

Application Note AN:005 details board layout using V•I Chip components. Additional consideration must be given to the external control circuit components.

The current sense shunt signal voltage is highly sensitive to noise. As such, current sensing circuitry should be located close to the shunt to minimize the length of the sense signals. A Kelvined connection at the shunt is recommended for best results.

The control signal from a remote voltage sense circuit to the PRM should be shielded. Avoid routing this, or other control signals directly underneath the PRM, if possible. Components that tie directly to the PRM should be located close to their respective pins. It is also critical that all control components be referenced to SG, and that SG not be tied to any other ground in the system, including –IN or –OUT of the PRM.

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Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com