

Not recommended for New Designs  
Replaced by [VTM48EF012T130A00](#)



## VTM™ Transformer

### FEATURES

- 40 Vdc to 1 Vdc 130 A transformer
  - Operating from standard 48 V or 24 V PRM™ regulators
- 150 A rated with reduced case temperature at 30°C
- High efficiency (>91%) reduces system power consumption
- High density (117 A/in<sup>2</sup>)
- “Full Chip” V•I Chip package enables surface mount, low impedance interconnect to system board
- Contains built-in protection features:
  - Overvoltage Lockout
  - Overcurrent
  - Short Circuit
  - Over Temperature
- Provides enable / disable control, internal temperature monitoring, current monitoring
- ZVS / ZCS resonant Sine Amplitude Converter topology
- Less than 50°C temperature rise at full load in typical applications

### TYPICAL APPLICATION

- High End Computing Systems
- Automated Test Equipment
- High Density Power Supplies

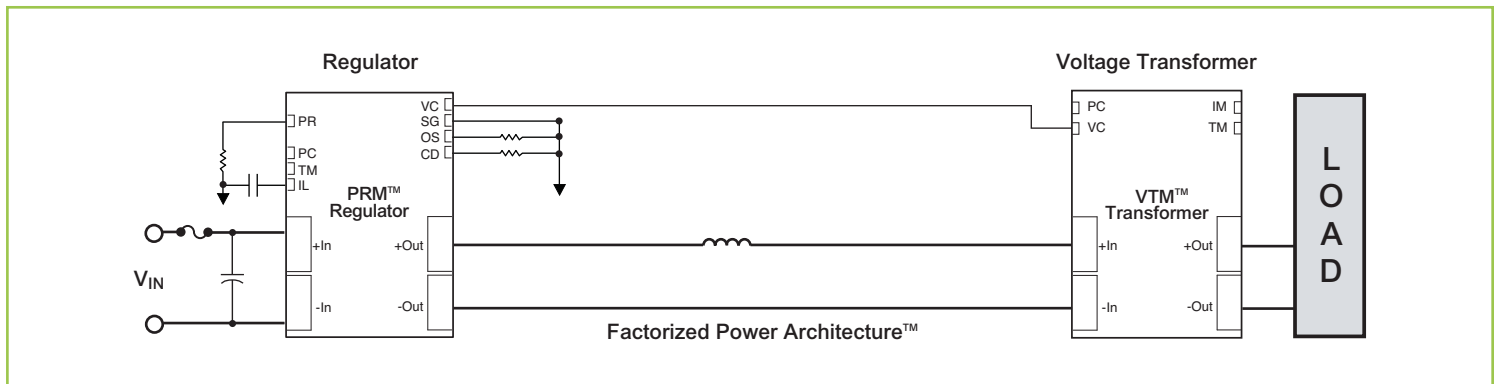
### DESCRIPTION

The V•I Chip™ transformer is a high efficiency (>91%) Sine Amplitude Converter™ (SAC™) operating from a 26 to 55 Vdc primary bus to deliver an isolated output. The Sine Amplitude Converter offers a low AC impedance beyond the bandwidth of most downstream regulators; therefore capacitance normally at the load can be located at the input to the Sine Amplitude Converter. Since the K factor of the VIV0005TFJ is 1/40, the capacitance value can be reduced by a factor of 1600, resulting in savings of board area, materials and total system cost.

The VIV0005TFJ is provided in a V•I Chip package compatible with standard pick-and-place and surface mount assembly processes. The co-molded V•I Chip package provides enhanced thermal management due to a large thermal interface area and superior thermal conductivity. The high conversion efficiency of the VIV0005TFJ increases overall system efficiency and lowers operating costs compared to conventional approaches. The VIV0005TFJ enables the utilization of Factorized Power Architecture™ which provides efficiency and size benefits by lowering conversion and distribution losses and promoting high density point of load conversion.

$V_{IN} = 26 \text{ to } 55 \text{ V}$	$I_{OUT} = 130 \text{ A}_{(NOM)}$
$V_{OUT} = 0.65 \text{ to } 1.37 \text{ V}_{(NO \text{ LOAD})}$	$K = 1/40$

PART NUMBER	DESCRIPTION
VIV0005TFJ	-40°C to 125°C T <sub>J</sub>



# VIV0005TFJ

## 1.0 ABSOLUTE MAXIMUM VOLTAGE RATINGS

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

	MIN	MAX	UNIT		MIN	MAX	UNIT
+ IN to - IN	-1	60	V <sub>DC</sub>	IM to - IN	0	3.15	V <sub>DC</sub>
PC to - IN	-0.3	20	V <sub>DC</sub>	+ IN / - IN to + OUT / - OUT (hipot)		100	V <sub>DC</sub>
TM to -IN	-0.3	7	V <sub>DC</sub>	+ IN / - IN to + OUT / - OUT (working)		60	V <sub>DC</sub>
VC to - IN	-0.3	20	V <sub>DC</sub>	+ OUT to - OUT	-1	5.5	V <sub>DC</sub>

## 2.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T<sub>J</sub> < 125°C (T-Grade)**; All other specifications are at **T<sub>J</sub> = 25°C** unless otherwise noted.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
Input voltage range	V <sub>IN</sub>	No external VC applied	<b>26</b>		<b>55</b>	V <sub>DC</sub>
		VC applied	<b>0</b>		<b>55</b>	
V <sub>IN</sub> slew rate	dV <sub>IN</sub> /dt				<b>1</b>	V/μs
V <sub>IN</sub> UV turn off	V <sub>IN_UV</sub>	Module latched shutdown, No external VC applied, I <sub>OUT</sub> = 130A		18	<b>26</b>	V
No load power dissipation	P <sub>NL</sub>	V <sub>IN</sub> = 40 V	<b>2</b>		<b>6.3</b>	W
		V <sub>IN</sub> = 26 V to 55 V			<b>7.5</b>	
		V <sub>IN</sub> = 40 V, T <sub>C</sub> = 25°C		3.2	4.5	
		V <sub>IN</sub> = 26 V to 55 V, T <sub>C</sub> = 25°C			6	
DC input current	I <sub>IN_DC</sub>				<b>4</b>	A
Transfer ratio	K	K = V <sub>OUT</sub> /V <sub>IN</sub> , I <sub>OUT</sub> = 0 A		<b>1/40</b>		V/V
Output voltage	V <sub>OUT</sub>	V <sub>OUT</sub> = V <sub>IN</sub> • K - I <sub>OUT</sub> • R <sub>OUT</sub> , Section 11				V
Output current (average)	I <sub>OUT_AVG</sub>	30°C < T <sub>C</sub> < 100°C, I <sub>out_max</sub> = - (2/7) • T <sub>C</sub> + 159			<b>130</b>	A
		T <sub>C</sub> = 30°C			150	
Output current (peak)	I <sub>OUT_PK</sub>	T <sub>PEAK</sub> < 10 ms, I <sub>OUT_AVG</sub> ≤ 130 A			<b>195</b>	A
Output power (average)	P <sub>OUT_AVG</sub>	I <sub>OUT_AVG</sub> ≤ 130 A			<b>178</b>	W
Efficiency (ambient)	η <sub>AMB</sub>	V <sub>IN</sub> = 40 V, I <sub>OUT</sub> = 130 A	87.5	89.2		%
		V <sub>IN</sub> = 26 V to 55 V, I <sub>OUT</sub> = 130 A	81.7			
		V <sub>IN</sub> = 40 V, I <sub>OUT</sub> = 65 A	89.1	91		
		V <sub>IN</sub> = 40 V, I <sub>OUT</sub> = 150 A	86.2	88.2		
Efficiency (hot)	η <sub>HOT</sub>	V <sub>IN</sub> = 40 V, T <sub>C</sub> = 100°C, I <sub>OUT</sub> = 130 A	85.1	87.5		%
Efficiency (over load range)	η <sub>20%</sub>	26 A < I <sub>OUT</sub> < 130 A	<b>78</b>			%
Output resistance (cold)	R <sub>OUT_COLD</sub>	T <sub>C</sub> = -40°C, I <sub>OUT</sub> = 130 A	0.45	0.575	0.75	mΩ
Output resistance (ambient)	R <sub>OUT_AMB</sub>	T <sub>C</sub> = 25°C, I <sub>OUT</sub> = 130 A	0.55	0.668	0.87	mΩ
Output resistance (hot)	R <sub>OUT_HOT</sub>	T <sub>C</sub> = 100°C, I <sub>OUT</sub> = 130 A	0.7	0.82	1.02	mΩ
Switching frequency	F <sub>SW</sub>		<b>1.53</b>	1.61	<b>1.67</b>	MHz
Output ripple frequency	F <sub>SW_RP</sub>		<b>3.06</b>	3.22	<b>3.34</b>	MHz
Output voltage ripple	V <sub>OUT_PP</sub>	C <sub>OUT</sub> = 0 F, I <sub>OUT</sub> = 130 A, V <sub>IN</sub> = 40 V, 20 MHz BW, Section 12		125	<b>150</b>	mV
Output inductance (parasitic)	L <sub>OUT_PAR</sub>	Frequency up to 30 MHz, Simulated J-lead model		150		pH
Output capacitance (internal)	C <sub>OUT_INT</sub>			360		μF
<b>PROTECTION</b>						
Overvoltage lockout	V <sub>IN_OVLO+</sub>	Module latched shutdown	55.01	57.5	59.99	V
Overvoltage lockout response time	T <sub>OVLO</sub>	Effective internal RC filter		0.24		μs
Output overcurrent trip	I <sub>OC</sub>		165	200	275	A
Short circuit protection trip current	I <sub>SCP</sub>		275			A
Output overcurrent response time constant	T <sub>OC</sub>	Effective internal RC filter (Integrative).		7.13		ms
Short circuit protection response time	T <sub>SCP</sub>	From detection to cessation of switching (Instantaneous)		2		μs
Thermal shutdown setpoint	T <sub>J_OTP</sub>		125	130	135	°C

# VIV0005TFJ

## 3.0 SIGNAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$  (T-Grade); All other specifications are at  $T_J = 25^{\circ}\text{C}$  unless otherwise noted.

### VTM CONTROL : VC

- Used to wake up powertrain circuit.
- A minimum of 11.5 V must be applied indefinitely for  $V_{IN} < 26$  V to ensure normal operation.
- VC slew rate must be within range for a successful start.
- PRM VC can be used as valid wake-up signal source.
- VC voltage may be continuously applied; there will be no VC current drawn when  $V_{IN} > 26$  V.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Steady	External VC voltage	$V_{VC\_EXT}$	Required for start up, and operation below 26 V. See Section 7.	<b>11.5</b>		<b>16.5</b>	V
		VC current draw	$I_{VC}$	VC = 11.5 V, $V_{IN} = 0$ V VC = 11.5 V, $V_{IN} > 26$ V Fault mode. VC > 11.5 V	<b>0</b>	100	<b>150</b>	mA
	Start Up	VC slew rate	dVC/dt	Required for proper start up; $0^{\circ}\text{C} < T_C < 100^{\circ}\text{C}$	<b>0.001</b>		<b>0.25</b>	V/ $\mu\text{s}$
		VC inrush current	$I_{INR\_VC}$	Required for proper start up; $-40^{\circ}\text{C} < T_C < 100^{\circ}\text{C}$ VC = 16.5 V, dVC/dt = 0.25 V/ $\mu\text{s}$	<b>0.0025</b>		<b>0.25</b>	V/ $\mu\text{s}$
	Transitional	VC to PC delay	$T_{VC\_PC}$	VC = 11.5 V to PC high, $V_{IN} = 0$ V, dVC/dt = 0.25 V/ $\mu\text{s}$		75	<b>125</b>	$\mu\text{s}$
		Internal VC capacitance	$C_{VC\_INT}$	VC = 0 V		1		$\mu\text{F}$

### PRIMARY CONTROL : PC

- The PC pin enables and disables the VTM. When held below 2.0 V, the VTM will be disabled.
- PC pin outputs 5 V during normal operation. PC pin is equal to 2.5 V during fault mode given  $V_{IN} > 26$  V and VC > 11.5 V.
- After successful start up and under no fault condition, PC can be used as a 5 V regulated voltage source with a 2 mA maximum current.
- Module will shutdown when pulled low with an impedance less than 850  $\Omega$ .
- In an array of VTMs, connect PC pin to synchronize start up.
- PC pin can't sink current and will not disable other modules during fault mode.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	PC voltage	$V_{PC}$		<b>4.7</b>	<b>5</b>	<b>5.3</b>	V
		PC source current	$I_{PC\_OP}$				<b>2</b>	mA
		PC resistance (internal)	$R_{PC\_INT}$	Internal pull down resistor	<b>50</b>	150	<b>400</b>	k $\Omega$
	Start Up	PC source current	$I_{PC\_EN}$		<b>50</b>	100	<b>300</b>	$\mu\text{A}$
		PC capacitance (internal)	$C_{PC\_INT}$	Section 7			<b>1000</b>	pF
DIGITAL INPUT / OUPUT	Enable	PC resistance (external)	$R_{PC\_EXT}$		<b>60</b>			k $\Omega$
		PC voltage	$V_{PC\_EN}$		<b>2</b>	2.5	<b>3</b>	V
	Disable	PC voltage (disable)	$V_{PC\_DIS}$				<b>2</b>	V
		PC pull down current	$I_{PC\_PD}$		<b>5.1</b>			mA
	Transitional	PC disable time	$T_{PC\_DIS\_T}$			5		$\mu\text{s}$
		PC fault response time	$T_{FR\_PC}$	From fault to PC = 2.0 V		100		$\mu\text{s}$

### TEMPERATURE MONITOR : TM

- The TM pin monitors the internal temperature of the VTM controller IC within an accuracy of  $\pm 5^{\circ}\text{C}$ .
- Can be used as a "Power Good" flag to verify that the VTM is operating.
- The TM pin has a room temperature setpoint of 3 V and approximate gain of 10 mV/ $^{\circ}\text{C}$ .

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	TM voltage	$V_{TM\_AMB}$	$T_J$ controller = $27^{\circ}\text{C}$	2.95	3	3.05	V
		TM source current	$I_{TM}$				<b>100</b>	$\mu\text{A}$
		TM gain	$A_{TM}$			10		mV/ $^{\circ}\text{C}$
		TM voltage ripple	$V_{TM\_PP}$	$C_{TM} = 0$ F, $V_{IN} = 40$ V, $I_{OUT} = 130$ A		120	<b>200</b>	mV
DIGITAL OUTPUT (FAULT FLAG)	Disable	TM voltage	$V_{TM\_DIS}$			0		V
	Transitional	TM resistance (internal)	$R_{TM\_INT}$	Internal pull down resistor	<b>25</b>	40	<b>50</b>	k $\Omega$
		TM capacitance (external)	$C_{TM\_EXT}$				<b>50</b>	pF
		TM fault response time	$T_{FR\_TM}$	From fault to TM = 1.5 V		10		$\mu\text{s}$

# VIV0005TFJ

## 3.0 SIGNAL CHARACTERISTICS (CONT.)

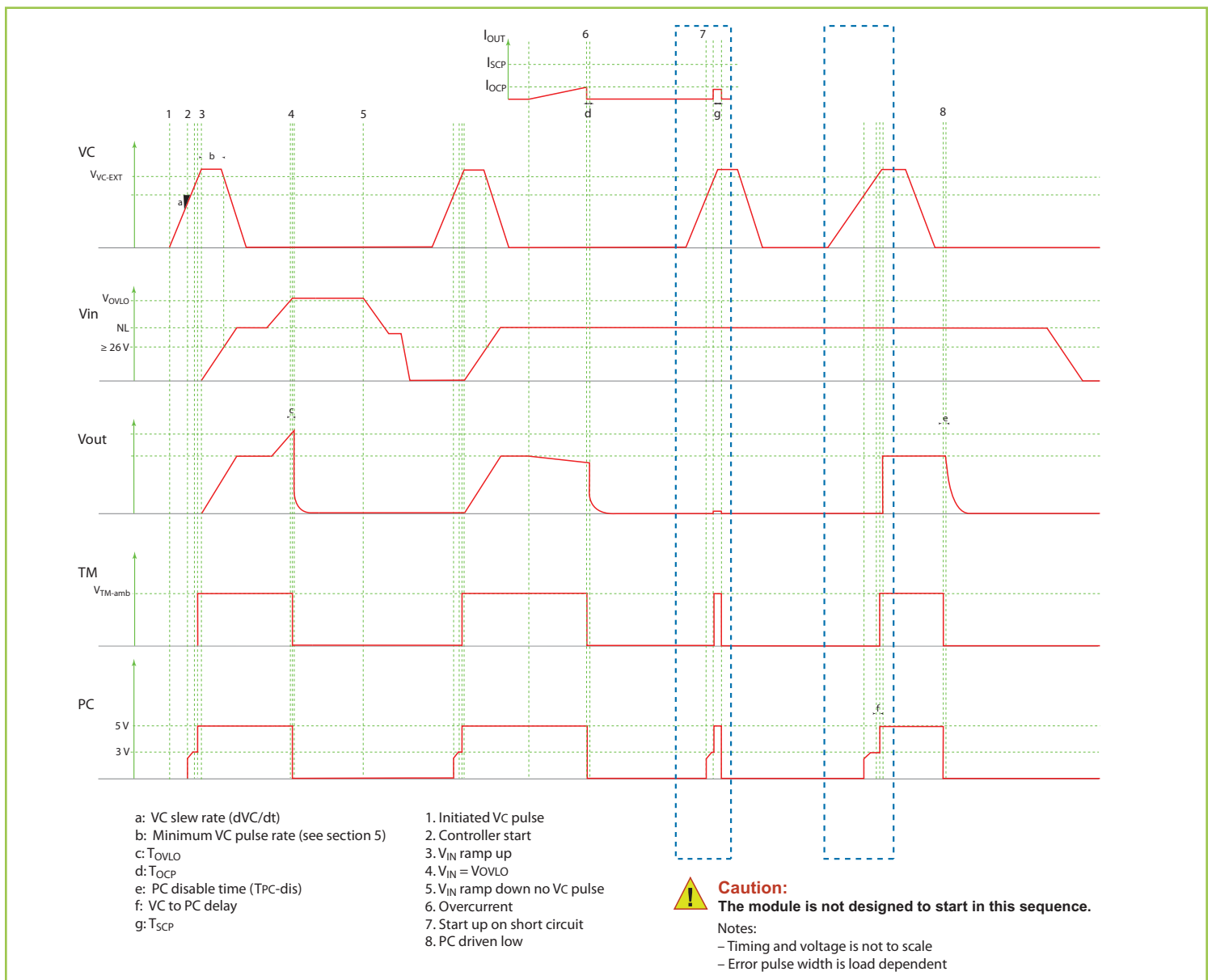
Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$  (T-Grade); All other specifications are at  $T_J = 25^{\circ}\text{C}$  unless otherwise noted.

### CURRENT MONITOR : IM

- The IM pin voltage varies between 0.1 V and 1.825 V representing the output current within  $\pm 25\%$  under all operating line temperature conditions between 50% and 100%.
- The IM pin provides a DC analog voltage proportional to the output current of the VTM.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	IM voltage (no load)	$V_{IM\_NL}$	$T_J = 25^{\circ}\text{C}, V_{IN} = 40\text{ V}, I_{OUT} = 0\text{ A}$	0.1	0.206	0.4	V
		IM voltage (50%)	$V_{IM\_50\%}$	$T_J = 25^{\circ}\text{C}, V_{IN} = 40\text{ V}, I_{OUT} = 65\text{ A}$		0.857		V
		IM voltage (full load)	$V_{IM\_FL}$	$T_J = 25^{\circ}\text{C}, V_{IN} = 40\text{ V}, I_{OUT} = 130\text{ A}$		1.825		V
		IM gain	$A_{IM}$	$T_J = 25^{\circ}\text{C}, V_{IN} = 40\text{ V}, I_{OUT} > 65\text{ A}$		14.9		mV/A
		IM resistance (external)	$R_{IM\_EXT}$		<b>3</b>			MΩ

## 4.0 TIMING DIAGRAM



## 5.0 APPLICATION CHARACTERISTICS

The following values, typical of an application environment, are collected at  $T_J = 25^\circ\text{C}$  unless otherwise noted. See associated figures for general trend data.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	TYP	UNIT
No load power dissipation	$P_{NL}$	$V_{IN} = 42\text{ V}$ , PC enabled	3.2	W
Efficiency (ambient)	$\eta_{AMB}$	$V_{IN} = 42\text{ V}$ , $I_{OUT} = 130\text{ A}$	89.5	%
Efficiency (hot)	$\eta_{HOT}$	$V_{IN} = 42\text{ V}$ , $I_{OUT} = 130\text{ A}$	88	%
Output resistance (ambient)	$R_{OUT\_AMB}$	$V_{IN} = 42\text{ V}$	0.69	$\text{m}\Omega$
Output resistance (hot)	$R_{OUT\_HOT}$	$V_{IN} = 42\text{ V}$	0.85	$\text{m}\Omega$
Output resistance (cold)	$R_{OUT\_COLD}$	$V_{IN} = 42\text{ V}$	0.6	$\text{m}\Omega$
Output voltage ripple	$V_{OUT\_PP}$	$C_{OUT} = 0\text{ F}$ , $I_{OUT} = 130\text{ A}$ , $V_{IN} = 40\text{ V}$ , 20 MHz BW, Section 12	116	mV
$V_{OUT}$ transient (positive)	$V_{OUT\_TRAN+}$	$I_{OUT\_STEP} = 0\text{ A TO }150\text{ A}$ , $V_{IN} = 40\text{ V}$ , $I_{SLEW} > 10\text{ A/us}$	90	mV
$V_{OUT}$ transient (negative)	$V_{OUT\_TRAN-}$	$I_{OUT\_STEP} = 150\text{ A TO }0\text{ A}$ , $V_{IN} = 40\text{ V}$ , $I_{SLEW} > 10\text{ A/us}$	100	mV

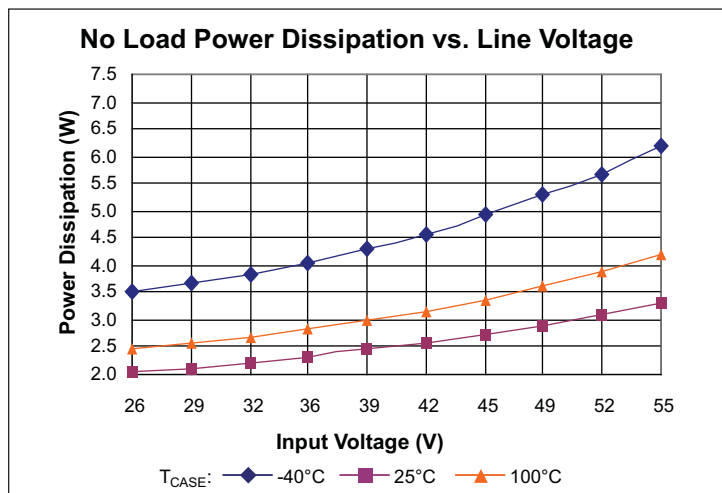


Figure 1 – No load power dissipation vs.  $V_{IN}$

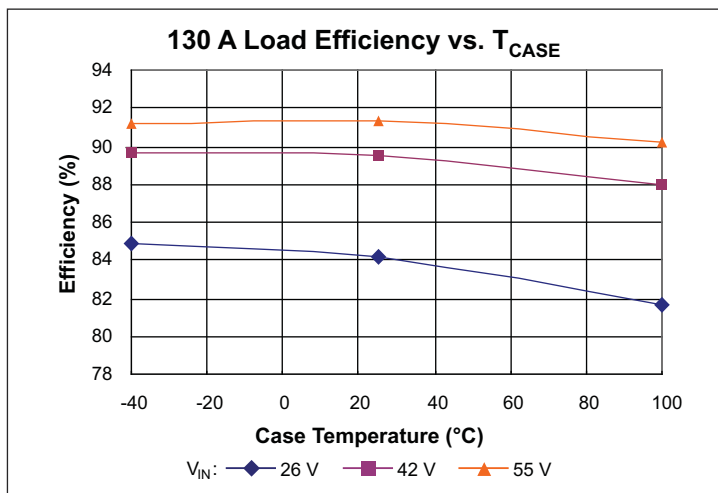


Figure 2 – Full load efficiency vs. temperature

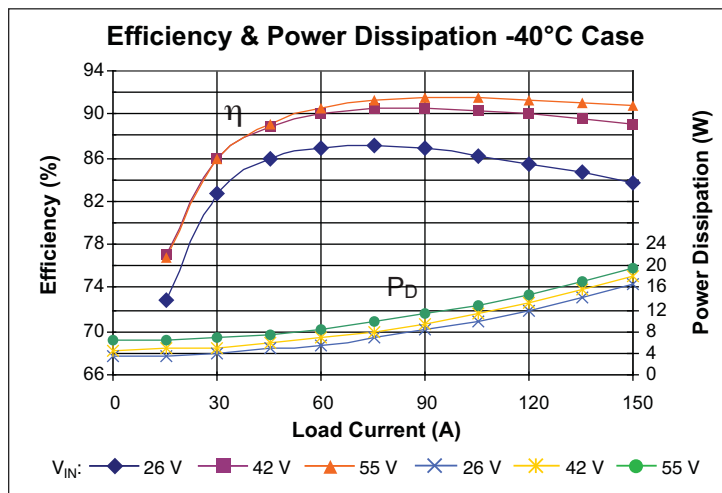


Figure 3 – Efficiency and power dissipation at  $-40^\circ\text{C}$

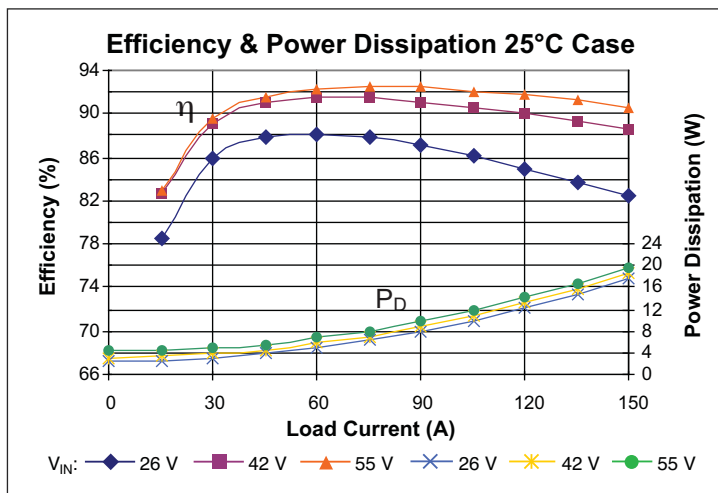


Figure 4 – Efficiency and power dissipation at  $25^\circ\text{C}$

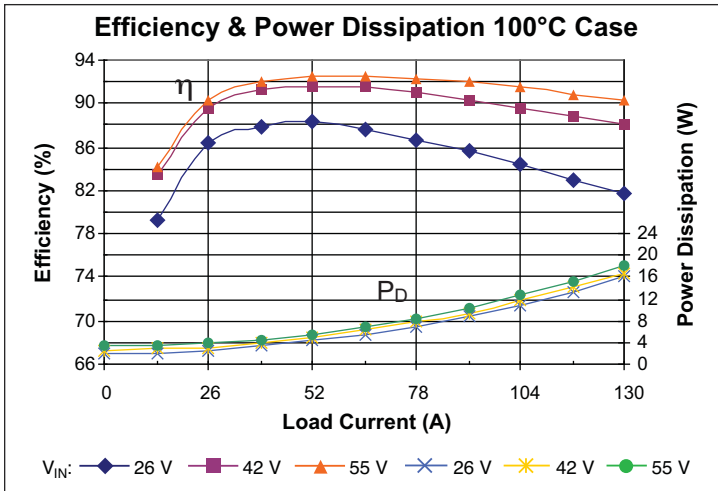


Figure 5 – Efficiency and power dissipation at 100°C

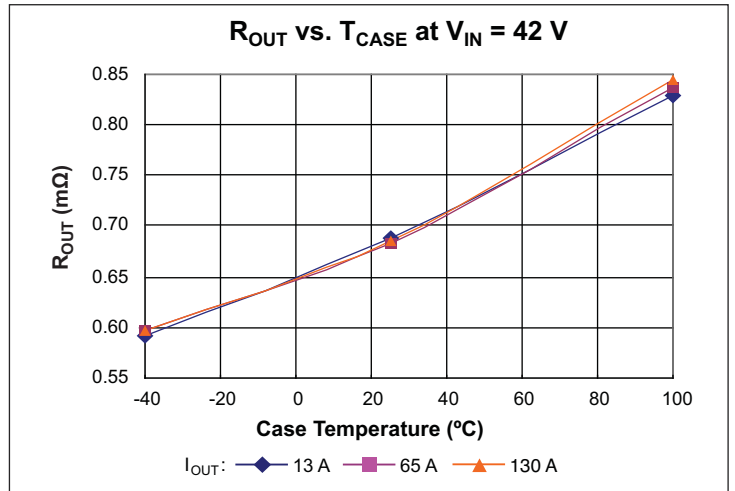


Figure 6 – R<sub>OUT</sub> vs. temperature

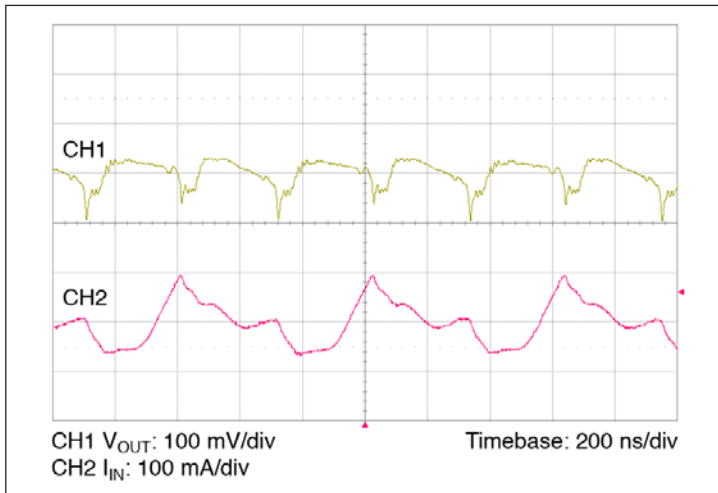


Figure 7 – Full load ripple, 100  $\mu$ F C<sub>IN</sub>; No external C<sub>OUT</sub>. Board mounted module, scope setting : 20 MHz analog BW, digital filter 1.5 bits -3 dB @ 12 MHz

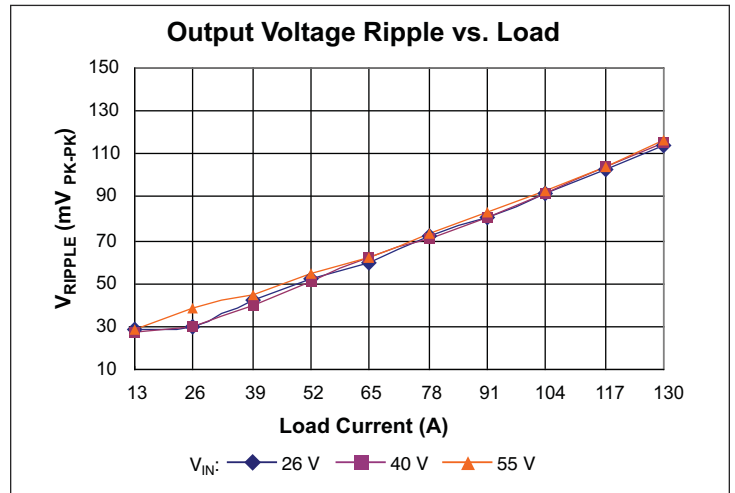


Figure 8 – V<sub>RIPPLE</sub> vs. I<sub>OUT</sub>; V<sub>IN</sub>. No external C<sub>OUT</sub>. Board mounted module, scope setting : 20 MHz analog BW, digital filter 1.5 bits -3 dB @ 12 MHz

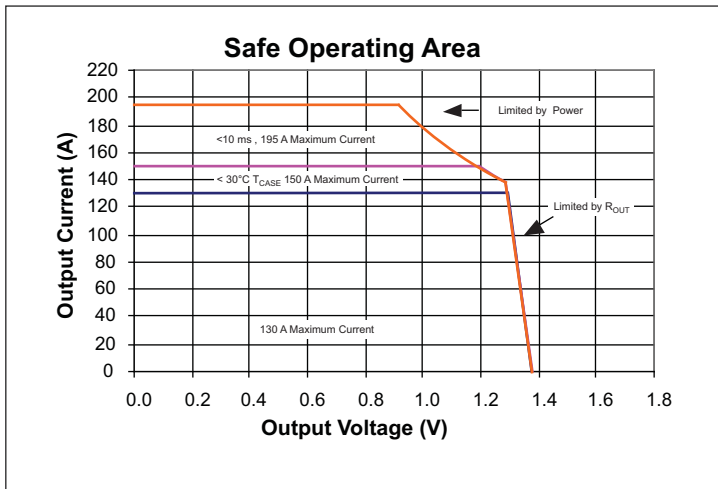


Figure 9 – Safe operating area

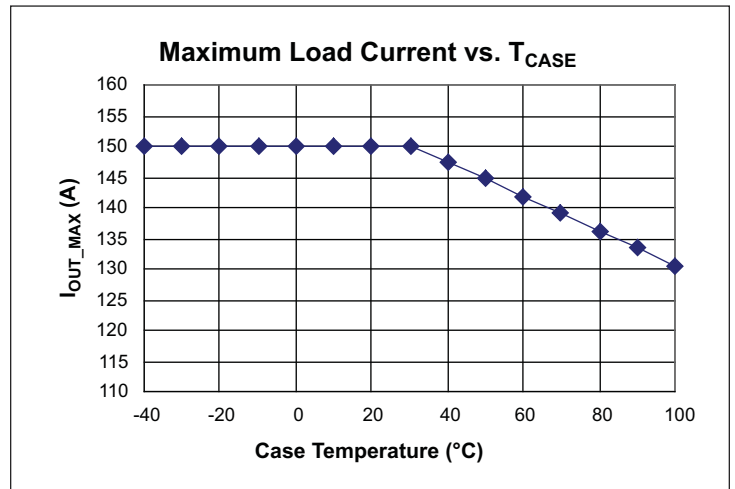


Figure 10 – Maximum load current using  $I_{out\_max} = -(2/7) * T_c + 159$ . Junction temperature less than 125°C

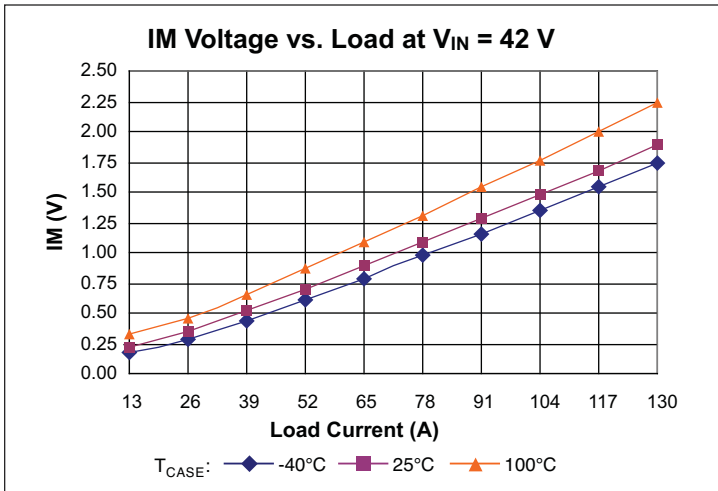


Figure 11 – IM voltage vs. load

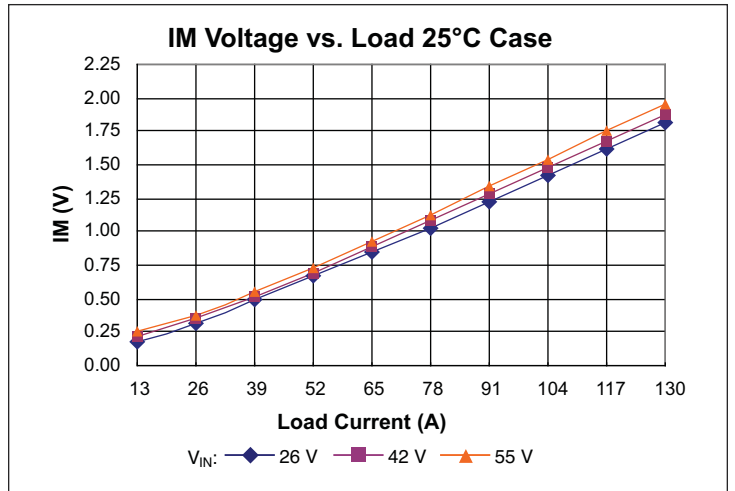


Figure 12 – IM voltage vs. load

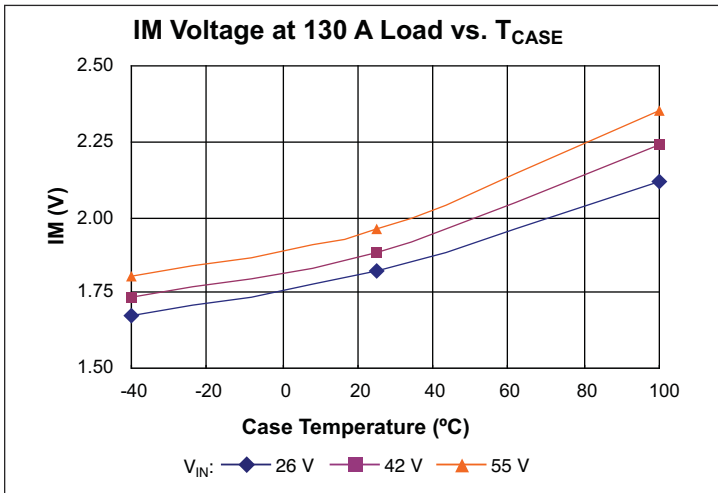


Figure 13 – Full load IM voltage vs.  $T_{CASE}$

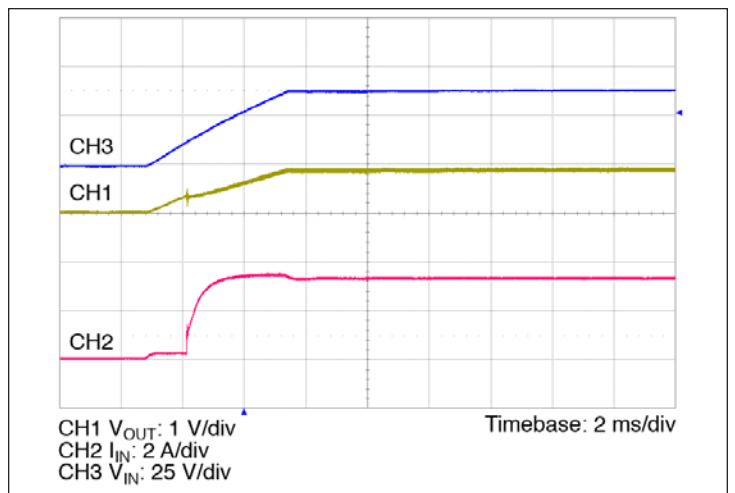


Figure 14 – Start up from application of  $V_{IN}$ ;  $V_C$  pre-applied

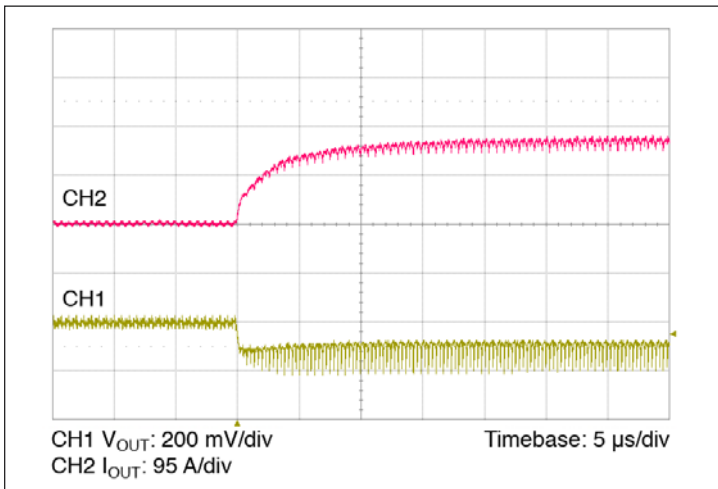


Figure 15 – 0 A – 150 A transient response:  
 $C_{IN} = 100 \mu F$ , no external  $C_{OUT}$

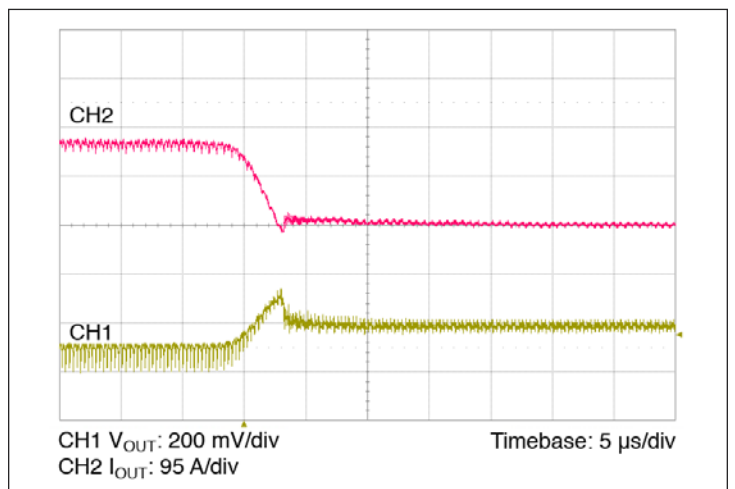


Figure 16 – 150 A – 0 A transient response:  
 $C_{IN} = 100 \mu F$ , no external  $C_{OUT}$

# VIV0005TFJ

## 6.0 GENERAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$  (T-Grade); All Other specifications are at  $T_J = 25^{\circ}\text{C}$  unless otherwise noted.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
<b>MECHANICAL</b>						
Length	L		32.25 / 1.27	32.5 / 1.28	32.75 / 1.29	mm/in
Width	W		21.75 / 0.86	22.0 / 0.87	22.25 / 0.88	mm/in
Height	H		6.48 / 0.255	6.73 / 0.265	6.98 / 0.275	mm/in
Volume	Vol	No heat sink		4.82 / 0.29		cm <sup>3</sup> /in <sup>3</sup>
Weight	W			0.512 / 14.5		oz/g
Lead Finish		Nickel	0.51		2.03	μm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
<b>THERMAL</b>						
Operating temperature	$T_J$		-40		125	°C
Thermal capacity				9		Ws/°C
<b>ASSEMBLY</b>						
Peak compressive force applied to case (Z-axis)		Supported by J-lead only		5	6	lbs
Storage temperature	$T_{ST}$		-40		125	°C
ESD withstand	ESD <sub>HBM</sub>	Human Body Model, "JEDEC JESD 22-A114C.01"	1000			$V_{DC}$
	ESD <sub>CDM</sub>	Charged Device Model, "JEDEC JESD 22-C101D"	400			
<b>SOLDERING</b>						
Peak temperature during reflow		MSL 5			225	°C
		MSL 6			245	°C
Peak time above 183°C					150	s
Peak heating rate during reflow				1.5	2	°C/s
Peak cooling rate post reflow				2.5	3	°C/s
<b>SAFETY</b>						
Working voltage (IN – OUT)	$V_{IN\_OUT}$				<b>60</b>	V <sub>bc</sub>
Isolation voltage (hipot)	$V_{HIPOT}$		<b>100</b>			V <sub>bc</sub>
Isolation capacitance	$C_{IN\_OUT}$	Unpowered unit	<b>0.018</b>	<b>0.02</b>	<b>0.022</b>	μF
Isolation resistance	$R_{IN\_OUT}$		<b>10</b>			MΩ
MTBF		MIL HDBK 217 Plus, 25°C, Ground Benign		3.9		MHrs
		Telcordia Issue 2, Method I		6.73		
Agency approvals / standards		cTUVus				
		cULus				
		CE Mark				
		RoHS 6 of 6				



## 7.0 USING THE CONTROL SIGNALS VC, PC, TM, IM

**VTM Control (VC)** pin is an input pin which powers the internal VCC circuitry within the specified voltage range of 26 V to 55 V. This voltage is required for VTM™ transformer start up, and must be applied as long as the input is below 26 V. In order to ensure a proper start, the slew rate of the applied voltage must be within the specified range. VC must be applied first to activate the controller prior to the input. When the input voltage is applied, the VTM output voltage will track the input allowing for a soft-start. If the VC voltage is removed prior to the input reaching 26 V, the VTM may shut down.

Some additional notes on using the VC pin:

- In most applications, the VTM module will be powered by an upstream PRM™ regulator, in which case the PRM will provide a typical 10 ms VC pulse during start up. In these applications the VC pins of the PRM and VTM should be tied together.
- The fault response of the VTM module is latching. A positive edge on VC, or toggling PC if VC is continuously applied, is required in order to restart the unit.
- The VTM is designed for continuous operation with VC applied.

**Primary Control (PC)** pin can be used to accomplish the following functions:

- Delayed start: Upon the application of VC, the PC pin will source a constant 100  $\mu$ A current to the internal RC network. Adding an external capacitor will allow further delay in reaching the 2.5 V threshold for module start.
- Auxiliary voltage source: Once enabled in regular operational conditions (no fault), each VTM PC provides a regulated 5 V, 2 mA voltage source.
- Output disable: PC pin can be actively pulled down in order to disable the module. Pull down impedance shall be lower than 850  $\Omega$ .
- Fault detection flag: The PC 5 V voltage source is internally turned off as soon as a fault is detected. It is important to notice that PC doesn't have current sink capability. Therefore, in an array, PC line will not be capable of disabling neighboring modules if a fault is detected.
- Fault reset: PC may be toggled to restart the unit if VC is continuously applied.

**Temperature Monitor (TM)** pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- Monitor the control IC temperature: The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e. 3.0 V = 300 K = 27°C). If a heat sink is applied, TM can be used to thermally protect the system.
- Fault detection flag: The TM voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of TM signal.

**Current Monitor (IM)** pin provides a voltage proportional to the output current of the VTM. The voltage will vary between 0.206 V and 1.825 V over the output current range of the VTM module (See Figures 11–13). The accuracy of the IM pin will be within 25% under all line and temperature conditions between 50% and 100% load. The accuracy of the pin can be improved using a predictive algorithm based on the input voltage and internal temperature.

## 8.0 THERMAL CONSIDERATIONS

V•I Chip™ products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input / output conditions, thermal management and environmental conditions. Maintaining the top of the VIV0005TFJ case to less than 100°C will keep all junctions within the V•I Chip module below 125°C for most applications.

The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a V•I Chip module for an extended period of time at full load without proper heat sinking.

## 9.0 FUSE SELECTION

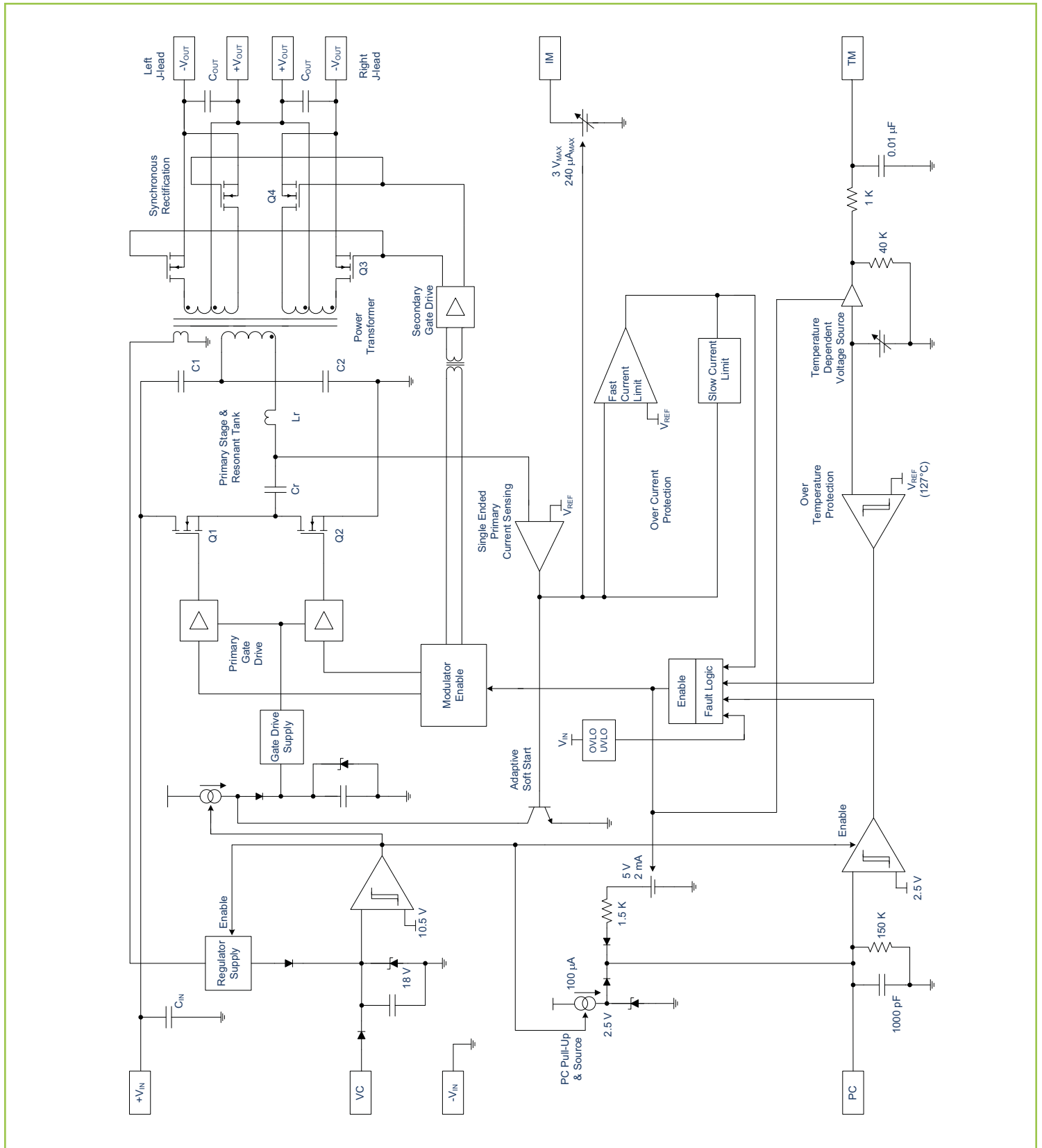
In order to provide flexibility in configuring power systems V•I Chip products are not internally fused. Input line fusing of V•I Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum VTM current)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting  $I^2t$

# VIV0005TFJ

## 10.0 VIV0005TFJ BLOCK DIAGRAM



## 11.0 SINE AMPLITUDE CONVERTER™ POINT OF LOAD CONVERSION

The Sine Amplitude Converter (SAC) uses a high frequency resonant tank to move energy from input to output. The resonant tank formed by Cr and leakage inductance Lr in the power transformer windings as shown in the VTM™ module Block Diagram (See Section 10). The resonant LC tank, operated at high frequency, is amplitude modulated as a

function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

The VIV0005TFJ SAC can be simplified into the following model:

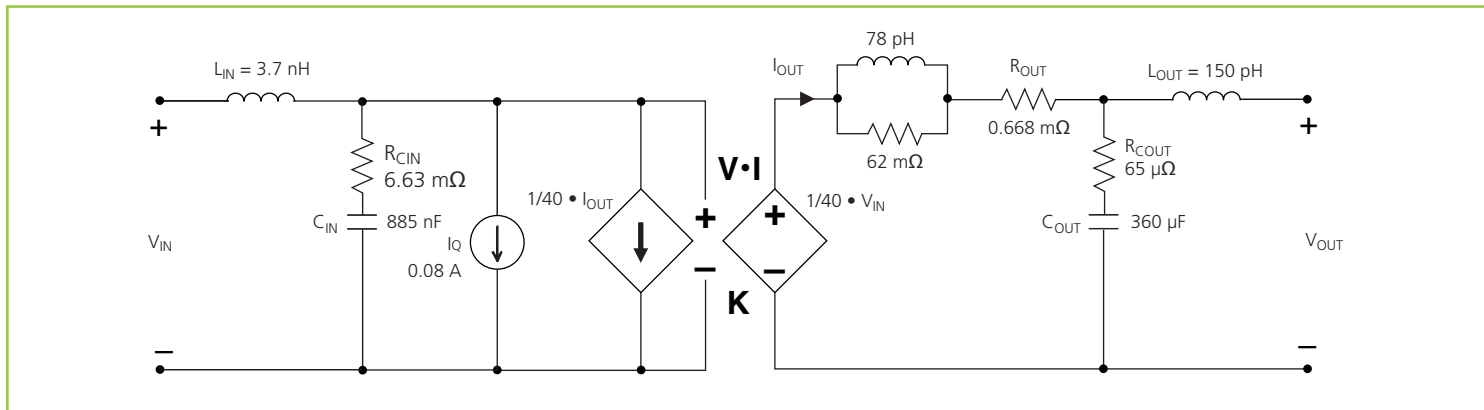


Figure 17 – V·I Chip™ AC model

At no load:

$$V_{OUT} = V_{IN} \cdot K \quad (1)$$

K represents the “turns ratio” of the SAC.

Rearranging Eq (1):

$$K = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In the presence of load,  $V_{OUT}$  is represented by:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R_{OUT} \quad (3)$$

and  $I_{OUT}$  is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \quad (4)$$

$R_{OUT}$  represents the impedance of the SAC, and is a function of the  $R_{DS(ON)}$  of the input MOSFETs and the winding resistance of the Power transformer.  $I_Q$  represents the quiescent current of the SAC control and gate drive circuitry.

The use of DC voltage transformation provides additional interesting attributes. Assuming that  $R_{OUT}$  and  $I_Q = 0$  A, Eq. (3)

now becomes Eq. (2) and is essentially load independent, resistor R is now placed in series with  $V_{IN}$  as shown in Figure 18.

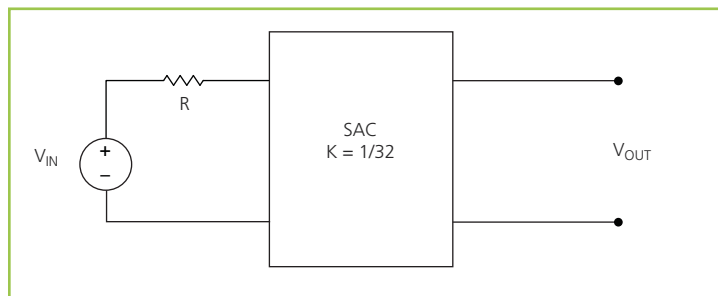


Figure 18 – K = 1/32 Sine Amplitude Converter with series input resistor

The relationship between  $V_{IN}$  and  $V_{OUT}$  becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \cdot R) \cdot K \quad (5)$$

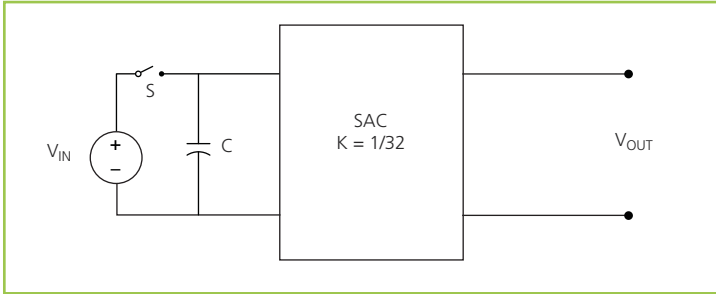
Substituting the simplified version of Eq. (4) ( $I_Q$  is assumed = 0 A) into Eq. (5) yields:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R \cdot K^2 \quad (6)$$

This is similar in form to Eq. (3), where  $R_{OUT}$  is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the input side of the SAC is effectively scaled by  $K^2$  with respect to the output.

Assuming that  $R = 1 \Omega$ , the effective R as seen from the secondary side is  $0.98 \text{ m}\Omega$ , with  $K = 1/32$  as shown in Figure 18.

A similar exercise should be performed with the addition of a capacitor or shunt impedance at the input to the SAC. A switch in series with  $V_{IN}$  is added to the circuit. This is depicted in Figure 19.



**Figure 19** – Sine Amplitude Converter™ with input capacitor

A change in  $V_{IN}$  with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C \frac{dV_{IN}}{dt} \quad (7)$$

Assume that with the capacitor charged to  $V_{IN}$ , the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \cdot K \quad (8)$$

Substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \cdot \frac{dV_{OUT}}{dt} \quad (9)$$

The equation specified in terms of the output has yielded a  $K^2$  scaling factor for C, in the denominator of the equation. A K factor less than unity results in an effectively larger capacitance on the output when expressed in terms of the input. With a  $K=1/32$  as shown in Figure 19,  $C=1 \mu\text{F}$  would appear as  $C=1024 \mu\text{F}$  when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance, or energy storage as a function of its K factor squared. However, these benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the VTM™ module are:

- No load power dissipation ( $P_{NL}$ ): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ( $R_{OUT}$ ): refers to the power loss across the VTM™ modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{ROUT} \quad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{ROUT} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{ROUT}}{P_{IN}} \quad (12)$$

$$= \frac{V_{IN} \cdot I_{IN} - P_{NL} - (I_{OUT})^2 \cdot R_{OUT}}{V_{IN} \cdot I_{IN}}$$

$$= 1 - \left( \frac{P_{NL} + (I_{OUT})^2 \cdot R_{OUT}}{V_{IN} \cdot I_{IN}} \right)$$

## 12.0 INPUT AND OUTPUT FILTER DESIGN

A major advantage of a SAC™ system versus a conventional PWM converter is that the former does not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

1. Guarantee low source impedance.

To take full advantage of the VTM™ module transformer dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The connection of the V•I Chip to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

2. Further reduce input and/or output voltage ripple without sacrificing dynamic response.

Given the wide bandwidth of the VTM module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the VTM module multiplied by its K factor.

3. Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures.

The V•I Chip module input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it. A criterion for protection is the maximum amount of energy that the input or output switches can tolerate if avalanched.

## 13.0 CAPACITIVE FILTERING CONSIDERATIONS FOR A SINE AMPLITUDE CONVERTER™

It is important to consider the impact of adding input and output capacitance to a Sine Amplitude Converter on the system as a whole. Both the capacitance value and the effective impedance of the capacitor must be considered.

A Sine Amplitude Converter has a DC  $R_{OUT}$  value which has already been discussed in section 11. The AC  $R_{OUT}$  of the SAC contains several terms:

- Resonant tank impedance
- Input lead inductance and internal capacitance
- Output lead inductance and internal capacitance

The values of these terms are shown in the behavioral model in section 11. It is important to note on which side of the transformer these impedances appear and how they reflect across the transformer given the K factor.

The overall AC impedance varies from model to model. For most models it is dominated by DC  $R_{OUT}$  value from DC to beyond 500 KHz. The behavioral model in section 11 should be used to approximate the AC impedance of the specific model.

Any capacitors placed at the output of the VTM reflect back to the input of the VTM module by the square of the K factor (Eq. 9) with the impedance of the VTM module appearing in series. It is very important to keep this in mind when using a PRM™ regulator to power the VTM module. Most PRMs have a limit on the maximum amount of capacitance that can be applied to the output. This capacitance includes both the PRM output capacitance and the VTM output capacitance reflected back to the input. In PRM remote sense applications, it is important to consider the reflected value of VTM output capacitance when designing and compensating the PRM control loop.

Capacitance placed at the input of the VTM appear to the load reflected by the K factor with the impedance of the VTM in series. In step-down VTM ratios, the effective capacitance is increased by the K factor. The effective ESR of the capacitor is decreased by the square of the K factor, but the impedance of the VTM appears in series. Still, in most step-down VTM modules an electrolytic capacitor placed at the input of the module will have a lower effective impedance compared to an electrolytic capacitor placed at the output. This is important to consider when placing capacitors at the output of the module. Even though the capacitor may be placed at the output, the majority of the AC current will be sourced from the lower impedance, which in most cases will be the VTM module. This should be studied carefully in any system design using a VTM module. In most cases, it should be clear that electrolytic output capacitors are not necessary to design a stable, well-bypassed system.

## 14.0 CURRENT SHARING

The SAC™ topology bases its performance on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array with the same K factor, the VTM module will inherently share the load current with parallel units according to the equivalent impedance divider that the system implements from the power source to the point of load.

It is important to notice that, when successfully started, VTMs are capable of bi-directional operation. Reverse power transfer is enabled if the VTM input falls within its operating range and the VTM is otherwise enabled. In parallel arrays, because of  $R_{OUT}$ , circulating currents are never experienced due to energy conservation law.

Some general recommendations to achieve matched array impedances:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide the PCB layout as symmetrical as possible.
- Apply same input / output filters (if present) to each unit.

For further details see [AN:016 Using BCM™ Bus Converters in High Power Arrays](#).

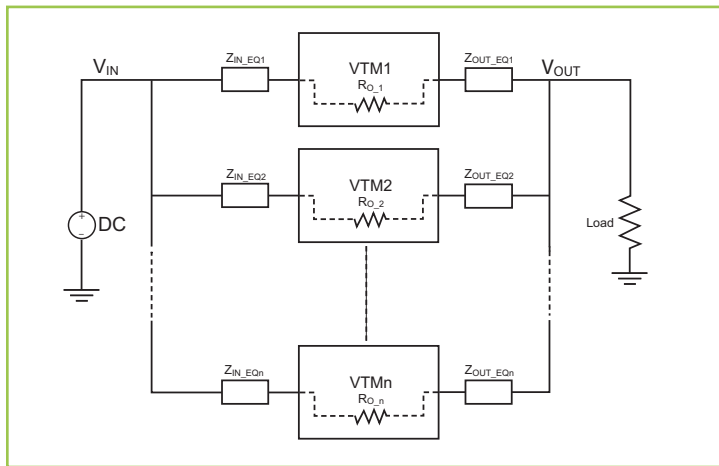


Figure 20 – VTM™ Transformer array

## 15.0 REVERSE INRUSH CURRENT PROTECTION

The VIV0005TFJ provides reverse inrush protection which prevents reverse current flow until the input voltage is high enough to first establish current flow in the forward direction. In the event that there is a DC voltage present on the output before the VTM module is powered up, this feature protects sensitive loads from excessive dV/dT during power up as shown in Figure 21.

If a voltage is present at the output of the VTM module which satisfies the condition  $V_{OUT} > V_{IN} \cdot K$  after a successful power up the energy will be transferred from secondary to primary. The input to output ratio of the VTM module will be maintained. The VTM module will continue to operate in reverse as long as the input and output voltages are within the specified range. The VIV0005TFJ has not been qualified for continuous reverse operation.

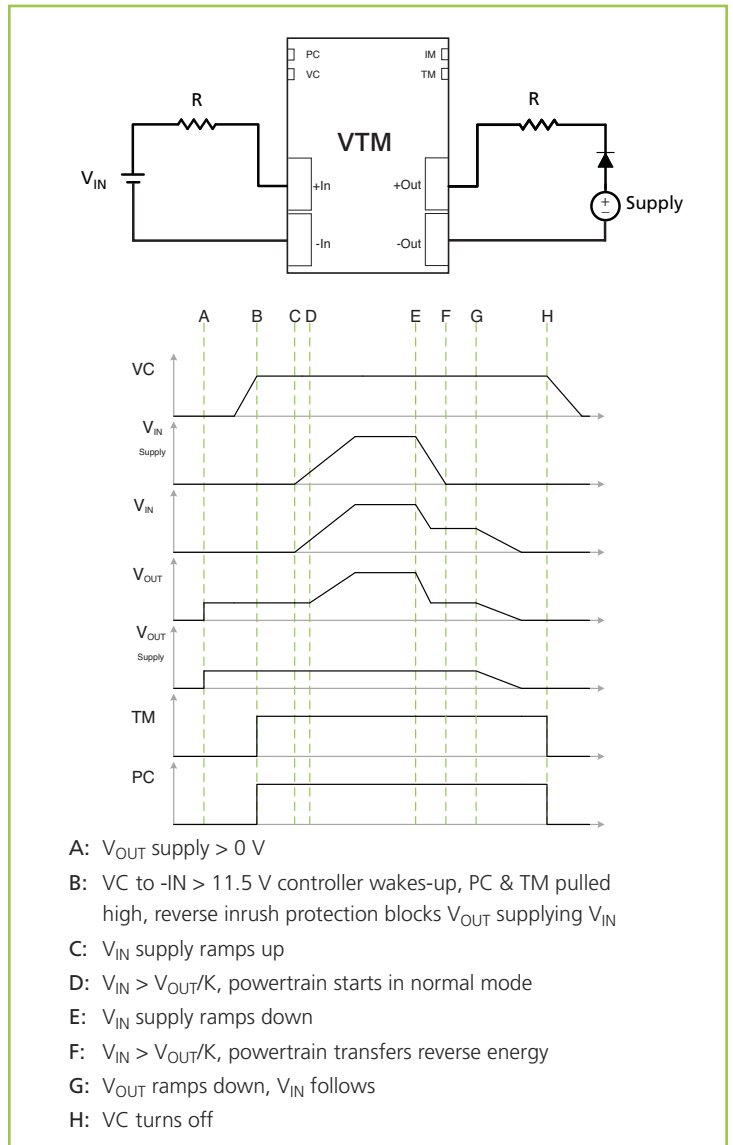


Figure 21 – Reverse inrush protection

## 16.0 LAYOUT CONSIDERATIONS

The VIV0005TFJ requires equal current density along the output J-leads to achieve rated efficiency and output power level. The negative output J-leads are not connected internally and must be connected on the board as close to the VTM™ transformer as possible. The layout must also prevent the high output current of the VIV0005TFJ from interfering with the input-referenced signals.

To achieve these requirements, the following layout guidelines are recommended:

- The total current path length from any point on the  $V_{+OUT}$  J-leads to the corresponding point on the  $V_{-OUT}$  J-leads should be equal (see Figure 22).
- Use vias along the negative output J-leads to connect the negative output to a common power plane.
- Use sufficient copper weight and number of layers to carry the output current to the load or to the output connectors.
- Be sure to include enough vias along both the positive and negative J leads to distribute the current among the layers of the PCB.
- Do not run input-referenced signal traces (VC, PC, TM and IM) between the layers of the secondary outputs.
- Run the input-referenced signal traces (VC, PC, TM and IM) such that  $V_{-IN}$  shields the signals. See [AN:005 FPA Printed Circuit Board Layout Guidelines](#) for more details.

Equalizing the current paths is most easily accomplished by centering the VTM module output J-leads between the output connections of the PCB and by designing the board such that the layout is symmetric from both sides of the output and from the front and back ends of the output as shown in Figures 23 and 24.

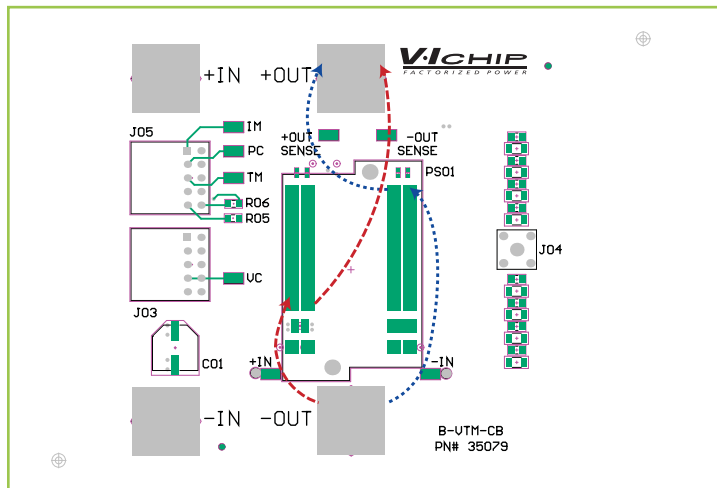


Figure 22 – Equal current path

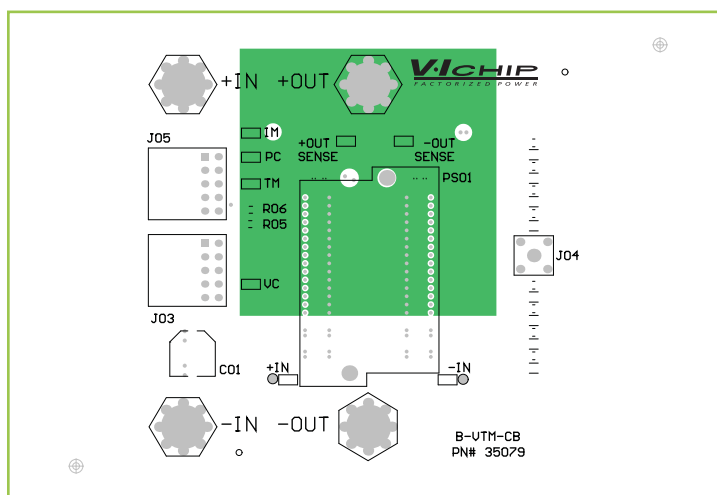


Figure 23 – Symmetric layout

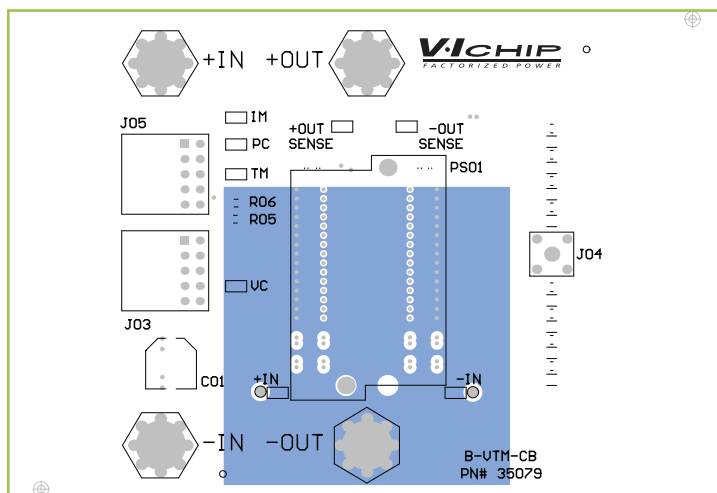
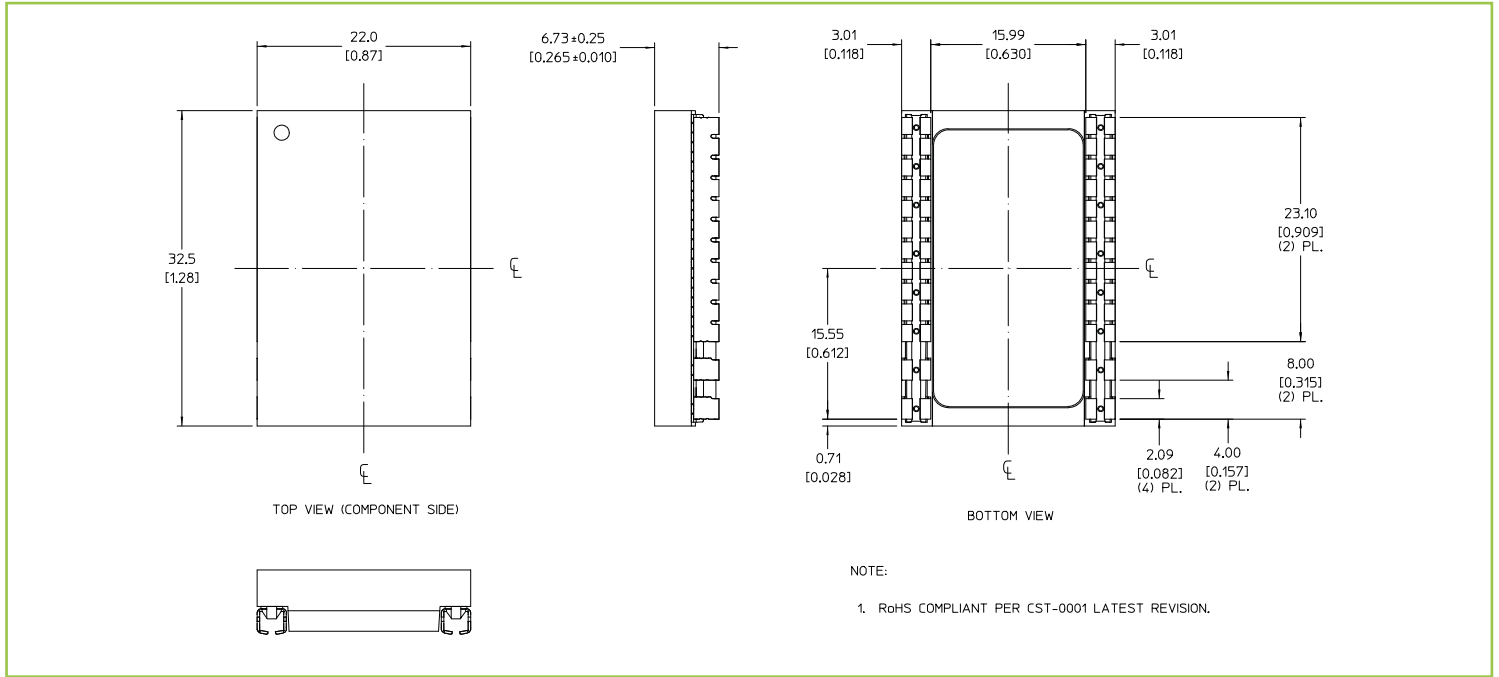


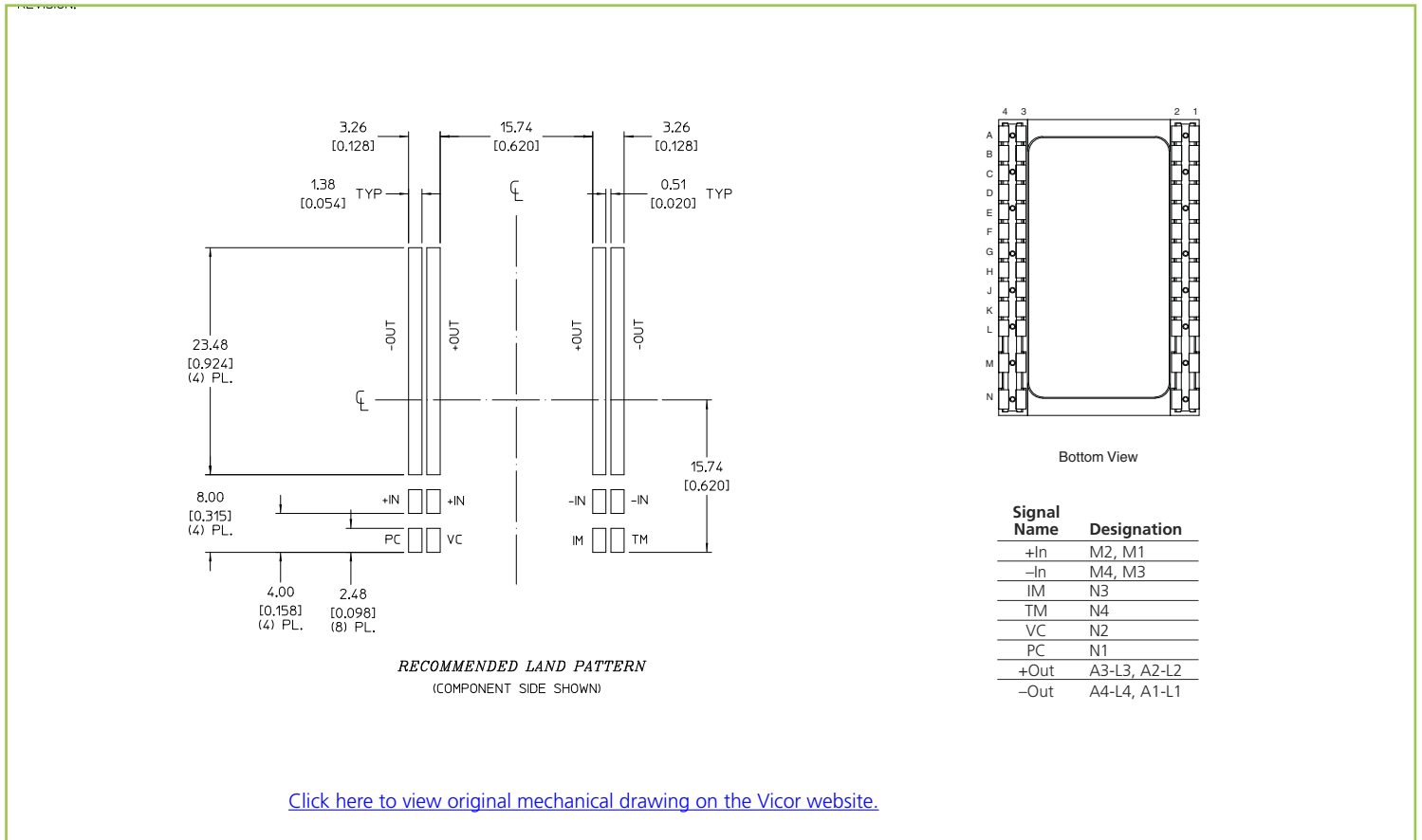
Figure 24 – Symmetric layout

# VIV0005TFJ

## 17.0 MECHANICAL DRAWING



## 17.1 RECOMMENDED LAND PATTERN



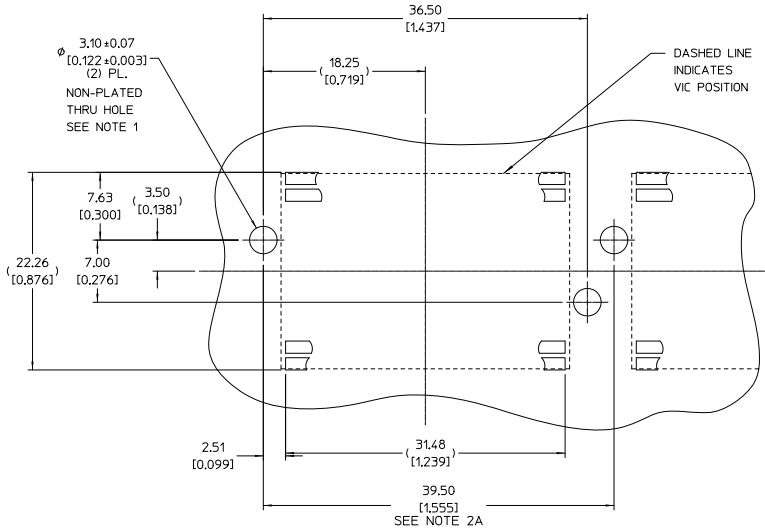
[Click here to view original mechanical drawing on the Vicor website.](#)



## 17.2 RECOMMENDED LAND PATTERN FOR PUSH PIN HEAT SINK

### RECOMMENDED LAND PATTERN (NO GROUNDING CLIPS)

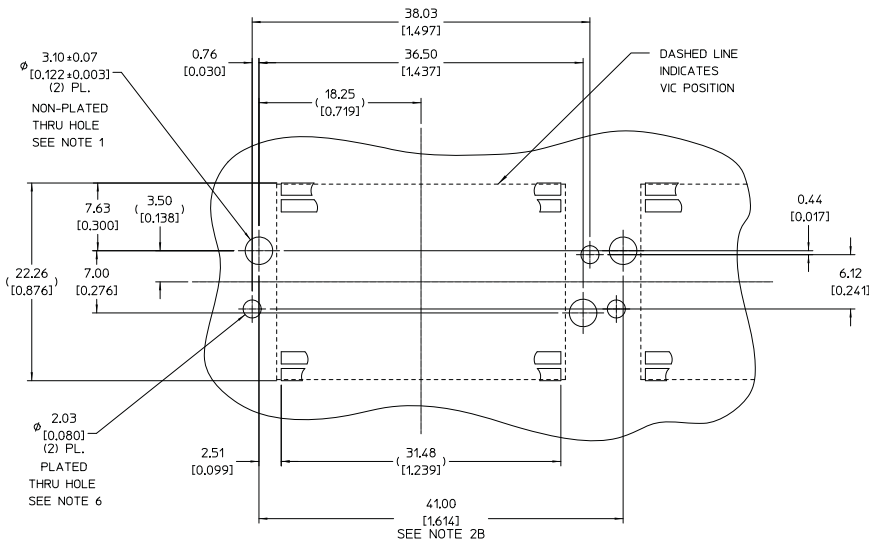
TOP SIDE SHOWN



- NOTES:
1. MAINTAIN 3.50 [0.138] DIA. KEEP-OUT ZONE FREE OF COPPER, ALL PCB LAYERS.
  2. (A) MINIMUM RECOMMENDED PITCH IS 39.50 [1.555], THIS PROVIDES 7.00 [0.275] COMPONENT EDGE-TO-EDGE SPACING, AND 0.50 [0.020] CLEARANCE BETWEEN VICOR HEAT SINKS.  
  
(B) MINIMUM RECOMMENDED PITCH IS 41.00 [1.614], THIS PROVIDES 8.50 [0.334] COMPONENT EDGE-TO-EDGE SPACING, AND 2.00 [0.079] CLEARANCE BETWEEN VICOR HEAT SINKS.
  3. V-I CHIP LAND PATTERN SHOWN FOR REFERENCE ONLY; ACTUAL LAND PATTERN MAY DIFFER. DIMENSIONS FROM EDGES OF LAND PATTERN TO PUSH-PIN HOLES WILL BE THE SAME FOR ALL FULL SIZE V-I CHIP PRODUCTS.

### RECOMMENDED LAND PATTERN (With GROUNDING CLIPS)

TOP SIDE SHOWN



4. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
5. UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE MM [INCH]. TOLERANCES ARE:  
X.X [X.XX] = ±0.3 [0.01]  
X.XX [X.XXX] = ±0.13 [0.005]
6. PLATED THROUGH HOLES FOR GROUNDING CLIPS (33855) SHOWN FOR REFERENCE. HEATSINK ORIENTATION AND DEVICE PITCH WILL DICTATE FINAL GROUNDING SOLUTION.

[Click here to view original mechanical drawing on the Vicor website.](#)

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