HDC Module

HDC300B120x400y-00

Isolated, Regulated DC-DC Converter

Features

- Isolated , regulated DC-to-DC converter
- Up to 400 W, 33.3 A continuous
- 93.2% peak efficiency
- 128 W/in^2 power density
- Wide input range 180 to 420 Vdc
- ZVS high frequency (MHz) switching
  - Enables low profile, high-density filtering
- Full operation during current limit
- OV, OC, UV, short circuit and thermal protection
- Through-hole Brick Package

Overview

- Part of the new HD Series of power conversion products
- Companion models to HDR Regulator Family
- Input Voltage: 180 to 420 Vdc
- Output: 12 Vdc
- Output Current to 33.3 Amperes
- Agency approvals: CE Mark

Product Overview

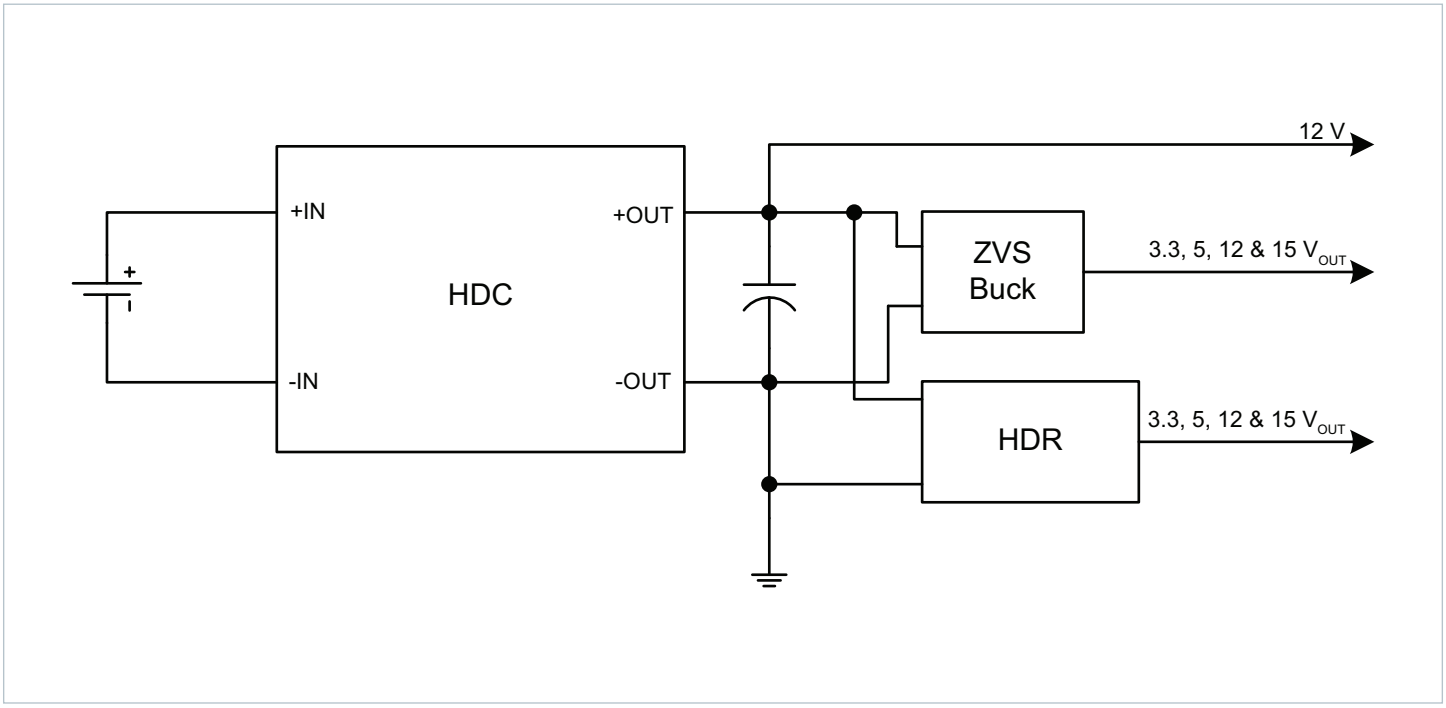
The HDC Isolated, Regulated DC Converter is a DC-to-DC converter, operating from an unregulated, wide range input to generate an isolated 12 Vdc output. With its high frequency zero voltage switching (ZVS) topology, the HDC consistently delivers high efficiency across the input line range. Modular HDC and downstream DC-DC products support efficient power distribution, providing superior power system performance and connectivity from a variety of unregulated power sources to the point-of-load.

Part Number Designation

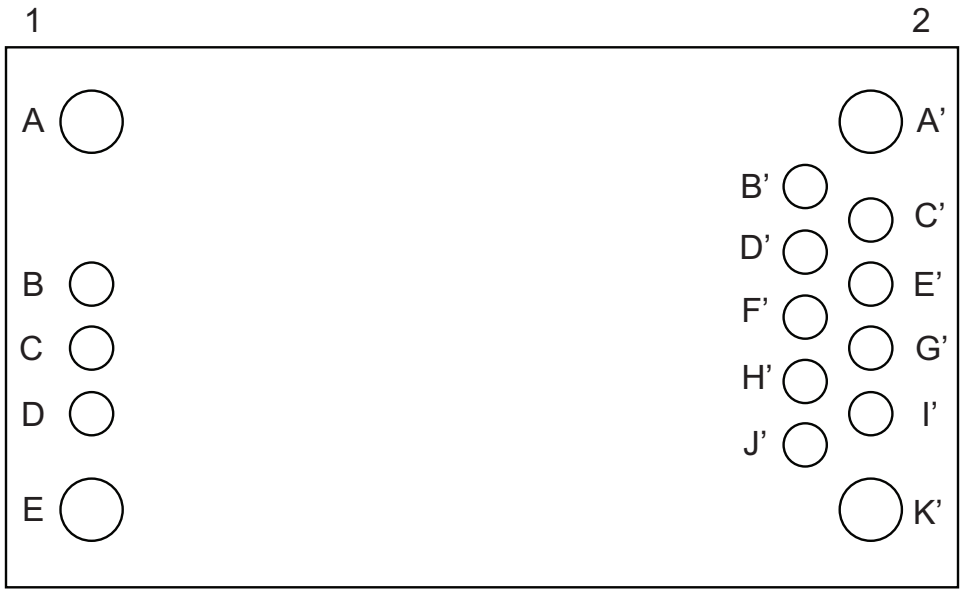
Model	Input Voltage	Package	Output Voltage (Nom.) x10	Temperature Grade	Power	Pin /Base	-	Rev / Var
HDC	300	B	120	x	400	L	-	00

- **HDC** = HD Converter Family
- **300** = 180 - 420 Vdc
- **B** Series
- **120** = (V_{OUT} nominal) x 10
- **C** = -20°C > T_{STG} > 100°C, -20°C > T_J > +125°C
  T = -40°C > T_{STG} > 100°C, -40°C > T_J > +125°C
  M = -65°C > T_{STG} > 100°C, -55°C > T_J > +125°C
- **400** = Max rated output power
- **L** = Flanged baseplate
  N = Flangeless baseplate
- **00** = Module
  CB = Evaluation Board

Typical Application



Pin Configuration



Pin Descriptions

Pin Number	Signal Name	Type	Function
A1	+IN	INPUT POWER	Positive input power terminal
B1	FT	DIGITAL OUTPUT	Fault indicator
C1	PC	DIGITAL INPUT	Primary control
D1	NC	NO CONNECTION	Do not connect to this pin
E1	-IN	INPUT POWER	Negative input power terminal
A'2	+OUT	OUTPUT POWER	Positive output power terminal
B'2, D'2	NC	NO CONNECTION	Do not connect to this pin
C'2	+S	OUTPUT POWER	Positive remote sense
E'2	VDD	OUTPUT POWER	3.3 V regulated voltage source for trimming
F'2	VDDB	INPUT POWER	Semi-regulated voltage for future use
G'2	TR	ANALOG INPUT	V_{OUT} trim reference to SGND
H'2	FB	DIGITAL OUTPUT	Feedback PWM pulses for master-slave array for future use
I'2	-S	OUTPUT POWER	Negative remote sense
J'2	SGND	GROUND	Signal ground
K'2	-OUT	OUTPUT POWER	Negative output power terminal

Absolute Maximum Ratings

Parameter	Rating	Unit	Notes
+In to –In voltage	-0.5 to 550	Vdc	550 for 100 ms
FT to –In	-0.5 to 3.6	Vdc	
PC to –In voltage	-0.5 to 3.3	Vdc	
+Out to –Out voltage, +S to -Out	-0.5 to 13.2	Vdc	Externally applied
VDD to -Out	-0.5 to 3.6	Vdc	
VDDB to -Out	-0.5 to 17.6	Vdc	
TR to -Out	-0.5 to 3.6	Vdc	
FB to -Out	-0.5 to 3.6	Vdc	
Operating Temperature	-55 to +125	°C	M-Grade
Storage Temperature	-65 to +125	°C	M-Grade
Mounting torque	5 (0.57)	in / lbs (N-M)	4 each

Electrical Specifications

Specifications apply over all line, trim and load conditions, T_{INT} (internal) = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Module Input Specifications						
Input voltage range, continuous operation	V_{IN}		180	300	420	V
Inrush current (peak)	I_{INRP}	With maximum $C_{OUT-EXT}$, full resistive load, over V_{IN} and trim			5	A
External input capacitance	C_{IN-EXT}		0.68			µF
Input inductance (external)	L_{IN}	Differential mode, with no further line bypassing			10	µH
Input power – disabled	P_Q	Nominal line			1.5	W
		Worst case line			2	W
Input power – enabled, no load	P_{NL}	Nominal line			2.4	W
		Worst case line			5	W
Module Output Specifications						
Output voltage set point	V_{OUT}	V_{IN} = 300, trim inactive, at full load	11.82	12	12.18	V
Output voltage trim range	$V_{OUT-TRIMING}$	At full rated load current	7.2		13.2	V
V_{OUT} accuracy	$\%_{VOUT-ACCURACY}$	The total output voltage setpoint accuracy from the calculated ideal Vout based on load, temp and trim			1.5	%
Rated output power	P_{OUT}	Continuous, $V_{OUT} \geq 12$, $180 < V_{IN} < 420$			400	W
Rated output current	I_{OUT}	Continuous, $V_{OUT} \geq 12$, $180 < V_{IN} < 420$			33.3	A
Output current limit	$I_{OUT-LIM}$	Low trim, will not shutdown when started into max C_{OUT}	38.7		43.1	A
		Nominal trim, will not shutdown when started into max C_{OUT}	38.9		41.1	
		High trim, will not shutdown when started into max C_{OUT}	32.5		37.7	
Current limit delay	$t_{IOUT-LIM}$	The module will power limit in a fast transient event		1		ms
Efficiency	η	Full load, nominal line, trim inactive	92.3	93.5		%
		Full load, over line and temperature, trim inactive	91.2			%
		50% load, over line, temperature and trim	89.5			%
Output voltage ripple	V_{OUT-PP}	Over all operating steady-state line, load and trim conditions, 20 MHz BW with minimum $C_{OUT-EXT}$		240		mV
Output capacitance (external)	$C_{OUT-EXT}$	Electrolytic capacitor preferred. Excludes component tolerances and temperature coefficient	1000		10000	µF
Initialization delay						
Output turn-on delay	t_{ON}	From rising edge PC, with V_{IN} pre-applied, V_{OUT} no trim	400	500	TBD	ms
Output turn-off delay	t_{OFF}	From falling edge PC			TBD	µs
Voltage deviation (transient)	$\%V_{OUT-TRANS}$	$C_{OUT-EXT}$ = min; (10 to 90% load step), excluding load line. Load transient slew rate up to full load current per ms		5	10	%
Recovery time	t_{TRANS}			1		ms

Electrical Specifications (cont.)

Specifications apply over all line, trim and load conditions, T_{INT} (internal) = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protection						
V_{IN} undervoltage threshold	$V_{IN-UVLO-}$		125		155	V
V_{IN} undervoltage recovery threshold	$V_{IN-UVLO+}$				177	V
V_{IN} overvoltage threshold	$V_{IN-OVLO+}$				455	V
V_{IN} overvoltage recovery threshold	$V_{IN-OVLO-}$		423			V
Overtemperature threshold (internal)	$T_{INT-OVP}$				125	°C
Short circuit, or temperature fault recovery time	t_{FAULT}			1		s

Signal Specifications

All specifications valid at 100% rated load and over specified input voltage range at 25°C, unless otherwise indicated.

Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C.

Fault: FT								
• The fault pin is the Fault flag pin. • When the module is enabled and no fault is present, the FT pin does not have current drive capability. • Whenever the powertrain stops (due to a fault protection or disabling the module by pulling PC low), the FT pin outputs V_{DD} and provides current to drive an external circuit. • When the module starts up, the FT pin is pulled high to V_{DD} during microcontroller initialization and will remain high until soft start process starts								
SIGNAL TYPE	**STATE**	**ATTRIBUTE**	**SYMBOL**	**CONDITIONS / NOTES**	**MIN**	**TYP**	**MAX**	**UNIT**
DIGITAL INPUT	FT Inactive	Internally generated V_{DD}			3.21	3.3	3.39	V
		FT internal pull up resistance to V_{DD}	$R_{FAULT-INACTIVE}$		9.5	10.0	10.5	kΩ
	FT Active	FT Voltage	$V_{FAULT-ACTIVE}$	At load = 4 ma	3.0			V
		FT current drive capability	$I_{FAULT-ACTIVE}$	Over-current FT drive beyond its capability may cause module damage			4	mA
		FT response time	$t_{RESPONSE-FAULT}$	After fault detected		200		µs
			$t_{RESPONSE-TIME}$	After PC being pulled low		5		µs
			$t_{RESPONSE-TIME1}$	After the module returns to no fault state, the time for FT to become inactive, for input UVLO and OVLO			1	ms
			$t_{RESPONSE-TIME2}$	After the module returns to no fault state, the time for FT to become inactive, for other (slower recovery) fault types			1	ms

Primary Control: PC								
• The PC pin enables and disables the converter; when held low the unit will be disabled. • The PC pin has an internal pull-up to V_{DD} and is referenced to the –IN pin of the converter.								
SIGNAL TYPE	**STATE**	**ATTRIBUTE**	**SYMBOL**	**CONDITIONS / NOTES**	**MIN**	**TYP**	**MAX**	**UNIT**
DIGITAL INPUT	Any	PC enable threshold	V_{PC-EN}				2.31	V
		PC disable threshold	V_{PC-DIS}		0.99			V
		Internally generated V_{DD}	V_{DD}		3.21	3.3	3.39	V
		PC internal pull up resistance to V_{DD}	$R_{ENABLE-INT}$	Pull up to V_{DD}	9.5	10.0	10.5	kΩ

Signal Specifications

All specifications valid at 100% rated load and over specified input voltage range at 25°C, unless otherwise indicated.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C.

Trim: TR

- The TR pin enables and disables trim functionality when V_{IN} is applied to the HDC. TR pin voltage is sampled right before soft start stage during startup
- If TR is not floating at power up and has a voltage less than TR trim enable threshold, trim is active
- If trim is active, the TR pin provides dynamic trim control with at least 500 Hz of -3 dB control bandwidth over the output voltage of the HDC
- The TR pin has an internal pull-up to V_{DD} and is referenced to SGND pin of the converter

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Regular Operation	FB Peak Voltage	V_{FB}				3.15	V
		PWM Frequency	F_{PWM}		3.20			V
ANALOG INPUT	Operational with Trim enabled	Internally generated V_{DD}	V_{DD}		3.23	3.30	3.37	V
		TR pin analog range	$V_{TRIM-RANGE}$		0	2.486	3.1	V
		V_{OUT} step resolution	$V_{OUT-RES}$	With V_{DD} = 3.3 V		6.21		mV
		TR internal pull up resistance to V_{DD}	$R_{TRIM-INT}$		5.105	5.11	5.115	kΩ

Regulated Voltage: VDD

- Regulated supply power
- Intended to be used as low current supply for ancillary circuits

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
POWER OUTPUT	Regular Operation	V_{DD} Voltage output	V_{VDD_OUT}		3.23	3.30	3.37	V
		V_{DD} Source current	I_{VDD_OUT}				20	mA

Semi-regulated Voltage: VDDB

- Unregulated supply power input, required for future products

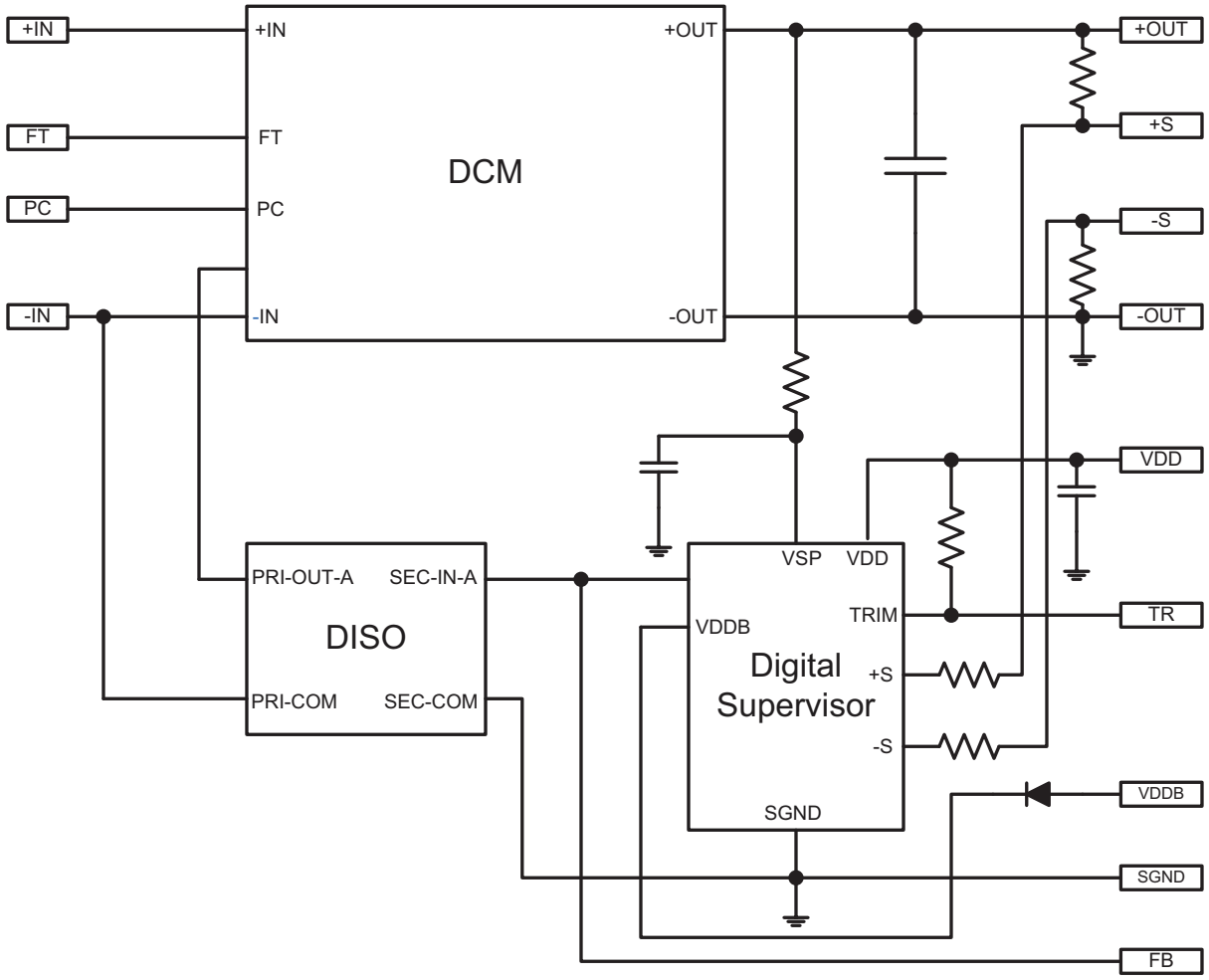
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
POWER INPUT	Regular Operation	VDDB Voltage	V_{VDDB}		4		16	V
		VDDB Current consumption	I_{VDDB}	V_{DD} pin not loaded		18	30	mA

Feedback: FB

- PWM voltage regulation feedback from Digital Supervisor to DCM
- Intended to be used for a parallel array (future option)

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL OUTPUT	Regular Operation	FB Peak Voltage	V_{FB}			3.3	3.37	V
		PWM Frequency	F_{PWM}			25		kHz
		FB PWM Duty Cycle	DC_{FB}		1		97	%

Block Diagram



Typical Performance Characteristics

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

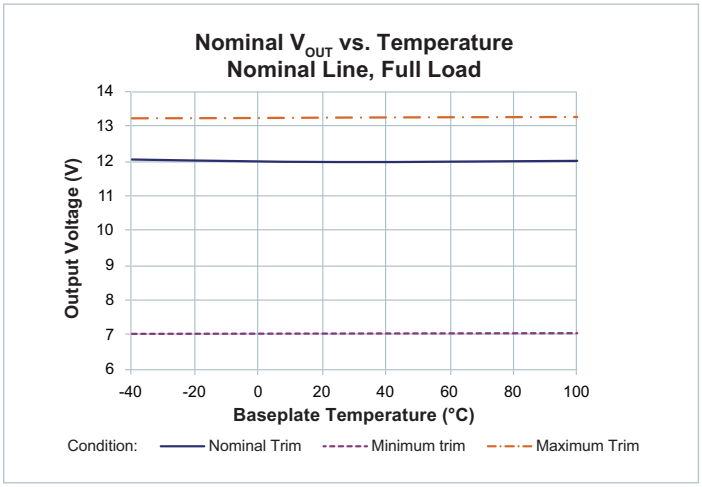


Figure 2 — *V_{OUT} vs. operating temperature trend, at full load and nominal line*

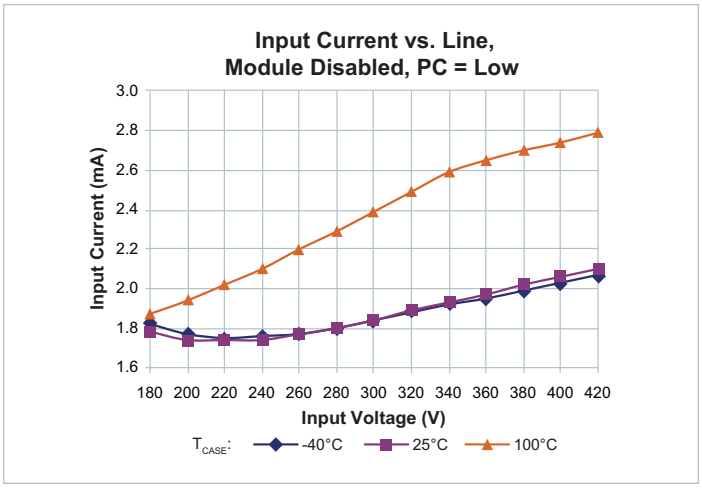


Figure 3 — *Disabled current consumption vs. V_{IN}*

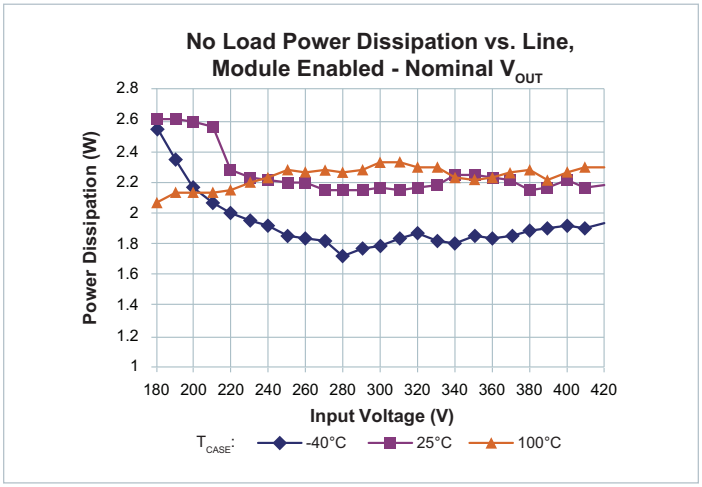


Figure 4 — *No load power dissipation vs. V_{IN}, at nominal trim*

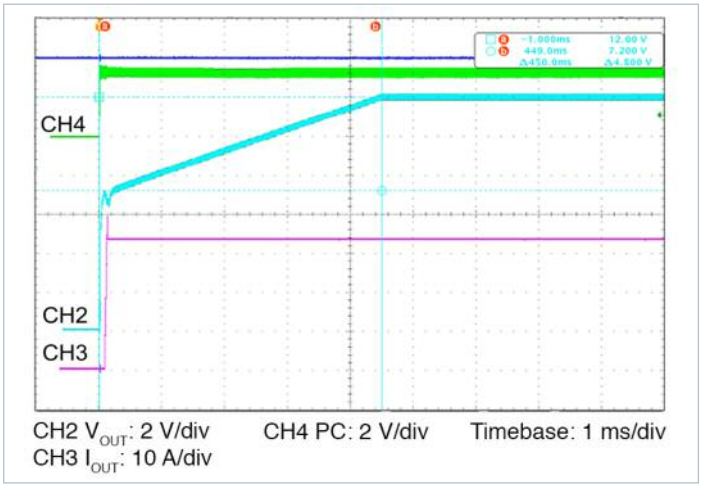


Figure 5 — *Initial startup from PC pin, with soft-start ramp. Nominal V_{IN}, C_{OUT_EXT} = 10000 uF, full load*

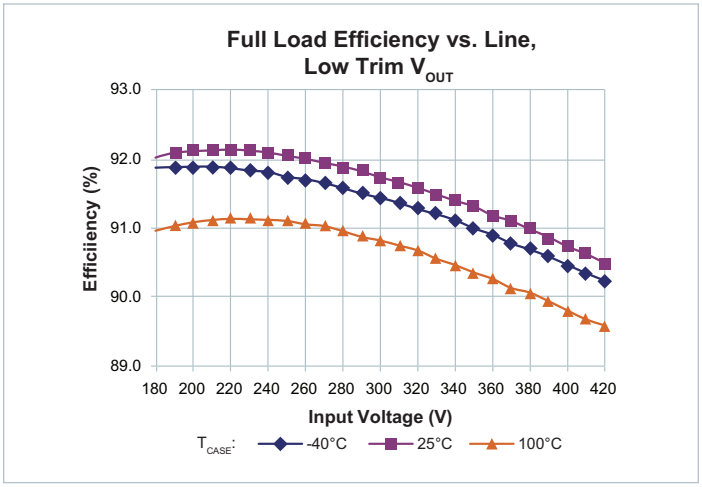


Figure 6 — *Full load efficiency vs. V_{IN}, V_{OUT} = 7.2 V*

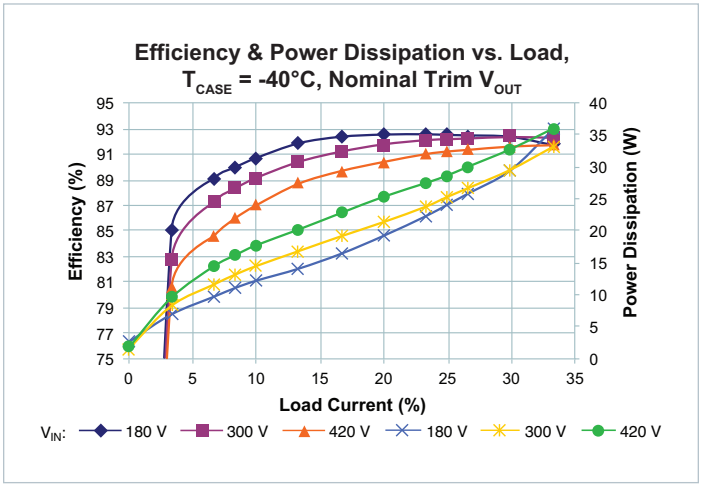


Figure 7 — *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = -40°C*

Typical Performance Characteristics (Cont.)

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

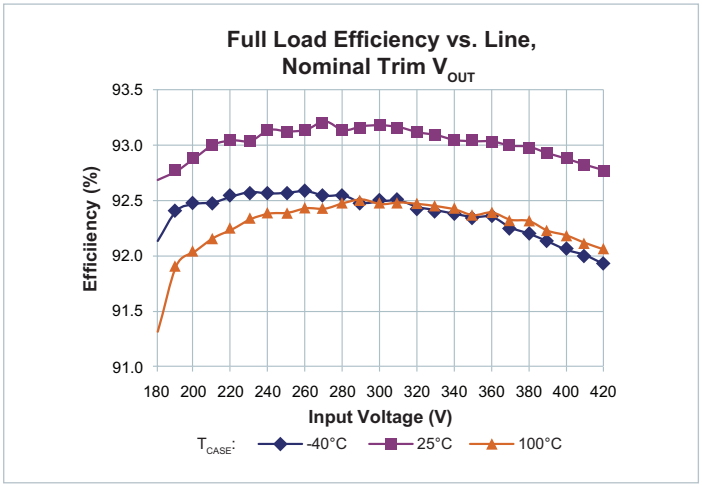


Figure 8 *— Full load efficiency vs. V_{IN}, V_{OUT} = 12 V*

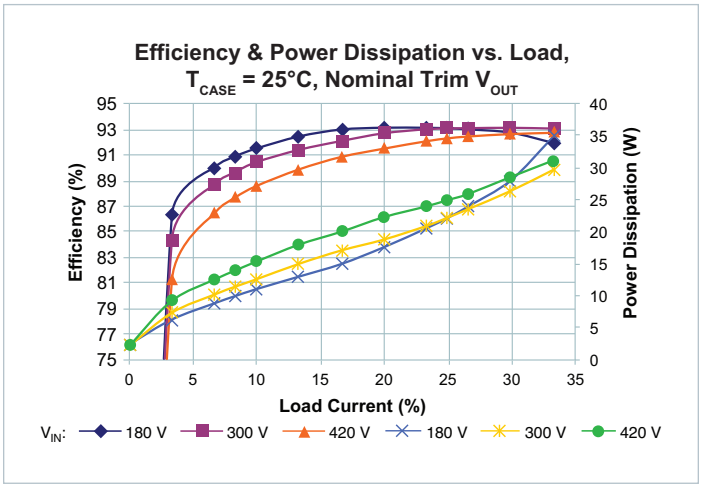


Figure 9 *— V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 25°C*

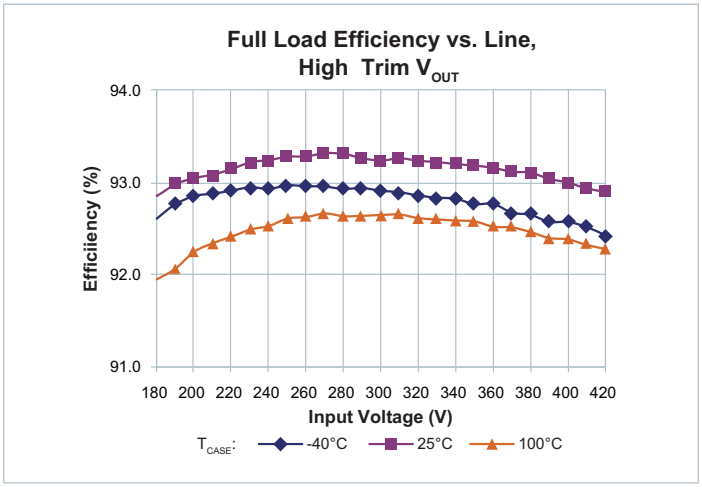


Figure 10 *— Full load efficiency vs. V_{IN}, V_{OUT} = 13.2 V*

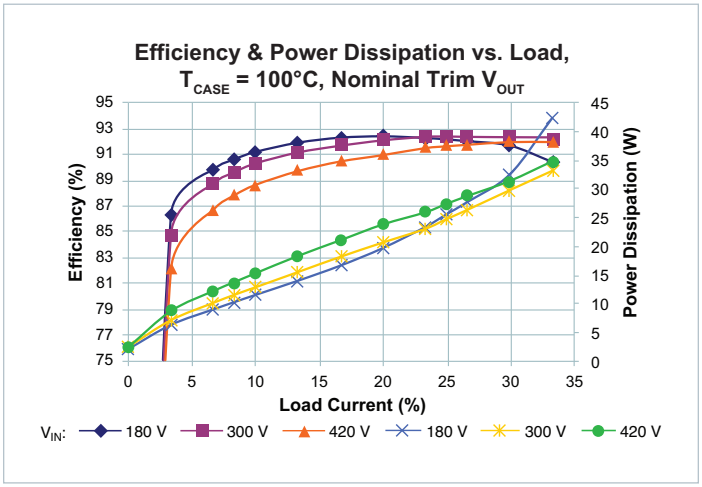


Figure 11 *— V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 100°C*

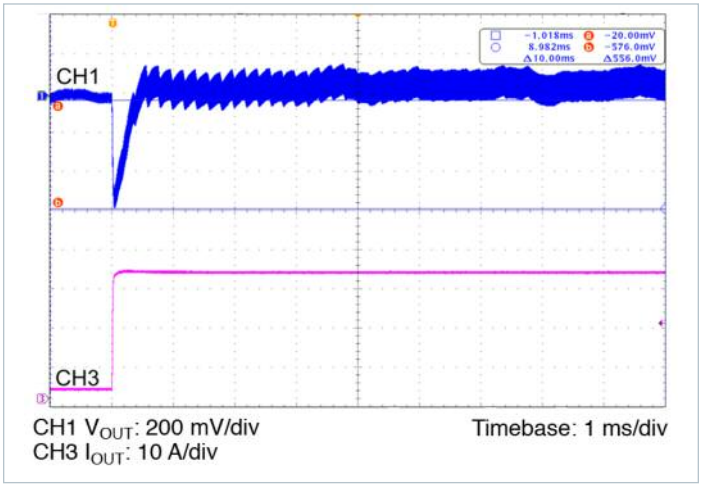


Figure 12 *— 10% to 100% load transient response, V_{IN} = 300 V, nominal trim, C_{OUT_EXT} = 1000 µF*

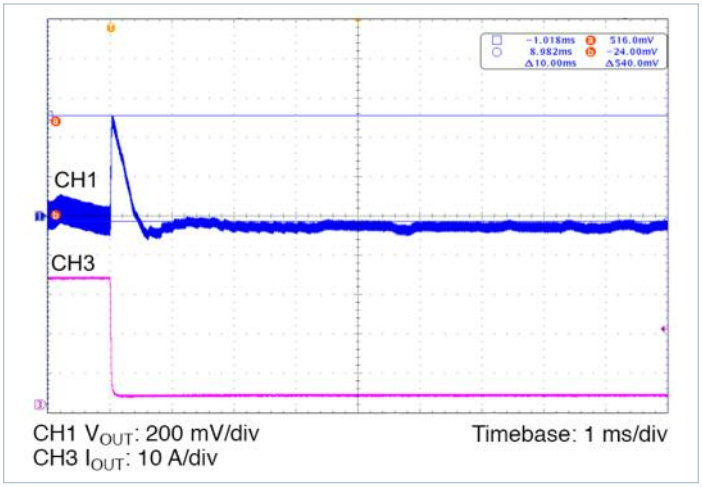


Figure 13 *— 100% to 10% load transient response, V_{IN} = 300 V, nominal trim, C_{OUT_EXT} = 1000 µF*

Typical Performance Characteristics (Cont.)

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

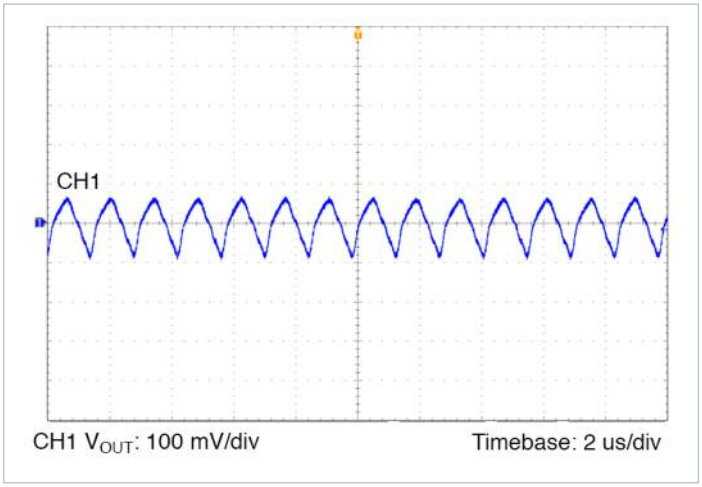


Figure 14 — *Typical output voltage ripple, V_{IN} = 300 V, V_{OUT} = 12 V, C_{OUT_EXT} = 1000 µF, full load*

General Characteristics

Specifications apply over all line, trim and load conditions, T_{INT} (internal) = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Flanged and flangeless baseplate	56.62 / [2.23]	57.00 / [2.24]	57.39 / [2.26]	mm/[in]
Width	W	Flanged baseplate	46.12 / [1.82]	46.50 / [1.83]	46.88 / [1.85]	
		Flangeless baseplate	34.61 / [1.36]	34.99 / [1.38]	35.37 / [1.39]	
Height	H	Flanged and flangeless baseplate	15.36 / [0.61]	16.00 / [0.63]	16.36 / [0.66]	
Volume	Vol	Flanged baseplate		43.00 / [2.63]		cm^3/[in^3]
		Flangeless baseplate		35.56 / [2.17]		
Weight	W			100 / [3.53]		g/[oz]
Pin material		C145 copper, ½ hard				µin
Underplate		Nickel	50		100	
Pin finish		Pure matte tin, whisker resistant chemistry	200		400	
Assembly						
Storage temperature	T_{ST}		-65		125	°C
ESD rating	HSM	Method per Human Body Model Test JEDEC JESD22-A114C	CLASS 1C			V
	CDM	Charged Device Model Test JEDEC JESD22-C101C				
Reliablity						
MTBF		Calculated per Telcordia TR-NT-000332, 25°C		3.58		MHrs
		Telcordia Issue 2 - Method I Case 3; 25°C Ground Benigh, Controlled				
Safety						
Isolation voltage	V_{HIPOT}	IN to OUT	**4,242**			V_{DC}
		IN to CASE	**2,121**			
		OUT to CASE	**2,121**			
Agency Approvals						
Agency approvals/standards		EN 60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

Environmental Qualification

Test Description	Test Detail
HALT (Highly Accelerated Life Testing)	EIAJESD22-A110-B
Fungus	MIL-STD-810F Method 508.5, section II
Salt Fog	MIL-STD-810F Method 509.4
Solderability	MIL-STD-202G Method 208H
Terminal Strength	MIL-STD-202G Method 211A, condition A
Acceleration	MIL-STD-202G Method 211A, condition A
Altitude	MIL-STD-810F Method 500.2, procedures I & II
Explosive Atmosphere	MIL-STD-810F Method 511.4, procedure I, operational
High Temperature Operating Life (HTOL)	Vicor internal reference EIAJESD22-A110-B
Humidity	MIL-STD-810F Method 507.4, 95% Relative Humidity
Mechanical Shock	MIL-STD-810F, Method 516.5 Procedure I, MIL-S-901D lightweight hammer shock, MILSTD-202F, Method 213B
Random Mechanical Vibration	MIL-STD-810F, Method 514.5, Procedure I, Category 14, MIL-STD-810F, Method 514C, general minimum integrity
Resistance to Solvents	MIL-STD-202G, Method 215K
Temperature Humidity Bias	JESD22-A101-B, 1000hrs
Temperature Cycle	JESD22-A104-B
Thermal Shock	MIL-STD-202G, Method 107G, Condition

Pin Functions

+IN, -IN
Input power pins. -IN is the reference for all control pins, and therefore a Kelvin connection is recommended to reduce effects of voltage drop due to -IN currents.

+OUT, -OUT
Output power pins.

PC (Primary Control)
This pin enables and disables the converter; when held low the unit will be disabled. It is referenced to the -IN pin of the converter. The PC pin has an internal pull-up to V_{DD_INT} through a 10 kΩ resistor.

- Output enable: When PC is allowed to float above the enable threshold, the module is enabled. If leave PC floating, it is pulled up to V_{DD} and module will be enabled.
- Output disable: PC may be pulled down externally in order to disable the module.

FT (Fault)
The FT pin provides a Fault signal. Anytime the module is enabled and has not recognized a fault, the FT pin is inactive. Whenever the powertrain stops (due to a fault protection or disabling the module by pulling PC low), the FT pin becomes active and provides current to drive an external circuit. The FT pin becomes active momentarily when the module starts up.

When active, FT pin drives to V_{DD}, with up to 5 mA of external loading. Module may be damaged from an over-current FT drive, thus a resistor in series for current limiting is recommended.

Remote Sense (+S, -S)
The Remote Sense pins sense the voltage at the load and adjusts the converter output voltage to compensate for the voltage drop in the leads/traces. The sense leads of the module must always terminate either directly to the output pins (local sense) or at the load (remote sense).

VDD
3.3 V regulated voltage for external ancillary circuits.

VDDB
Semi-regulated voltage for future products.

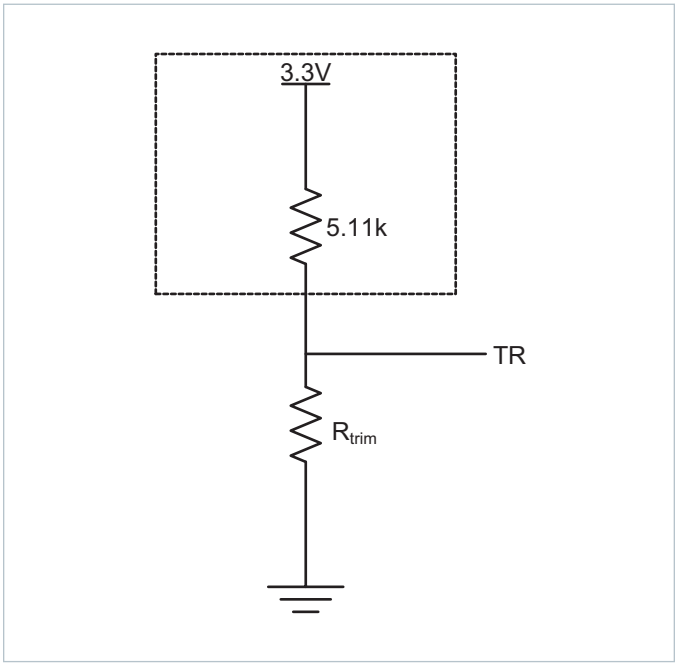
TR (Trim)
The TR pin is used to select the trim mode and to trim the output voltage of the converter. The TR pin has an internal pull-up to V_{DD_INT} through a 5.11 kΩ resistor.

The converter shall latch trim behavior at application of V_{IN}, and persist in that same behavior until loss of input voltage.

- At application of V_{IN}, if TR is sampled at above $V_{TRIM-DIS}$, the module shall latch in a non-trim mode, and will ignore the TR input for as long as V_{IN} is present.
- At application of V_{IN}, if TR is sampled at below $V_{TRIM-EN}$, the TR will serve as an input to control real time output voltage trim. It will persist in this behavior until V_{IN} is no longer present.

If trim is active, the TR pin provides dynamic trim control at a typical 500 Hz of -3dB bandwidth over the output voltage. V_{OUT} set point under full load and room temperature can be calculated using the equation below:

$$V_{OUT} = \left[1 + 0.171 \bullet \left(\frac{3.3 \bullet R_{trim}}{5110 + R_{trim}}\right) - 0.425\right] \bullet V_{OUT\_NOM}$$



$$R_{trim} = \frac{1{,}277{,}500 \bullet (-40\ V_{OUT} + 23\ V_{OUT\_NOM})}{10{,}000\ V_{OUT} - 11{,}393\ V_{OUT\_NOM}}$$

FB (Feedback)
The FB pin produces PWM pulses whose duty cycle is maintained by the internal Digital Supervisor to regulate the output voltage. This pin will be used for paralleling modules to create high current/power arrays in the future.

SGND
Signal ground for referencing all control circuitry.

Soft Start
The first time the HDC starts after application of input voltage, it will go through a soft start sequence. Notice that the module will only startup if input voltage is inside the range of $V_{IN-FULL-POWER}$. After startup, the module can then operate in the entire VIN range.

This soft start sequence permits initial startup into a completely discharged load capacitance. The soft start sequence ramps the output voltage by modulating the internal error amplifier reference.

This causes the output voltage to approximate a piecewise linear ramp. The output ramp finishes then the voltage reaches either the nominal output voltage or the trimmed output voltage in cases where trim mode is active.

An HDC recovering from any fault condition does not assume that the output capacitance has remained charged. Just as with its initial startup sequence when V_{IN} is first applied, it will again execute the soft start ramp.

Output Current Limit

The HDC features a fully operational current limit which effectively keeps the module operating inside the Safe Operating Area (SOA) for all valid trim and load profiles. The current limit approximates a "brick wall" limit, where the output current is prevented from exceeding the current limit threshold by reducing the output voltage via the internal error amplifier reference. Output Overload protection threshold is typically 105% of maximum output current, and can vary from 100% to 120% of maximum output current.

When the output current exceeds the current limit threshold, current limit action is postponed by 1ms, which permits the converter to momentarily deliver higher peak output currents to the load. Peak output power during this time is still constrained by the internal Power Limit of the module. The fast Power Limit and relatively slow Current Limit work together to keep the module inside the SOA. Delaying entry into current limit also permits the converter to minimize droop voltage for load steps. Sustained operation in current limit is permitted, and no derating of output power is required in an array. Some applications may benefit from well matched current distribution, in which case fine tuning sharing via the trim pins permits control over sharing. The converter does not require this for proper operation, due to the power limit and current limit behaviors described here. Current limit can reduce the output voltage to as little as the UVP threshold ($V_{OUT-UVP}$). Below this minimum output voltage compliance level, further loading will cause the module to shut down due to the output undervoltage fault protection.

Line Impedance and Output Stability Requirements

Connect a high-quality, low-noise power supply to the +IN and –IN terminals. The interconnect cables can be up to 1 meter long each way, and up to 0.1 m apart between each other. Additional capacitance may have to be added between +IN and –IN to make up for impedances in the interconnect cables as well as deficiencies in the source. Significant source impedance can bring system stability issue for a regulated DC-DC converter and needs to be avoided or compensated.

Make sure input voltage slew rate dVin/dt is less than 1 V/us, otherwise a pre-charge circuit is required in the input side to control the charging slew rate. For the HDC, the output voltage stability is guaranteed as long as hold up capacitance C_{OUT} falls within the specified ranges.

Input Fuse Selection

The HDC is not internally fused, see safety approvals for required fusing.

Fault Handling

Input Undervoltage Fault Protection (UVLO)

The converter's input voltage is monitored to detect an input under voltage condition. If the converter is not already running, then it will ignore enable commands until the input voltage is greater than $V_{IN-UVLO+}$. If the converter is running and the input voltage falls below $V_{IN-UVLO-}$, the converter recognizes a fault condition, the powertrain stops switching, and the output voltage of the unit falls.

UVLO faults which are shorter than t_{UVLO} may not be detected by the fault sequence logic, in which case the converter may not respond. After a UVLO fault is detected by the fault sequence logic and the converter shuts down as a result, it will wait for the input voltage to rise above $V_{IN-UVLO+}$. Provided the converter is still enabled, the powertrain will again enter the soft start sequence.

Input Overvoltage Fault Protection (OVLO)

The converter's input voltage is monitored to detect an input over voltage condition. When the input voltage is more than the $V_{IN-OVLO-}$, a fault is detected, the powertrain immediately stops switching, and the output voltage of the converter falls.

After an OVLO fault occurs, the converter will wait for the input voltage to fall below $V_{IN-OVLO-}$. Provided the converter is still enabled, the powertrain will again enter the soft start sequence.

The powertrain controller itself also monitors the input voltage. Transient OVLO events which have not yet been detected by the fault sequence logic may first be detected by the controller, if the input slew rate is sufficiently large. In this case, powertrain switching will immediately stop. If the input voltage falls back in range before the fault sequence logic detects the out of range condition, the powertrain will resume switching and the fault logic will not interrupt operation Regardless of whether the powertrain is running at the time or not, if the input voltage does not recover from OVLO before t_{OVLO}, the converter fault logic will detect the fault.

Output Undervoltage Fault Protection (UVP)

The converter determines that an output overload or short circuit condition exists by measuring its primary sensed output voltage. In general, whenever the powertrain is switching and the primary-sensed output voltage falls below $V_{OUT-UVP}$ threshold, a short circuit fault will be registered. Once an output undervoltage condition is detected, the powertrain immediately stops switching, and the output voltage of the converter falls. The converter remains disabled for a time t_{FAULT} and then provided the converter is still enabled, the powertrain will again enter the soft start sequence after t_{INIT} and t^{ON}.

Temperature Fault Protections (OTP)

The fault logic monitors the internal temperature of the converter. If the measured temperature goes higher than $T_{INT-OTP}$, a temperature fault is registered. As with the undervoltage fault protection, once a temperature fault is registered, the powertrain immediately stops switching, the output voltage of the converter falls, and the converter remains disabled for a time t_{FAULT}. Then, the converter waits for the internal temperature to return to below $T_{INT-OTP}$ before recovering. Once recovered, provided the converter is still enabled, the HDC will again enter the soft start sequence after t_{INIT} and t_{ON}.

Output Overvoltage Fault Protection (OVP)

The converter monitors the primary sensed output voltage during switching to detect output OVP. If the primary sensed output voltage exceeds $V_{OUT-OVP}$, a fault is latched, the logic disables the powertrain, and the output voltage of the converter falls.

This type of fault is latched, and the converter will not operate until the latch is cleared. Clearing the fault latch is achieved by either disabling the converter via the PC pin, or else by removing the input power.

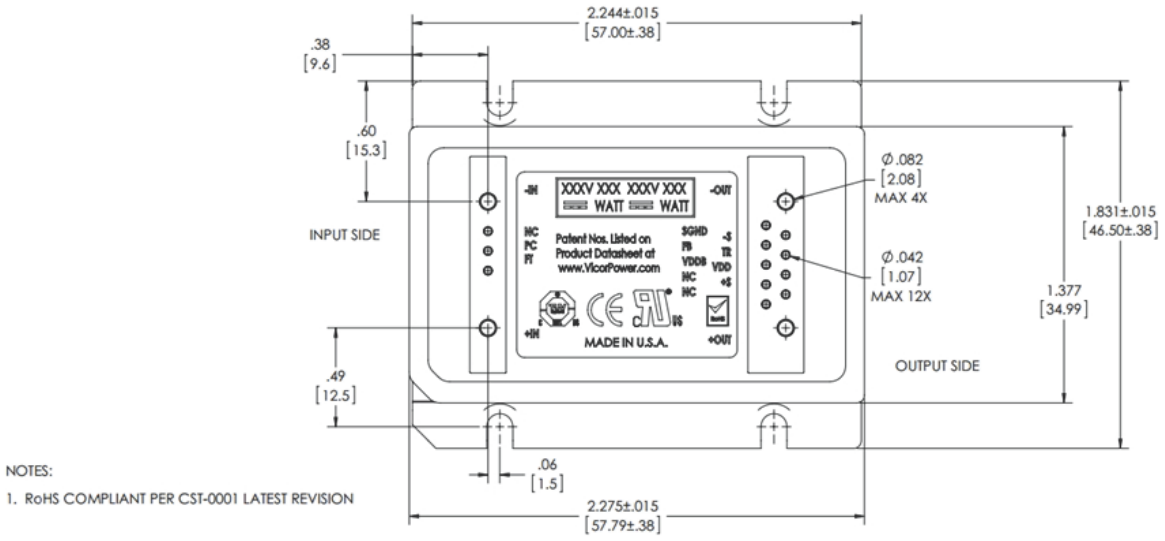
Burst Mode

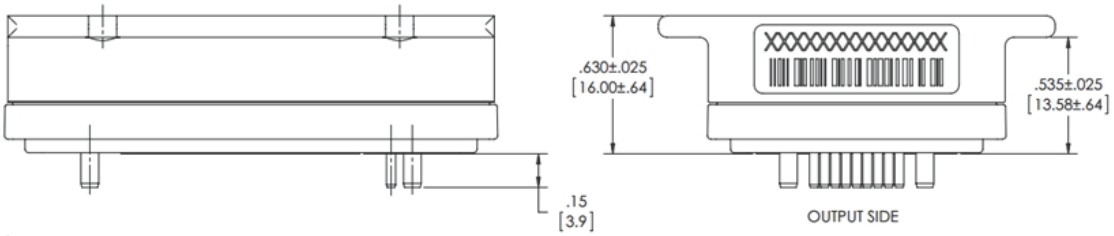
Under light loading conditions, the HD Converter may operate in burst mode depending on the line voltage. Burst mode occurs whenever the internal power consumption of the converter combined with the external output load is less than the minimum power transfer per switching cycle. To prevent the output voltage from rising in this case, the powertrain is switched off and on repeatedly to effectively lower the average switching frequency, and permit operation with no external load. During the time when the power train is off, the module internal consumption is significantly reduced, and there is a notable reduction in no-load input power in burst mode.

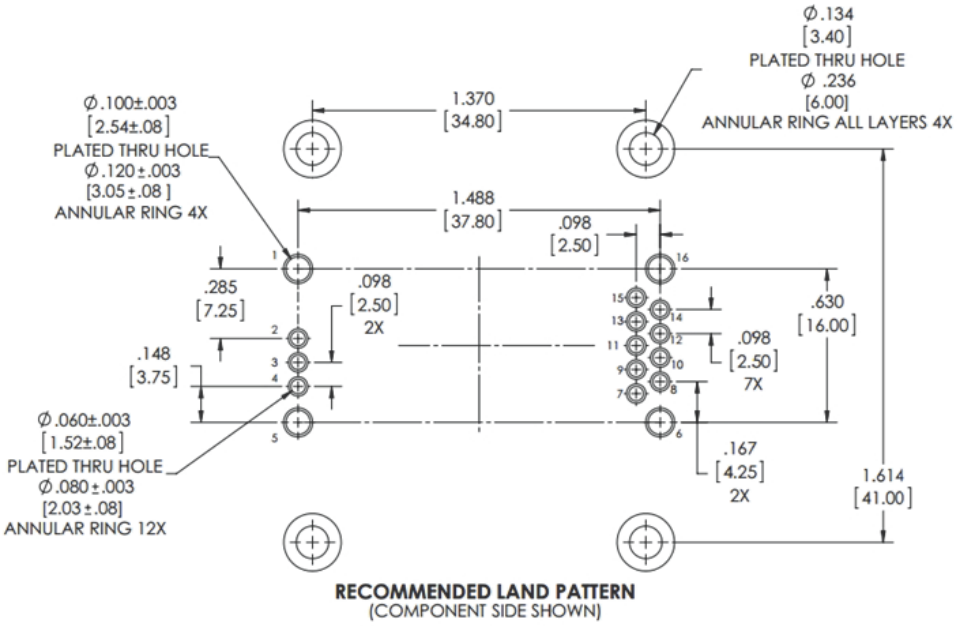
Pin Solderability

Please refer to the Soldering Methods and Procedures for Vicor Power Modules application note for guidance on soldering the HDC module to printed circuit boards. The application note can be found at: www.vicorpower.com/documents/application_notes/an_powermodulesoldering.pdf

Mechanical Drawings

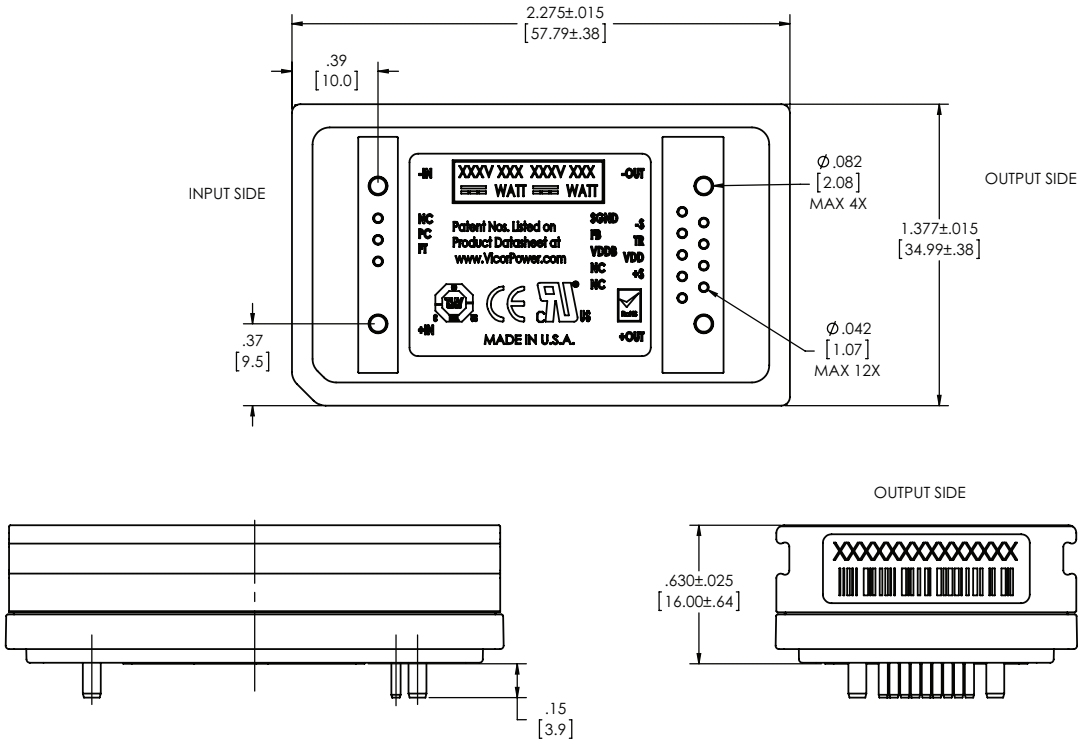






Flanged baseplate

Mechanical Drawings (Cont.)



Flangeless baseplate

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