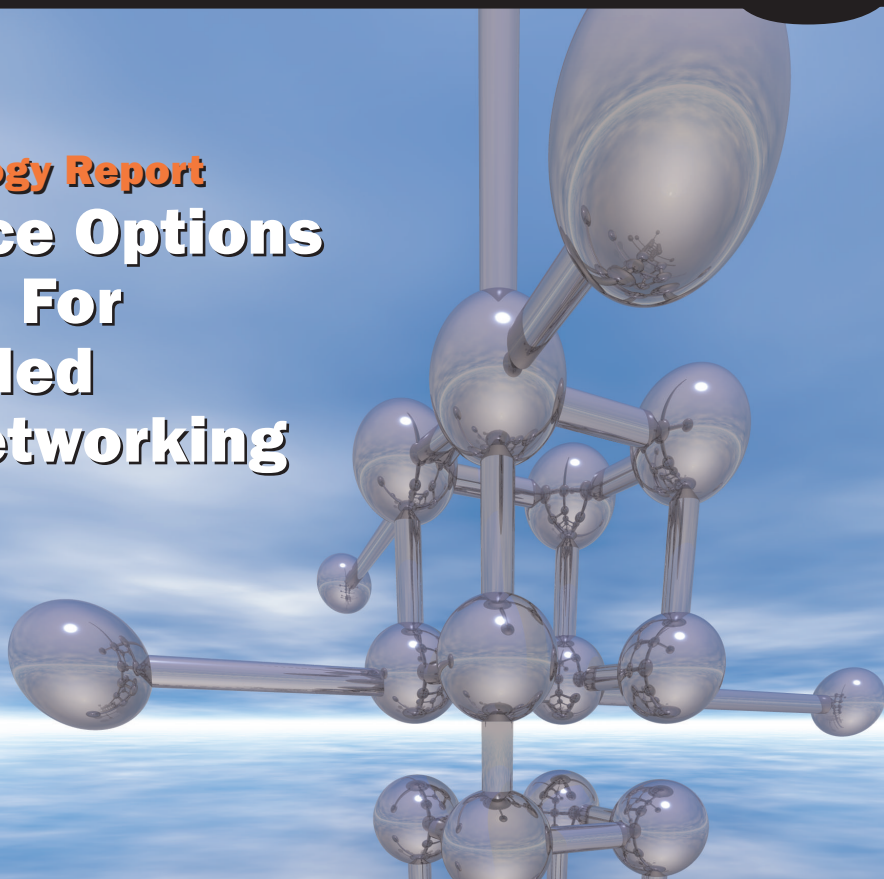
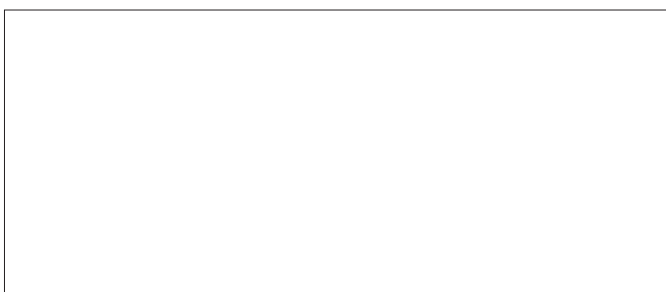


electronic design

45 Technology Report
Interface Options
Abound For
Embedded
MCU Networking



- 40: LEAPFROG: INDUSTRY FIRST**
Distributed Power: Novel Architecture
Yields New DC-DC Building Blocks
- 53: DESIGN VIEW:**
DDR Memories Place Tough
Demands On Voltage Regulators
- 55: DESIGN BRIEFS:**
Simple High-Efficiency
Current Source Is Adjustable



DISTRIBUTED POWER: NOVEL ARCHITECTURE YIELDS NEW DC-DC BUILDING BLOCKS

David G. Morrison /// ANALOG/POWER EDITOR

BGA-style dc-dc building blocks implement a new distributed power architecture that promises higher performance and lower cost. • Bricks and SIPs, more generically known as dc-dc converters, have long been the basic building blocks of distributed power

architectures. Over time, the performance of these modules has been improved to meet a variety of system demands for higher efficiencies and current densities, smaller packages, and lower cost. At the same time, architectural refinements, like the intermediate voltage bus, have helped designers deal with the increasing number of supply voltages, faster load transients, and falling supply voltages.

But as system requirements continue to become more challenging, conventional distributed power architectures and existing dc-dc converters may have great difficulty keeping up with system demands. Vicor has responded by redrawing the distributed power scheme into what it calls the Factorized Power Architecture (FPA). This new approach to distributed power takes the basic power-conversion functions— isolation, voltage conversion, regulation, and EMI suppression— and re-orders them within novel IC-style devices. The effect is significantly improved electrical performance, greater reliability, and lower cost. These benefits accrue from the performance of the power devices employed as well as from the inherent flexibility of the new architecture.

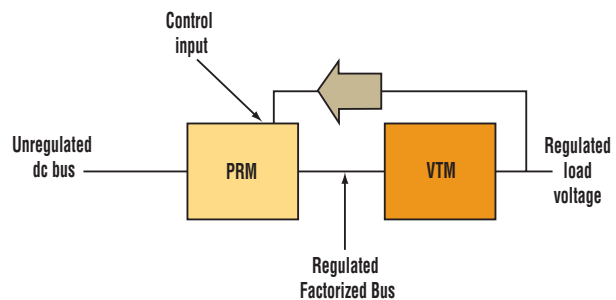
The company implemented FPA as a family of BGA-style devices called V•I Chips. These chips include two functional types—a preregulator module (PRM) and a voltage transformation module (VTM). The PRM takes an unregulated high-voltage bus, such as the 48-V bus found in telecom systems, and produces a regulated output at or near the nominal value of the input voltage. This regulated supply is called the *factorized power bus*. The VTM steps this bus voltage up or down with isolation to produce the voltage required at the load (Fig. 1).

The PRM and VTM may be operated open loop and still maintain a well regulated output. However, the output volt-

age may also be fed back to a control input on the PRM, which will then adjust PRM output to ensure tighter load regulation. The PRM accepts minimum inputs as low as 1.5 V and maximum inputs up to 400 V dc. But in practice, the input to an individual PRM is limited to a 5:1 voltage range within these extremes. The PRM's output, which is regulated but nonisolated, can assume a value from 0.5 V up to 400 V.

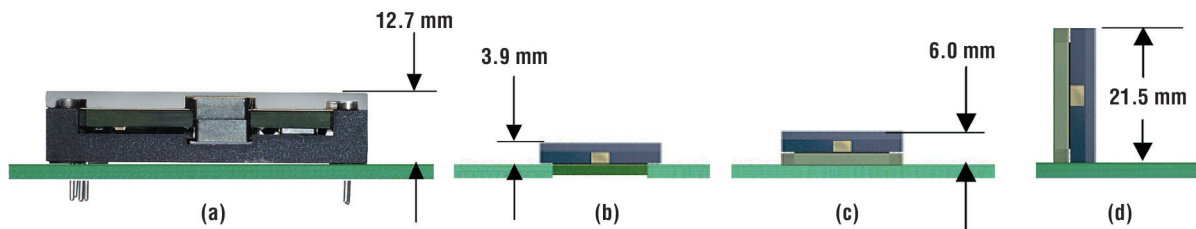
The PRM's input range accounts for 48-V battery-backed telecom systems, but it also covers the high-voltage dc output of an ac rectifier. When the input voltage is restricted to a 2:1 range, the PRM's conversion efficiency is 97% to 99%. A single PRM delivers as much as 200 W at 48 V dc.

Meanwhile, the VTM accepts a similarly wide range of voltages, in this case 2 to 400 V dc, and generates outputs from 0.5 to 400 V dc. In practice, the input voltage of a par-



1. In the FPA, a PRM produces a well-regulated high-voltage dc bus that can be distributed efficiently to one or more VTMs, which provide isolated voltage conversion with high efficiency, fast transient response, and low noise at the point of load.

INDUSTRY FIRST / DC-DC BUILDING BLOCKS



2. The FPA permits a quarter-brick dc-dc converter with through-hole mounting (a) to be replaced with a much smaller VTM mounted in-board, (b) on-board, (c) or even vertically (d) like a SIP. The PRM (not shown) can be remotely located.

ticular VTM is limited to a 2:1 range. In stepping up or down the factorized bus voltage, a single VTM provides 200 W or 80 A of output with a typical conversion efficiency of 92% to 96% or higher. This high efficiency is attributed to the part's high 3.5-MHz switching frequency. More detailed descriptions of FPA's underlying technology will be released later in the year.

Overall efficiency of the PRM-VTM combination from rectified ac input to low-voltage dc-output typically ranges from just below 90% to 95%. But under full-load conditions, it's possible to achieve overall efficiency exceeding 95%. That capability combined with the 0.846- by 1.260- by 0.236-in. BGA packaging of the two V•I Chips allows an FPA system to achieve power densities on the order of 400 W/in.³ Moreover, because the PRM produces a relatively high-voltage bus, which can be distributed with minimal I²R losses, the PRM may be mounted away from the load on a different pc board. At the point of load (POL), only the VTM need be present. Consequently, the POL power density can exceed 800 W/in.³

Those power densities reflect on-board mounting of the V•I Chips. In-board mounting options enable system-level power densities in excess of 500 W/in.³ and a POL power density greater than 1000 W/in.³ The latter value translates to a current density of nearly 500 A/in.³

For a direct comparison with a conventional dc-dc converter, consider that a leading-edge quarter brick may deliver 165 W (50 A at 3.3 V) in a 1.45- by 2.28- by 0.4-in. form factor. That translates to 125 W/in.³ Seen another way, a PRM-VTM two-chip solution with a smaller footprint and lower profile than a quarter brick will deliver 60 A at 3.3 V. At 2.5-V output, where quarter bricks now deliver up to 60 A, the PRM-VTM combination would offer 80 A (Fig. 2).

However, this limited comparison overlooks the flexibility and additional capabilities of FPA and the V•I Chips. Because of the low output impedance of the VTM (approximately 1 mΩ on units with low output voltages), the device's load regulation will be good (on the order of ±5%) even when the PRM and VTM operate open loop.

In closed-loop operation, where the output voltage is fed back to the PRM, load regulation improves to better than 1%. With voltage feedback, which allows for remote output voltage sensing, the PRM responds to changes in the load by adjusting its regulated output up or down, typically as much as 5%.

Therefore, it's possible to use a single PRM to power multiple VTMs with different voltage-transformation ratios, or

combine multiple PRMs and VTMs for independent voltage regulation on multiple outputs. It's also possible to parallel VTMs for higher current, or power VTMs off of existing dc-dc converters to generate a high-current POL. (For more on the different combinations, see "Mixing And Matching FPA Building Blocks" at www.elecdesign.com.)

The FPA approach offers an alternative to conventional brick-based distributed power schemes that duplicate isolation, voltage transformation, regulation, EMI filtering, and input protection at every point of load. Yet it also offers an alternative to the intermediate voltage bus architecture, where an isolated brick or bus converter feeds a series of nonisolated POL dc-dc converters. Because the intermediate voltage bus is at a low voltage (12 V or less), the bus converter will still need to be placed fairly close to the POLs, which is not a restriction with the FPA. Also, the lack of isolation in the POL converters makes overvoltage-sensitive loads more vulnerable to deadly faults and to potential ground loop problems. (For more, see "More Compact Than The Intermediate Voltage Bus" at www.elecdesign.com.)

The VTM's transient response opens up other possibilities. When faced with a 90% load step at 50 A/μs, the VTM can respond within 1.5 μs with a 5-μs settling time. Consequently, a PRM-VTM pair could replace a standard voltage regulator module (VRM) solution in some processor power applications. (For details, check out "V•I Chips May Challenge VRMs" online at www.elecdesign.com.)

By exploiting a zero-voltage switched and zero-current switched topology, the VTMs limit the common-mode and differential-mode noise at the point of load. For example, the output of a VTM configured to convert 48 V to 12 V exhibits about 50 mV p-p of high-frequency ripple. That noise voltage amounts to less than 0.5% of the dc output. This performance exceeds that of Vicor's low-noise bricks.

The FPA solution will be priced at about 14 cents/W per chip or 34 cents/A. Consequently, the PRM and VTM chips will each cost about \$25 in volume. The company expects to provide multiple sources for the V•I Chips through licensing agreements and electronic manufacturing service providers. VTM chips are now sampling in limited quantities, and sampling of PRMs is expected to begin in the third quarter. The earlier sampling of the VTMs will let customers take advantage of the VTMs in applications that require high-density POL converters as described above. **ED**

VICOR CORP.

www.vicr.com • Robert Marchetti, (978) 470-2900



DRILLDEEPER:

For more information:
www.elecdesign.com