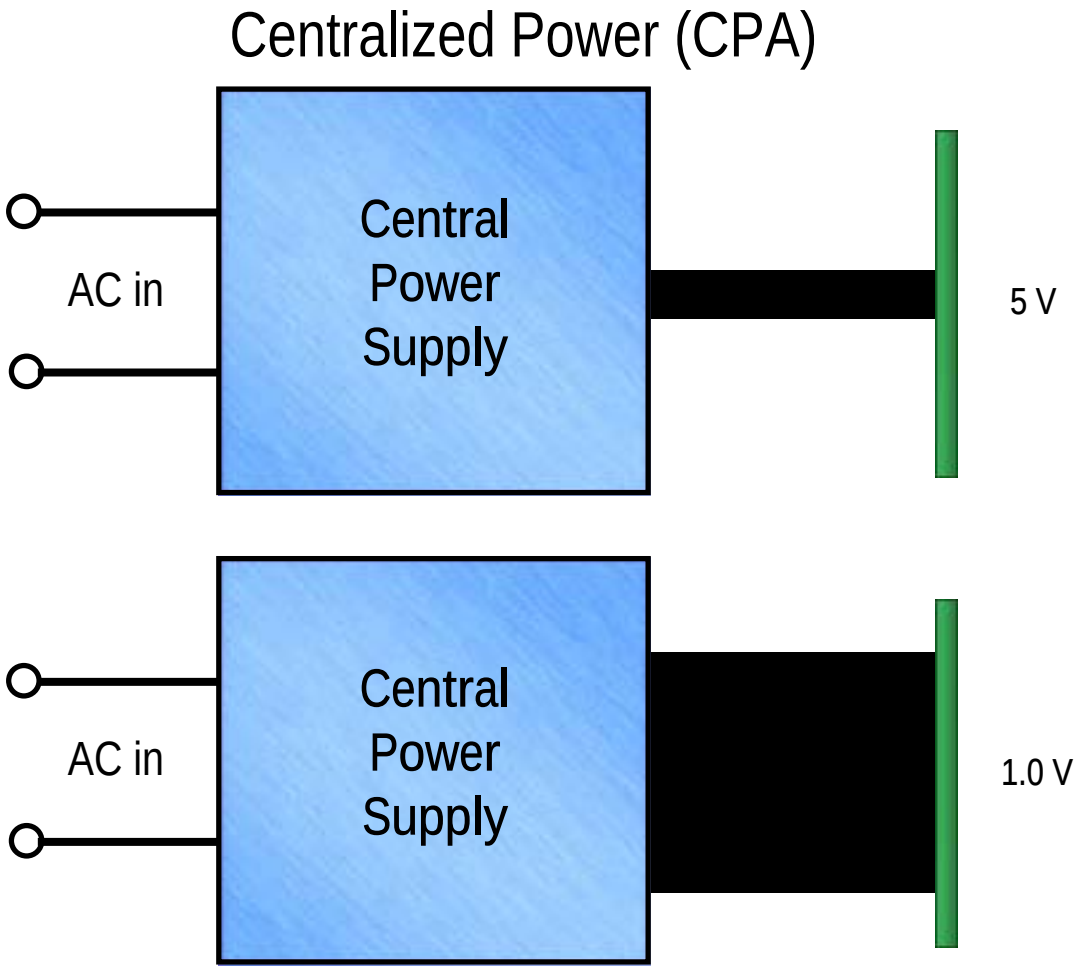
Factorized Power Architecture

New Engines for
Speed – Efficiency – Density

Quest for the Optimum Power Distribution Architecture

- Which power distribution architectures can efficiently support power systems from wall plugs, AC or DC outlets, through capacitors, super-capacitors or batteries, to processor cores – in the home, in the office, in the factory and everywhere in between?
  - Centralized Power Architecture (CPA)
  - Distributed Power Architecture (DPA)
  - Intermediate Bus Architecture (IBA)
  - Factorized Power Architecture (FPA)

Power Architecture Evolution



Centralized Power Architecture

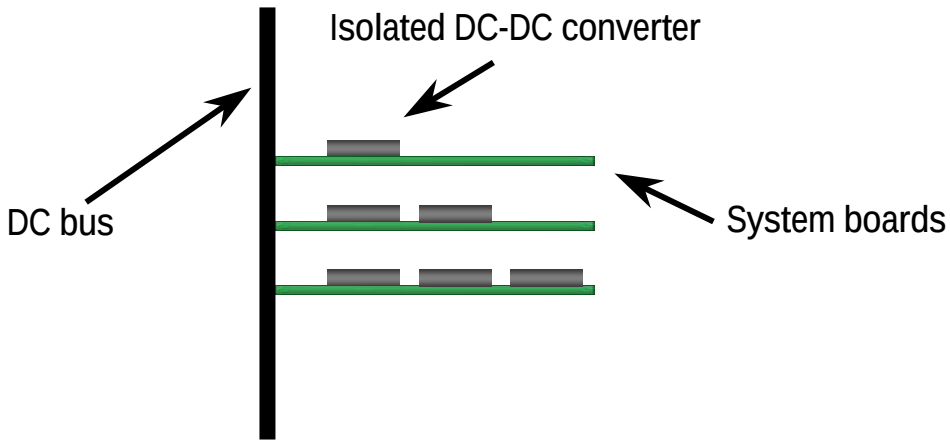
Centralized power remains pervasive in smaller systems due to its simplicity and low cost

- But is unable to efficiently deliver high currents at low voltages

Power Architecture Evolution

Centralized Power (CPA)

Distributed Power (DPA)



Distributed Power Architecture

Distributed power addresses architectural limitations of CPA

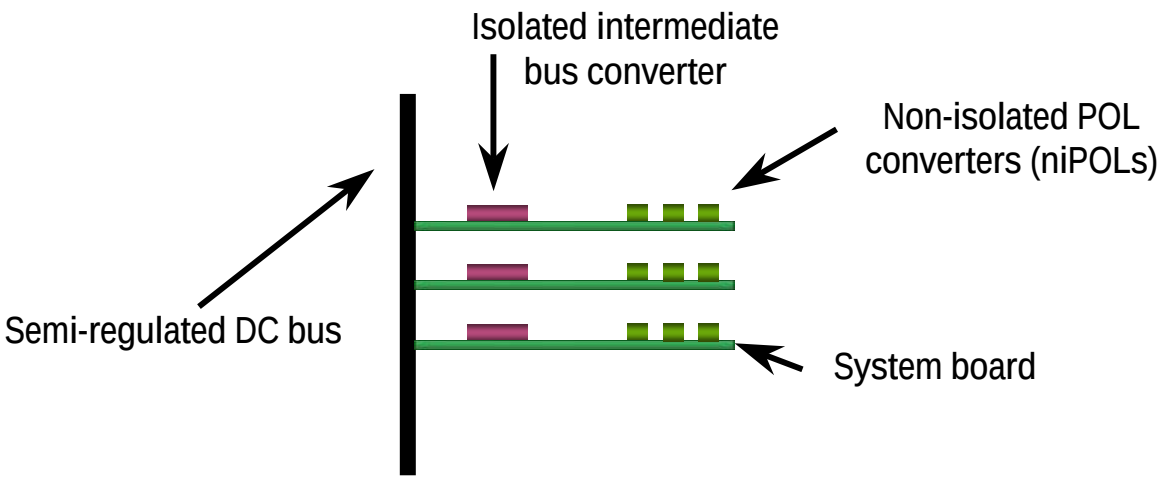
- Provides efficient power distribution at higher voltages
- Puts bricks at the Point of Load (POL)
- But DPA comes at a price
  - Board real estate
  - System cost

Power Architecture Evolution

Centralized Power (CPA)

Distributed Power (DPA)

Intermediate Bus (IBA)



Intermediate Bus Architecture

Intermediate bus deals with the proliferation of load voltages

- Puts inexpensive non-isolated buck converters at the POL
- But IBA is limited by
  - Inability to transform V and I
  - Having to decrease a duty cycle to reduce output voltage
  - Inductive inertia standing in the way of dynamic loads

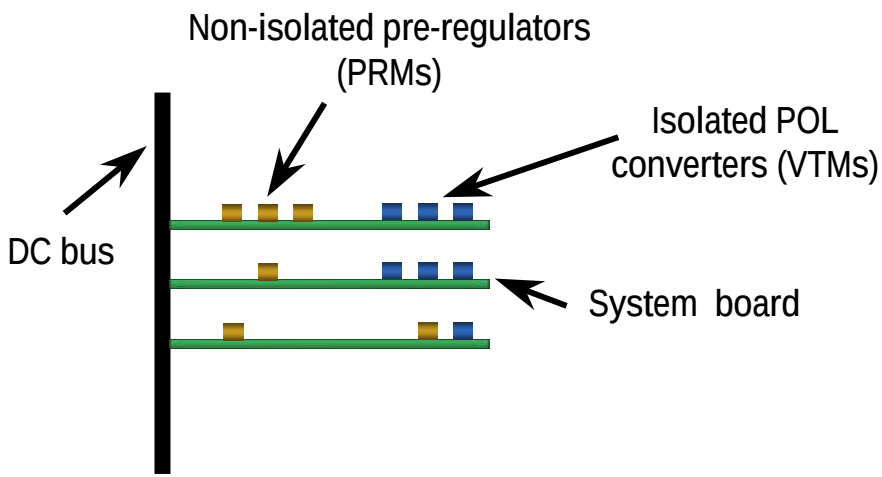
Power Architecture Evolution

Centralized Power (CPA)

Distributed Power (DPA)

Intermediate Bus (IBA)

Factorized Power (FPA)

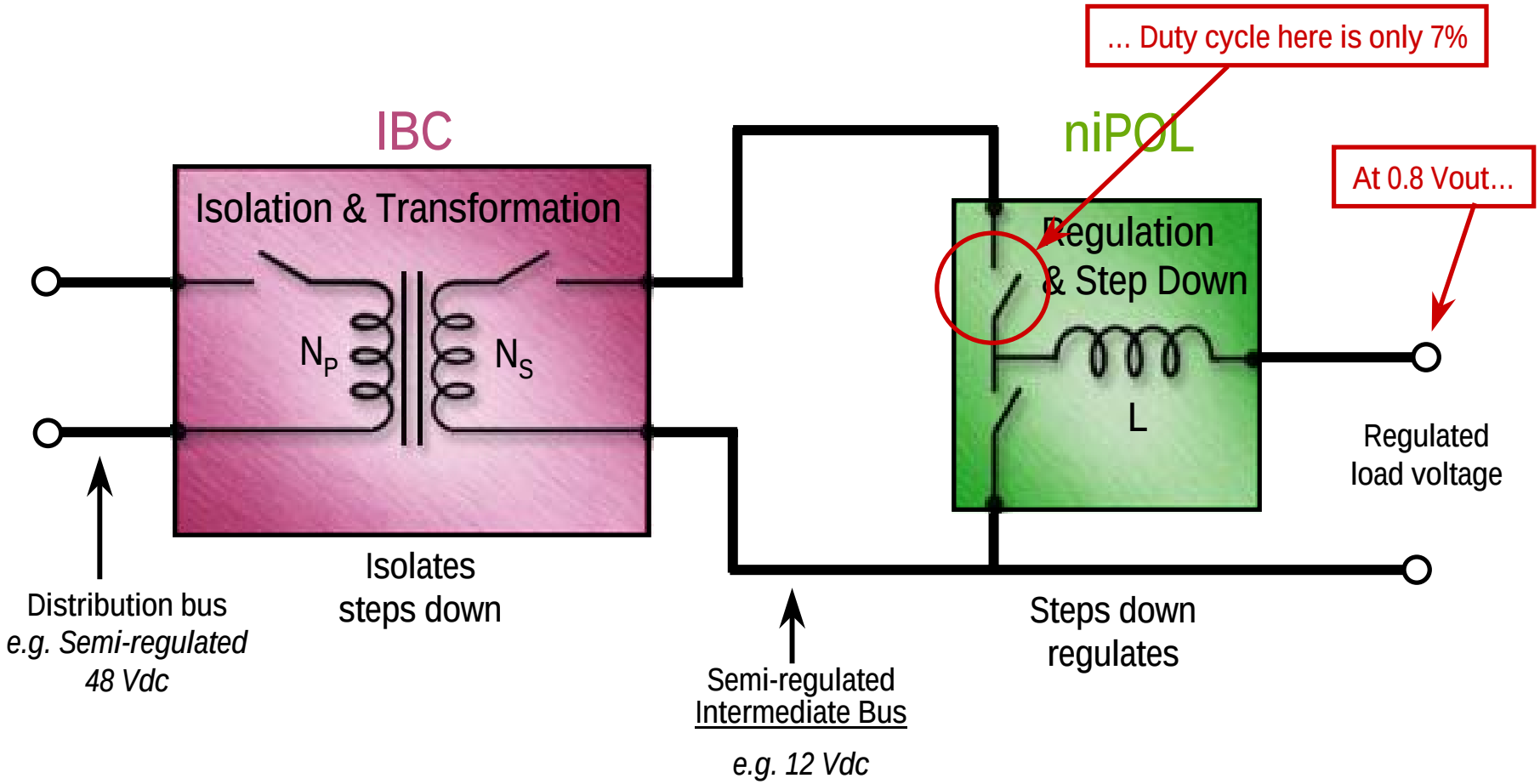


Factorized Power Architecture

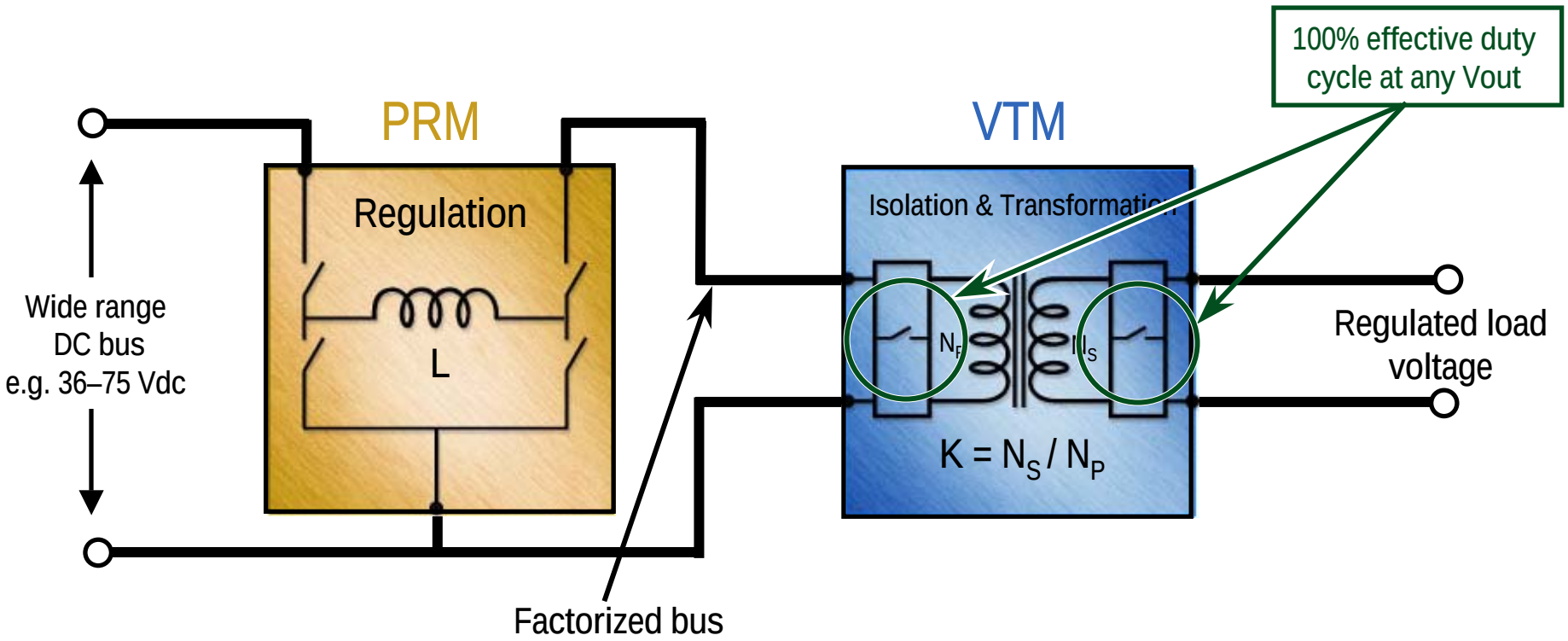
Factorized power addresses demanding POL current and voltage requirements:

- Puts a fast “current multiplier” at POL nodes
- Transforms V and I down to fractional POL voltages
- 100% effective duty cycle

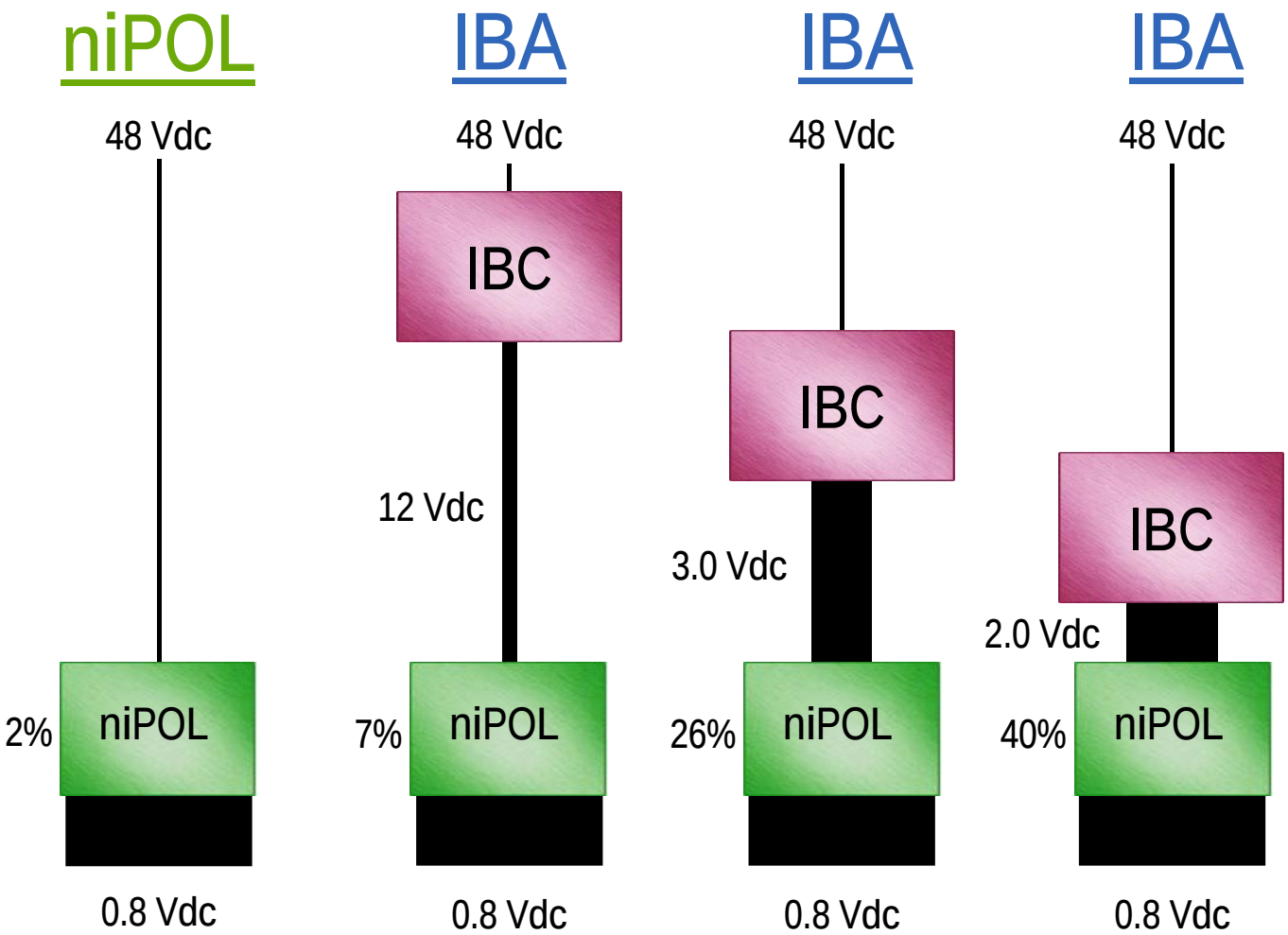
IBA – Inherent Duty Cycle Limitations



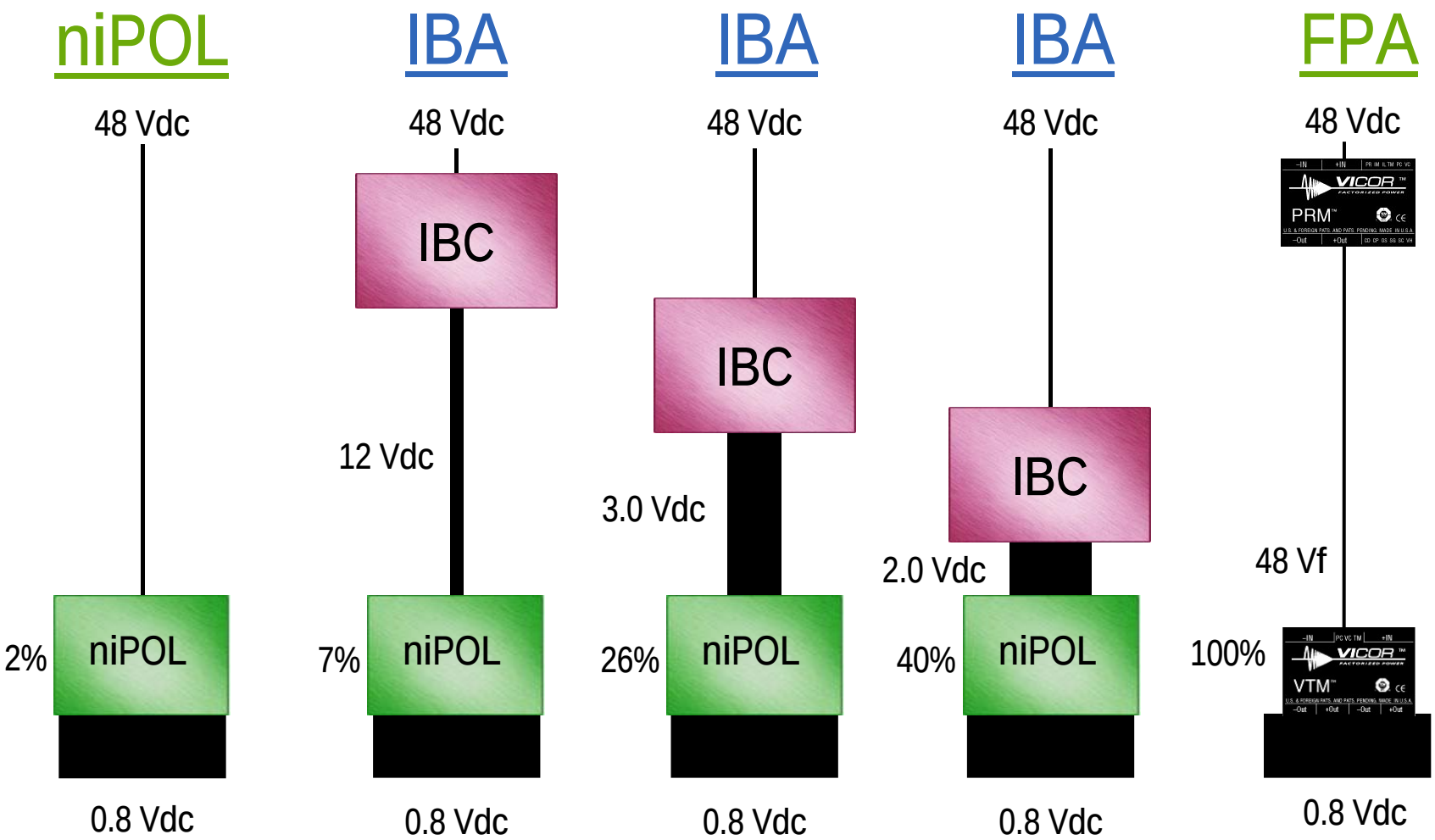
FPA – No Duty Cycle Limitations



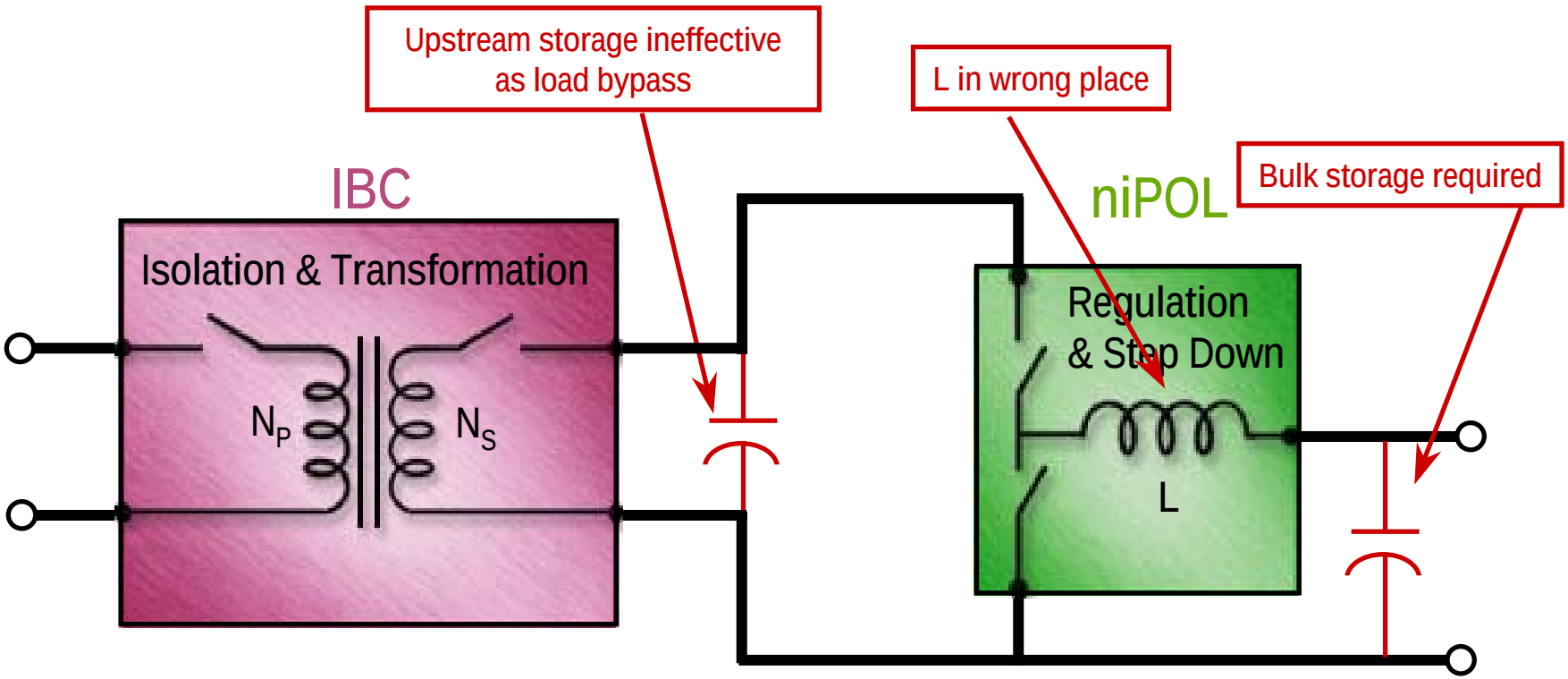
IBA – Inherent Step-Down Limitations



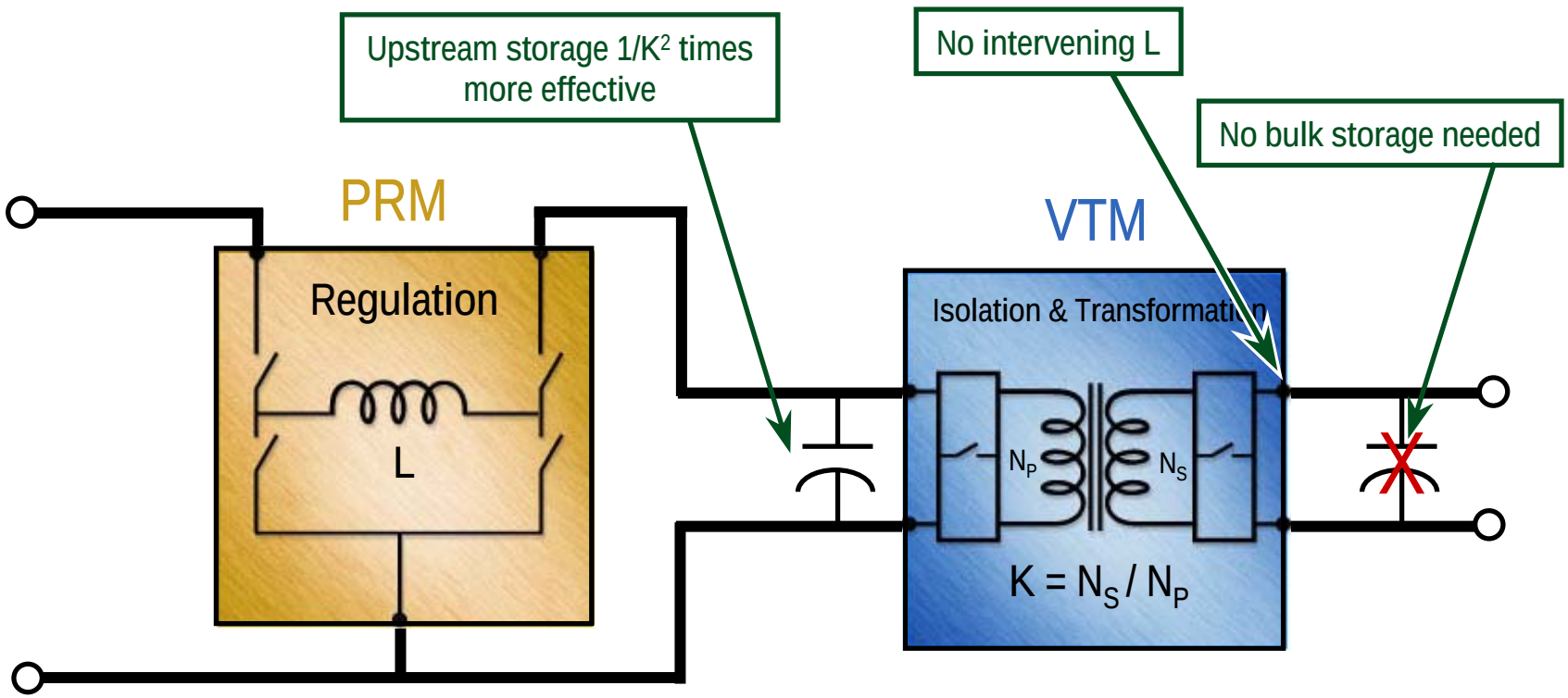
FPA – No Step-Down Limitations



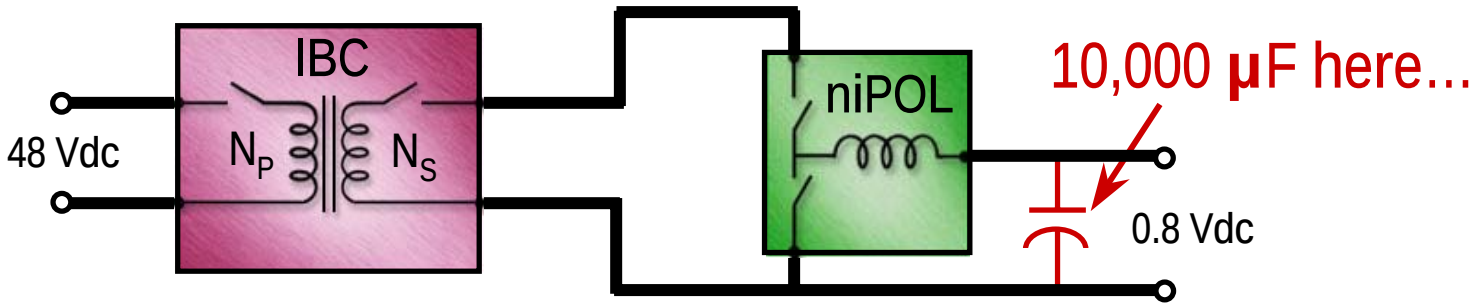
IBA – Inherent Energy Storage & Dynamic Response Limitations



FPA – No Energy Storage or Dynamic Response Limitations



Energy Storage in the Wrong Place



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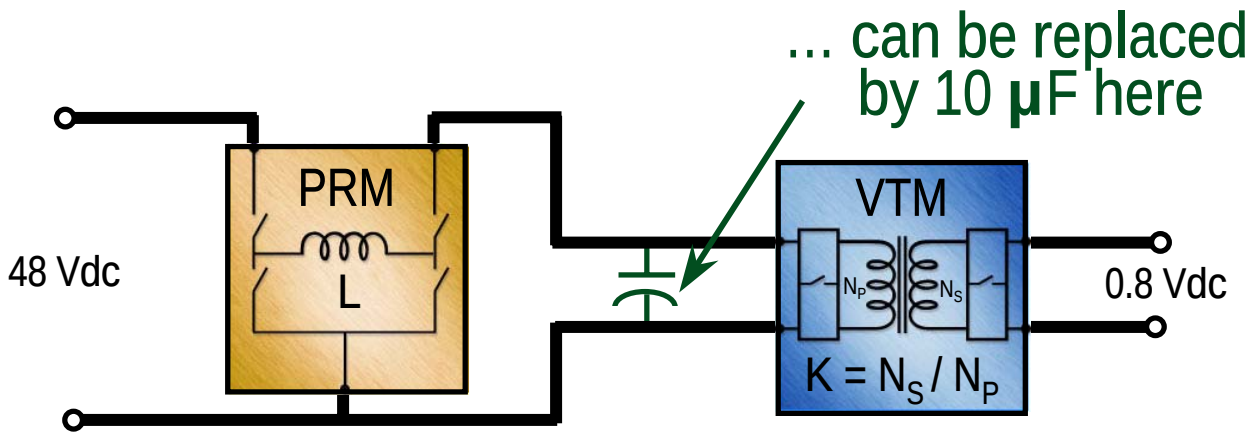


The Building Blocks of Factorized Power

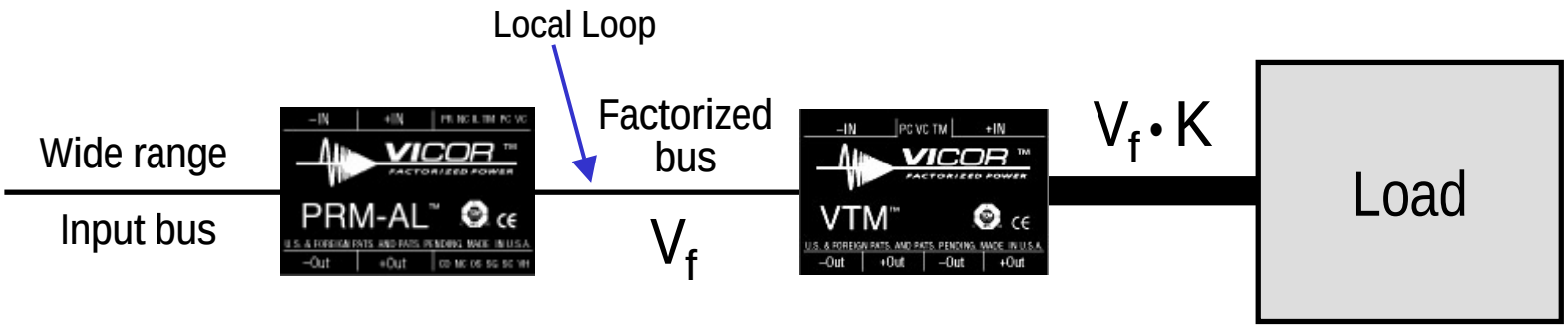
V•I Chips (VICs)

"Full VIC" ~ 1.0 in^2 surface mount package

PRM – Pre-Regulator Module

VTM – Voltage Transformation Module

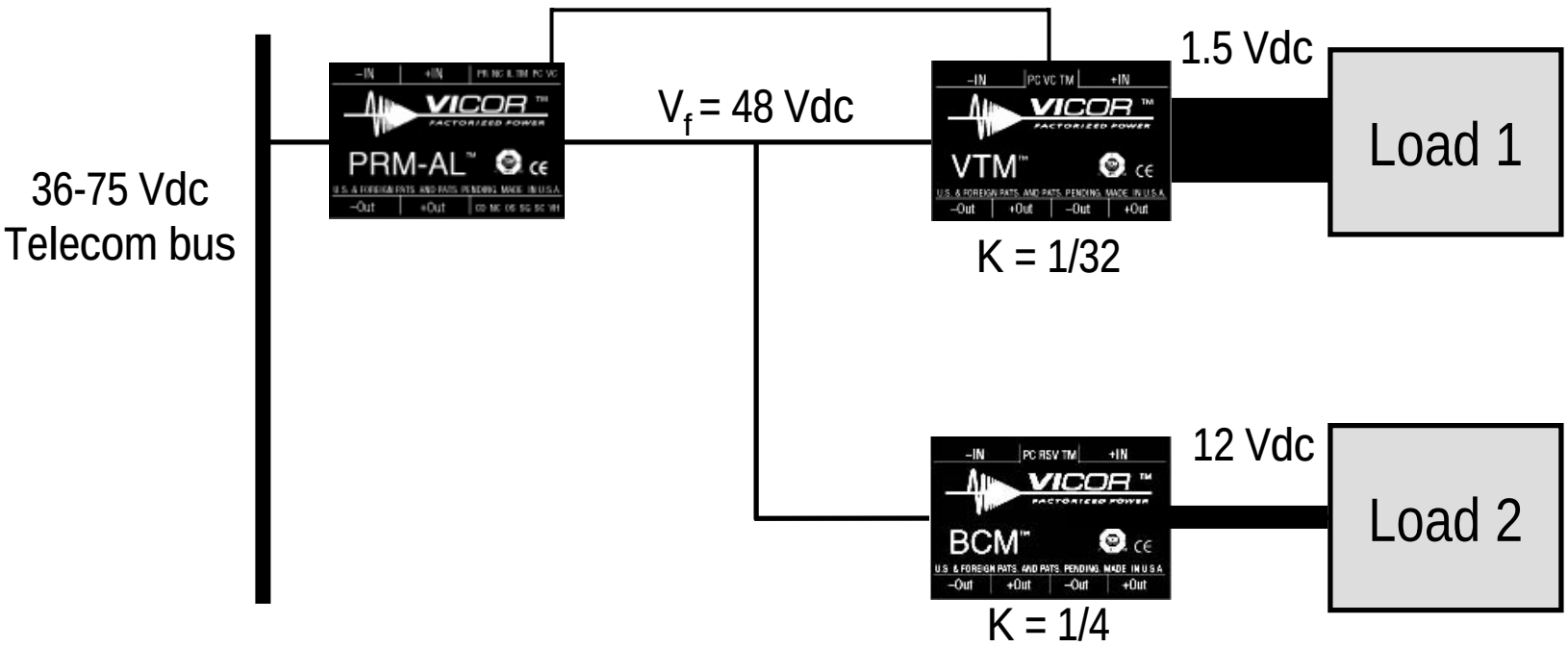
Basic FPA with PRM & VTM



- PRM controls the factorized bus voltage (V_f) to regulate the VTM output
- VTM transforms and isolates at the POL
- Combination: efficient distribution, regulation, transformation and isolation

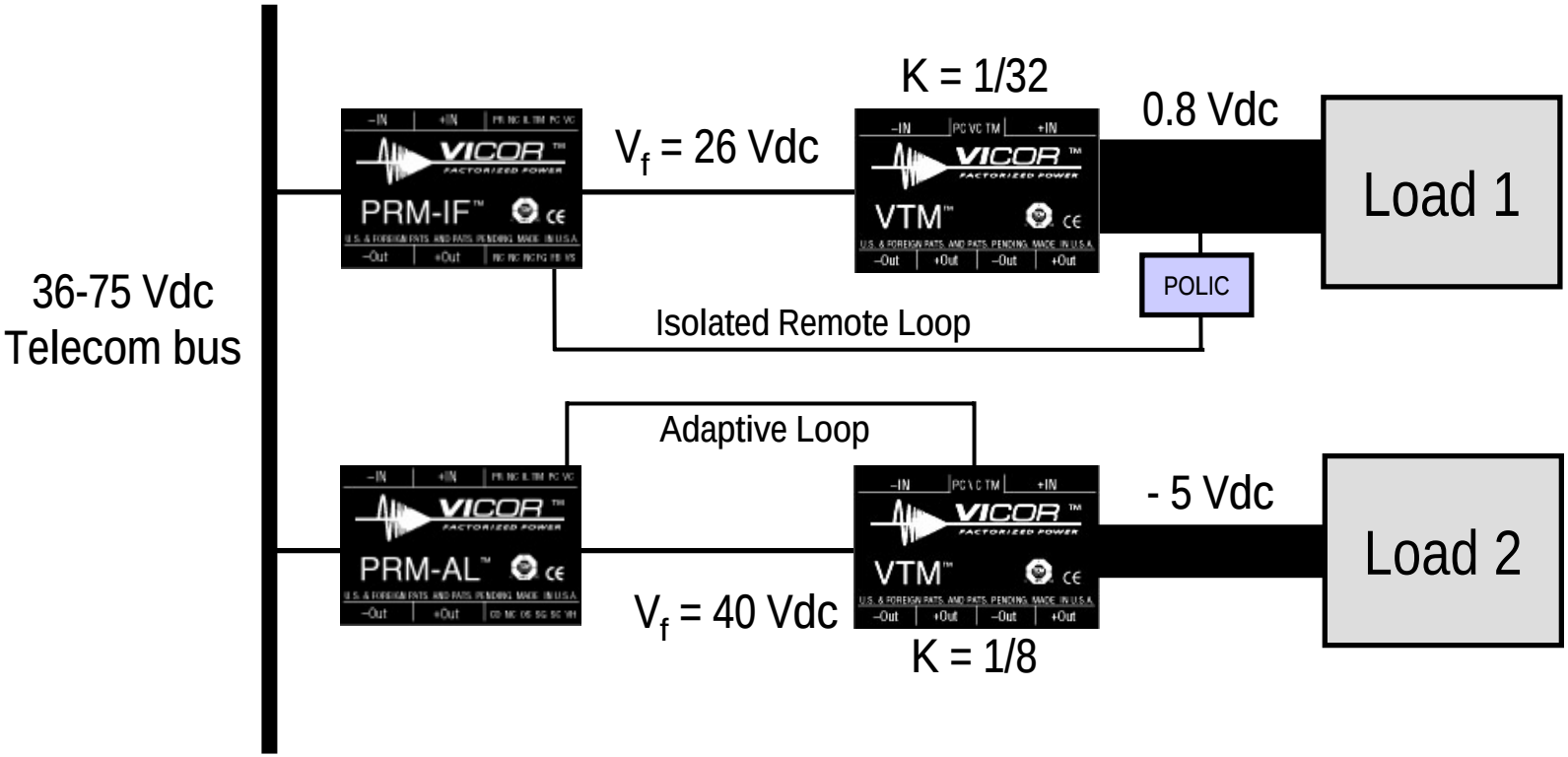
FPA Example

Adaptive Loop with PRM



FPA Example

Independently Regulated Outputs



Patents and Patents Pending

The Engine Under the Hood – PRM

“Full VIC” PRM Capabilities

- ZVS buck / boost regulator
- Input voltage: 1.5-400 V (up to 5:1 range)
- Step-up/step-down range: up to 5:1
- Output power: up to 300 W
- Conversion efficiency: up to 98%
- Frequency: up to 2 MHz

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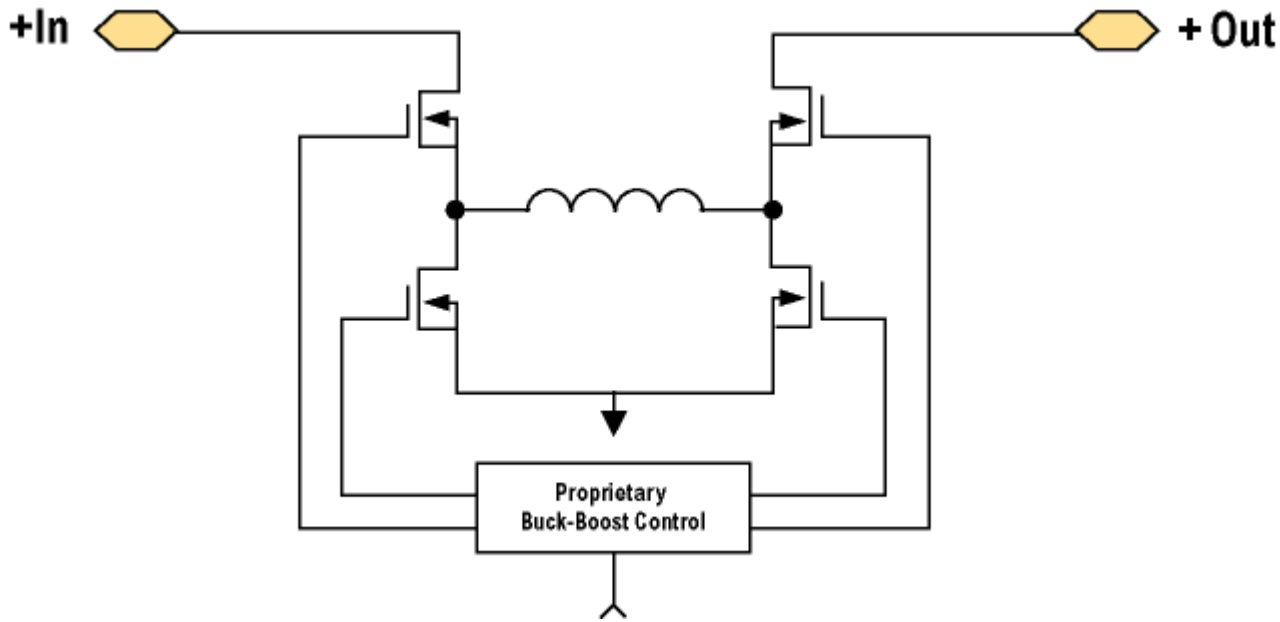
PRM – ZVS Buck/Boost Engine



- ZVS buck-boost topology and control architecture
- High frequency operation

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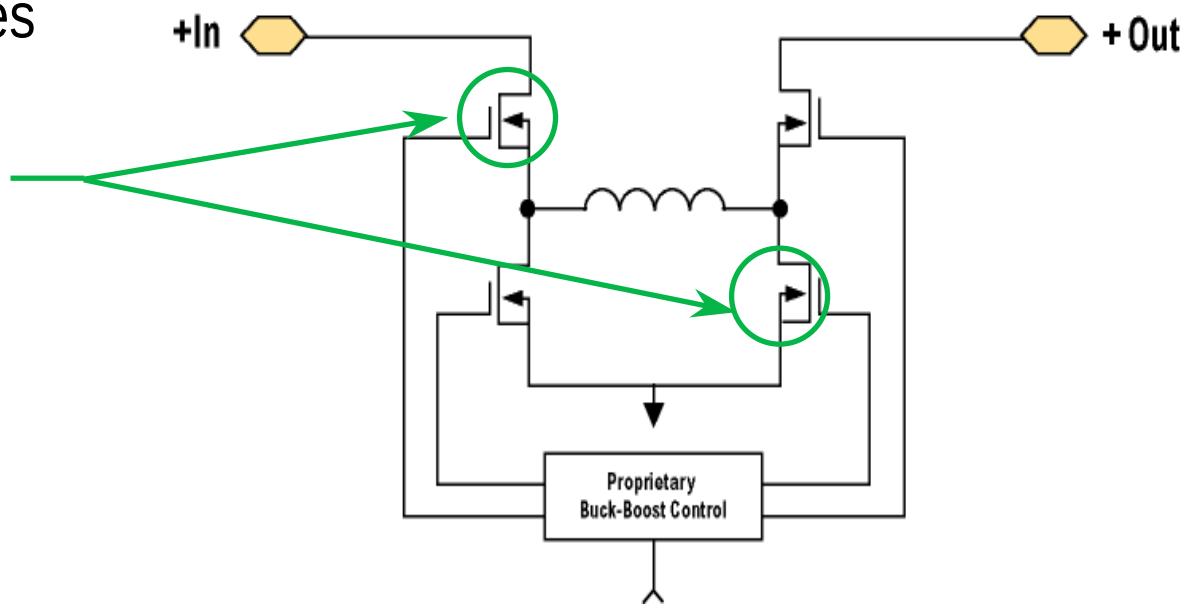
PRM Conduction Phases

- Power cycle comprises four conduction phases

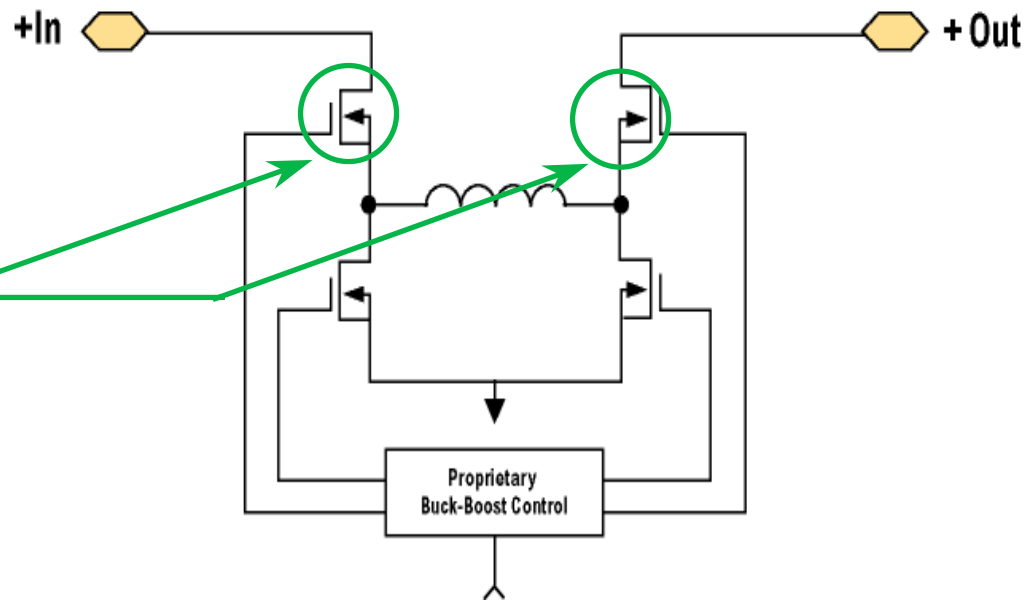
1. Input phase



PRM Conduction Phases

- Power cycle comprises four conduction phases

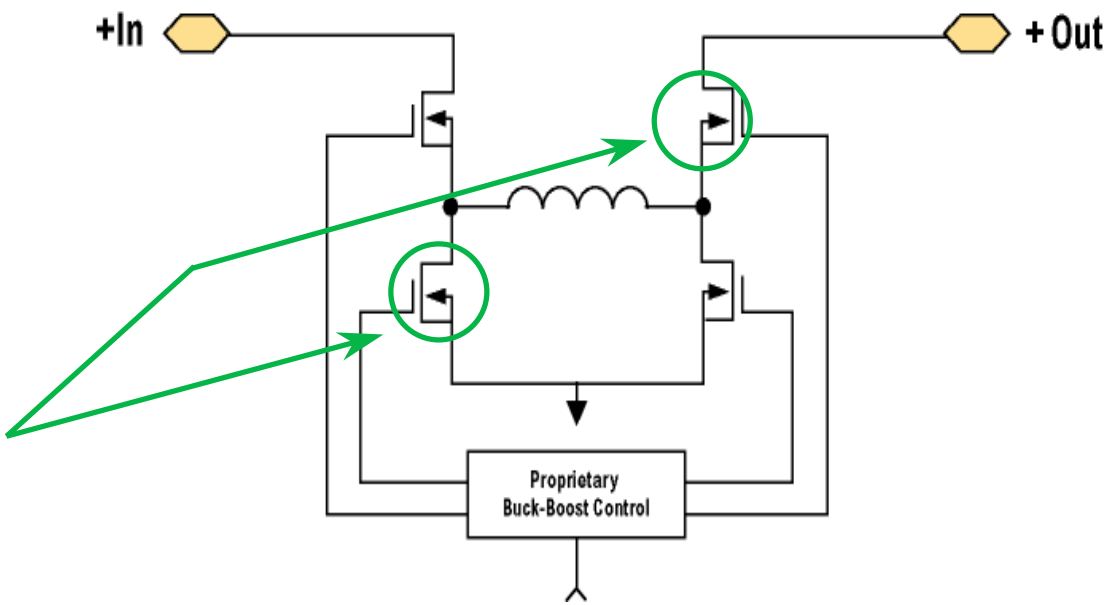
1. Input phase
2. Input-output phase



PRM Conduction Phases

- Power cycle comprises four conduction phases

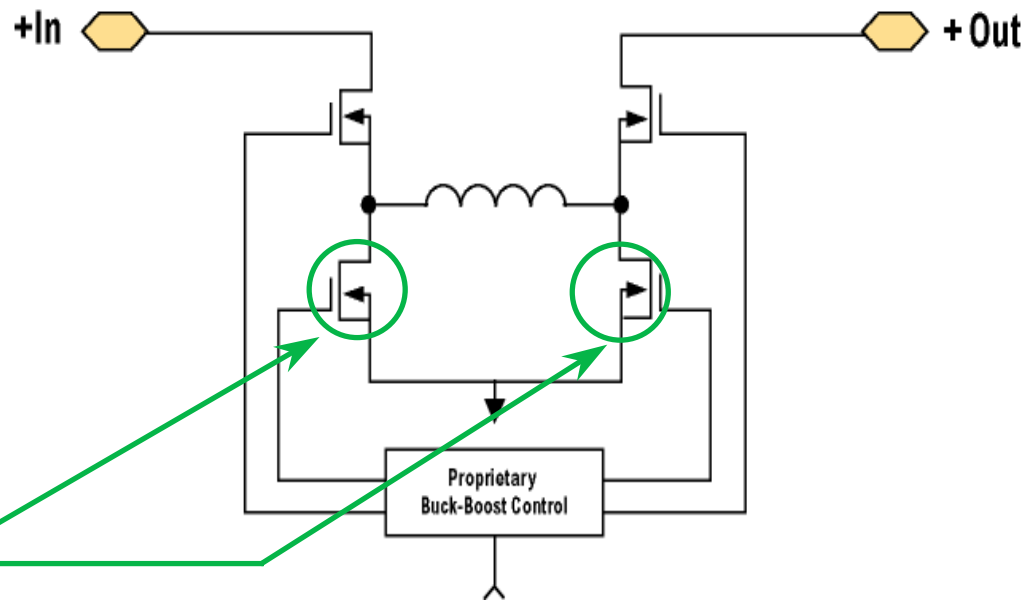
1. Input phase
2. Input-output phase
3. Free-wheeling phase



PRM Conduction Phases

- Power cycle comprises four conduction phases

1. Input phase
2. Input-output phase
3. Free-wheeling phase
4. Clamp phase



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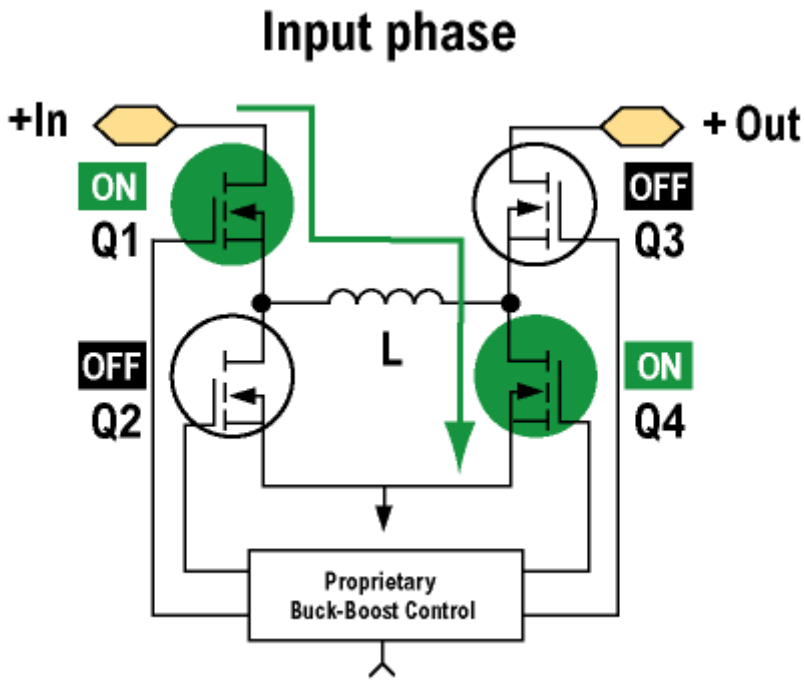

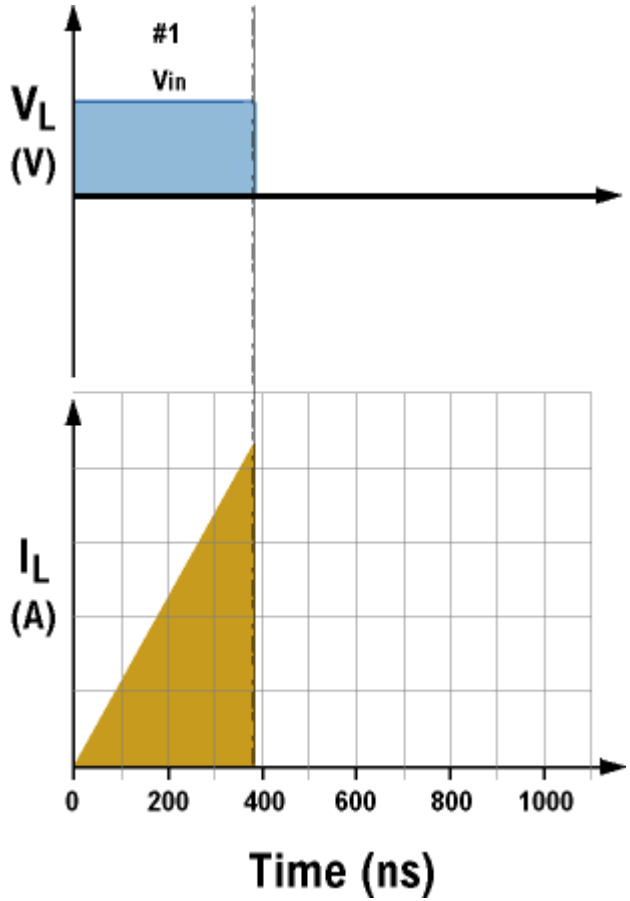

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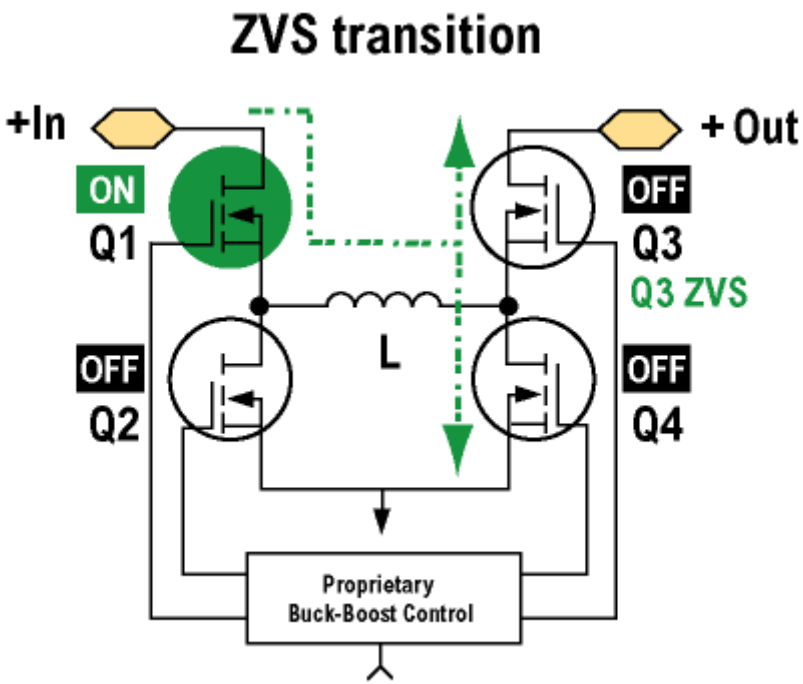

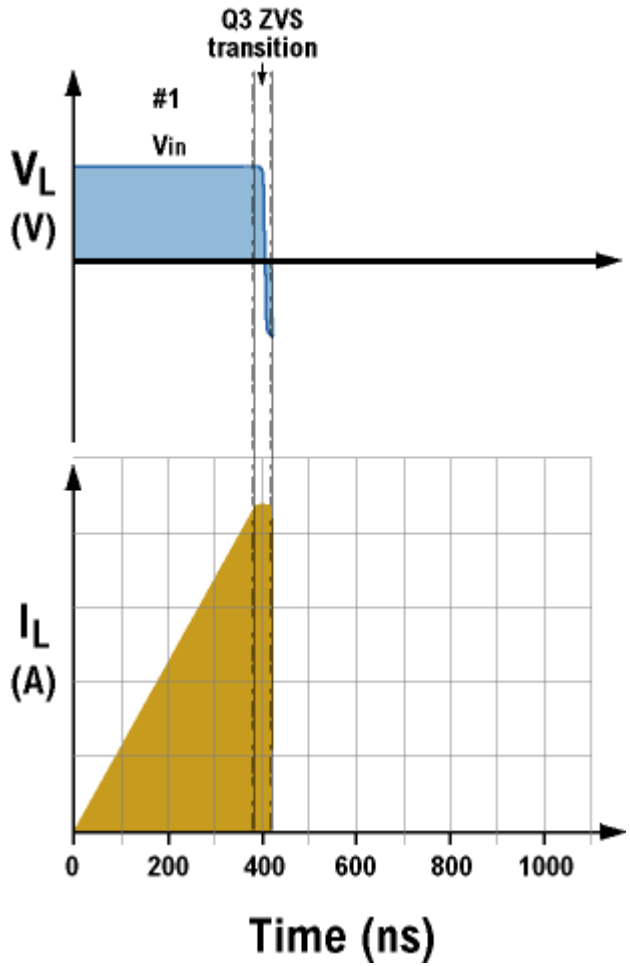

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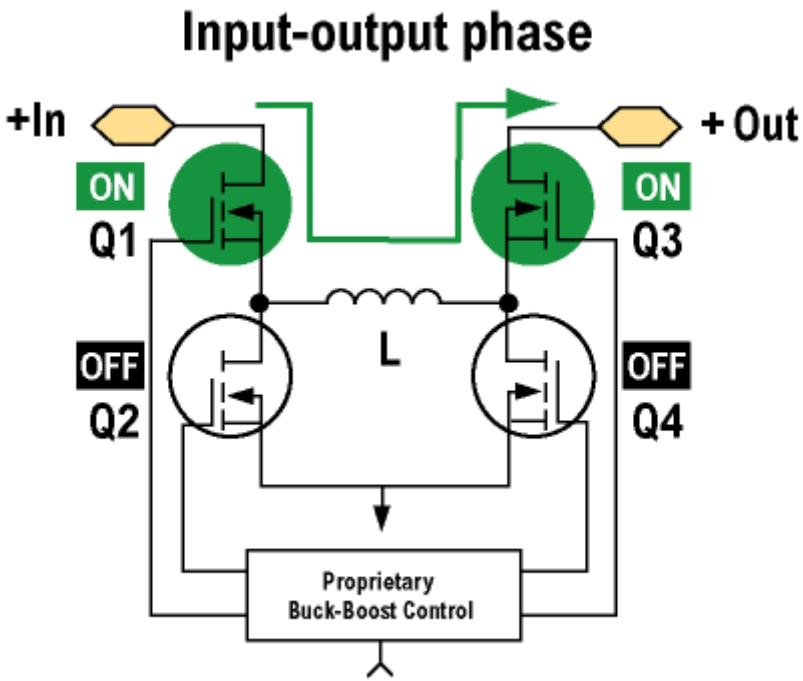

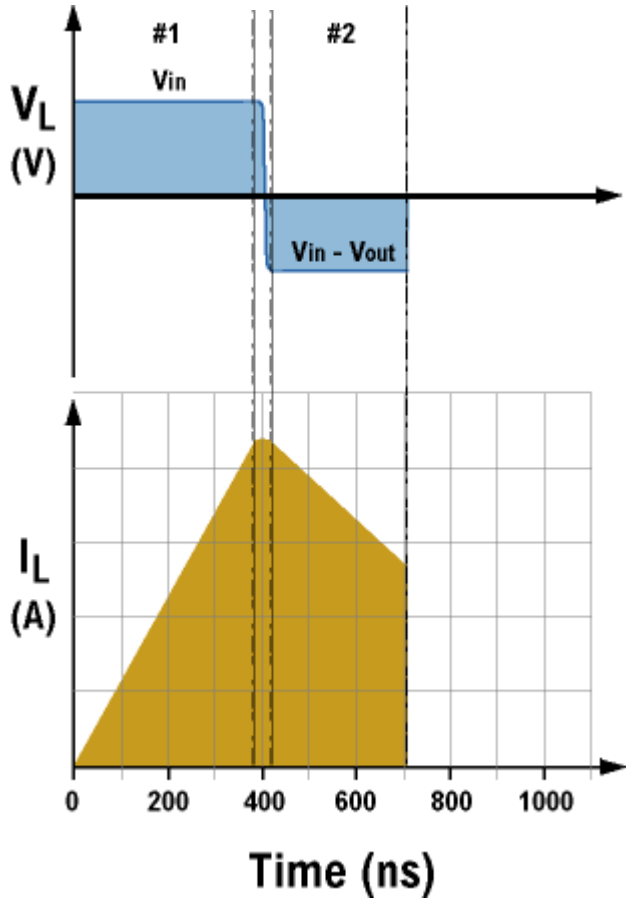

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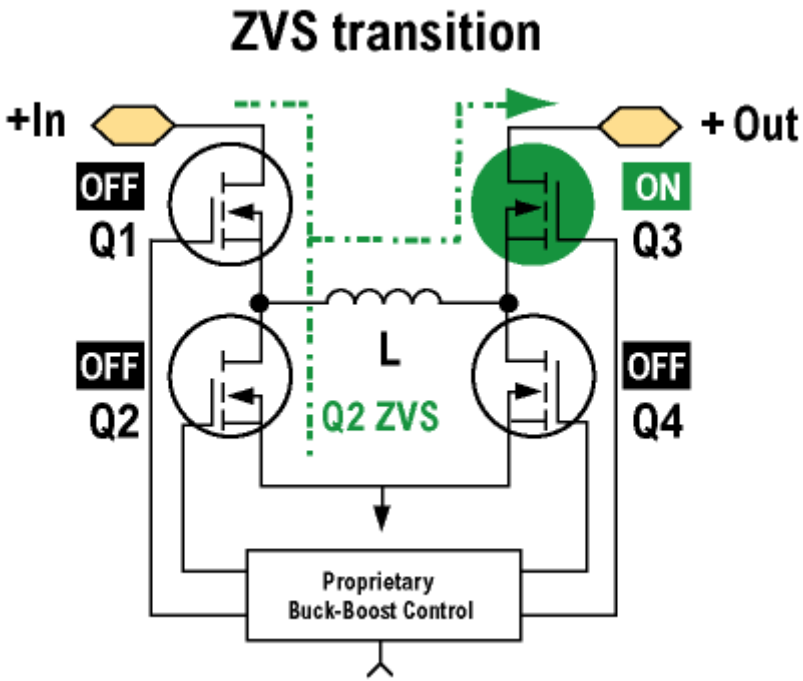

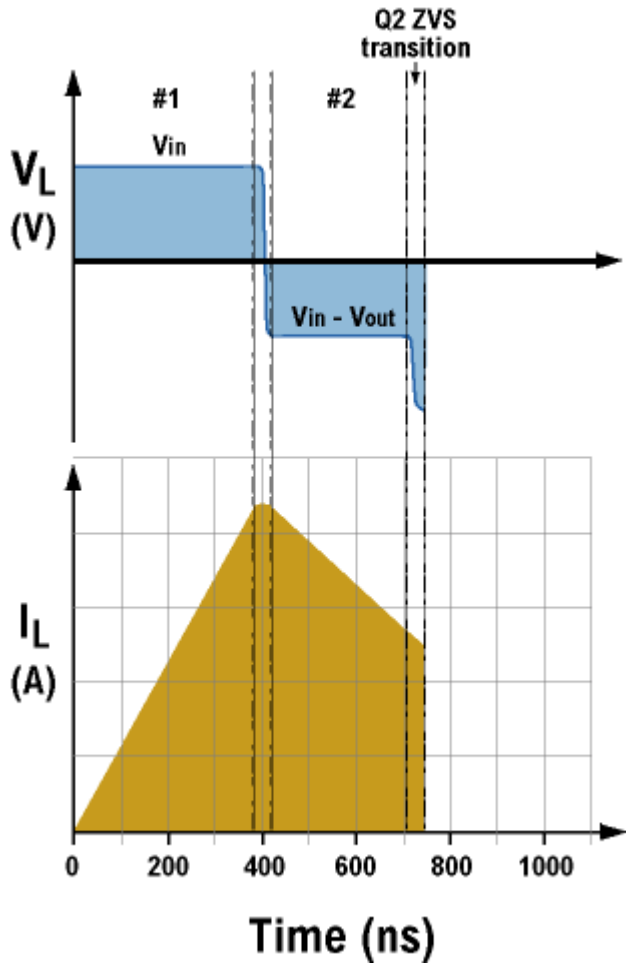

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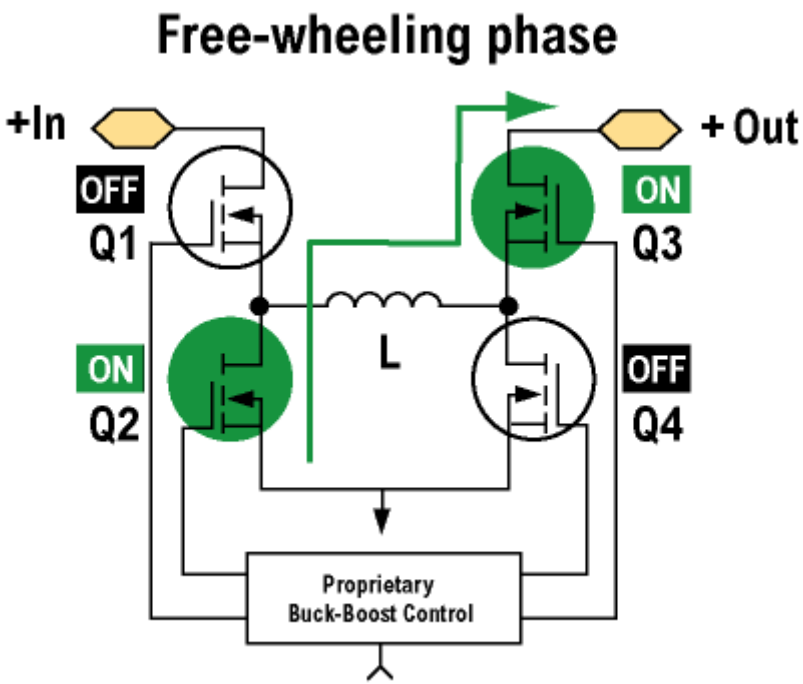

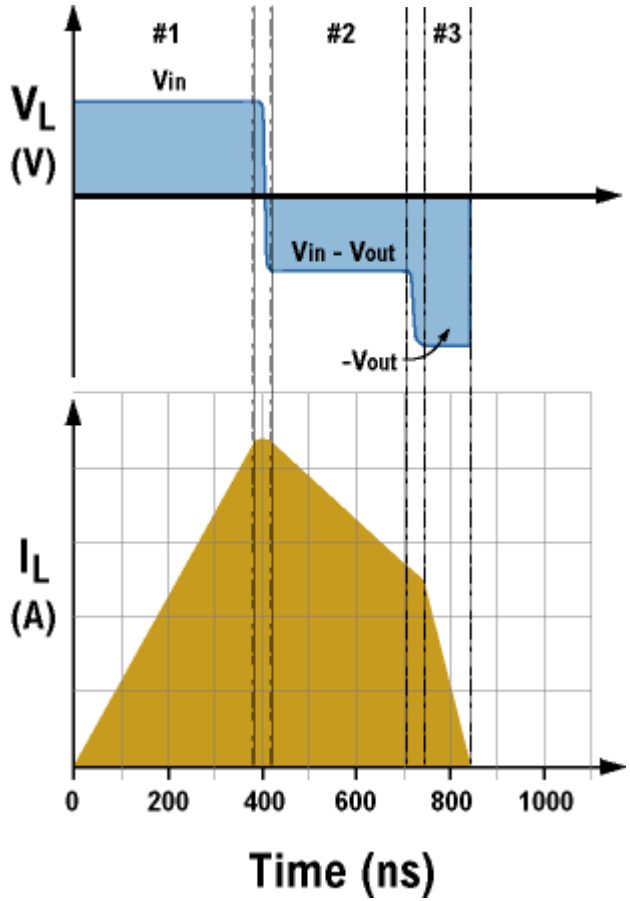

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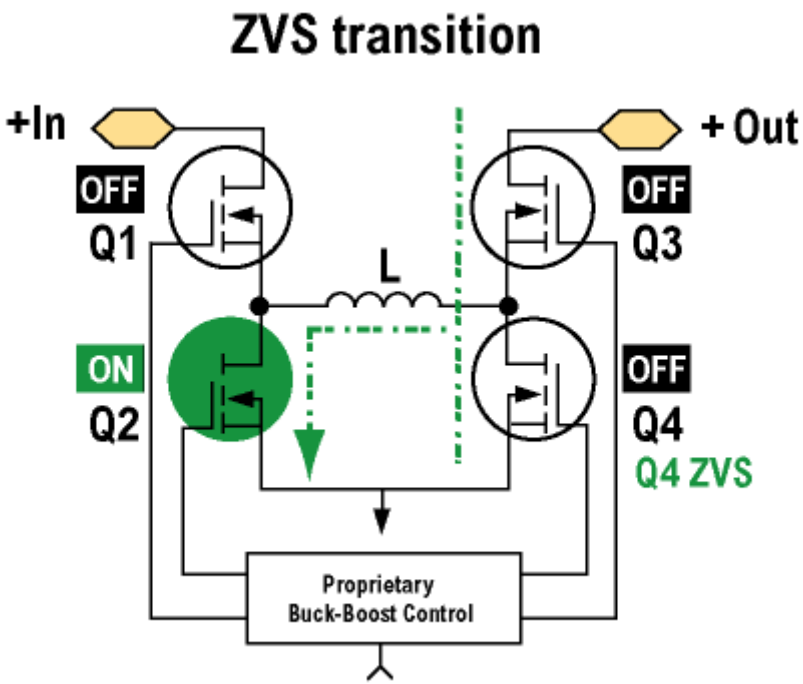

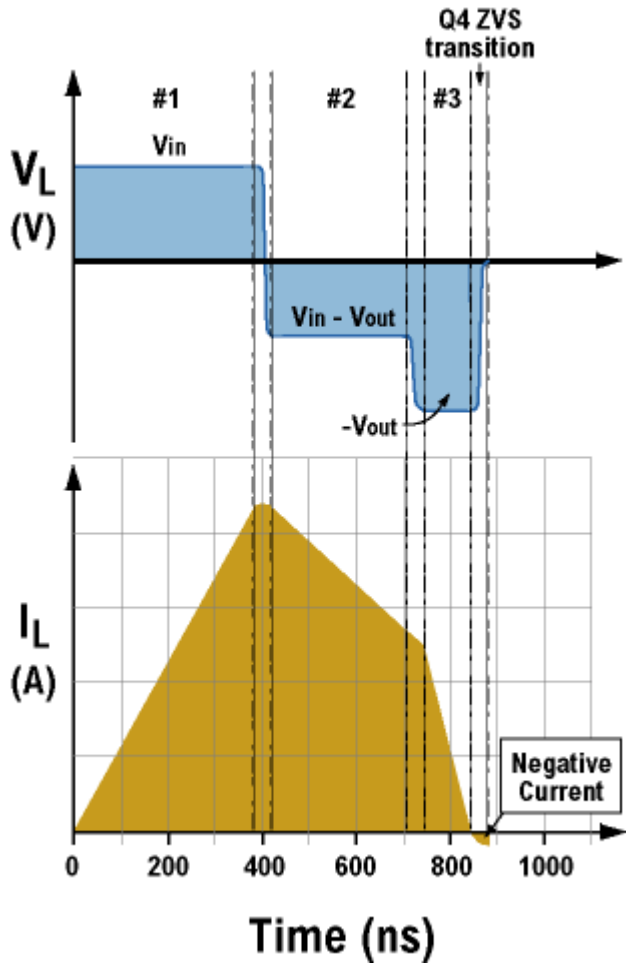

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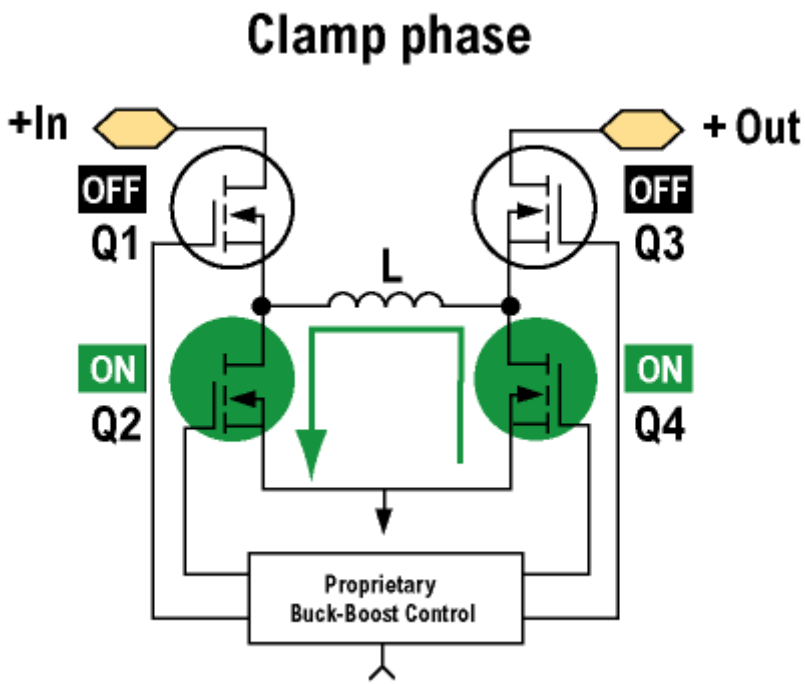

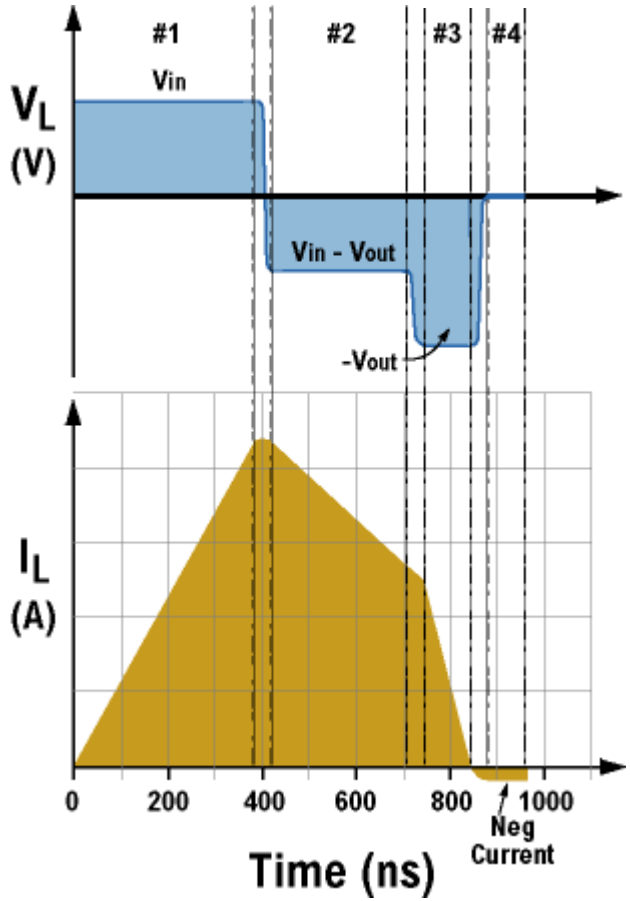

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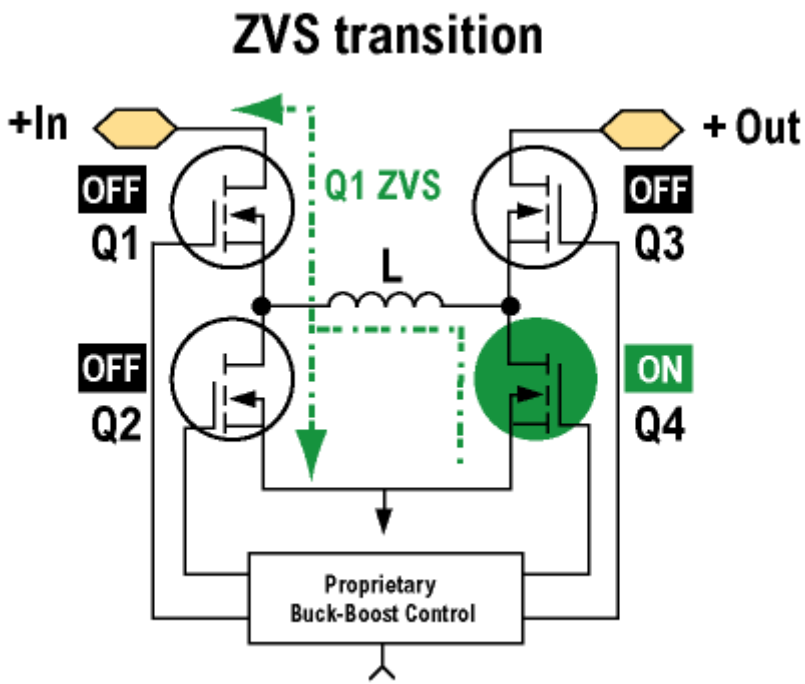

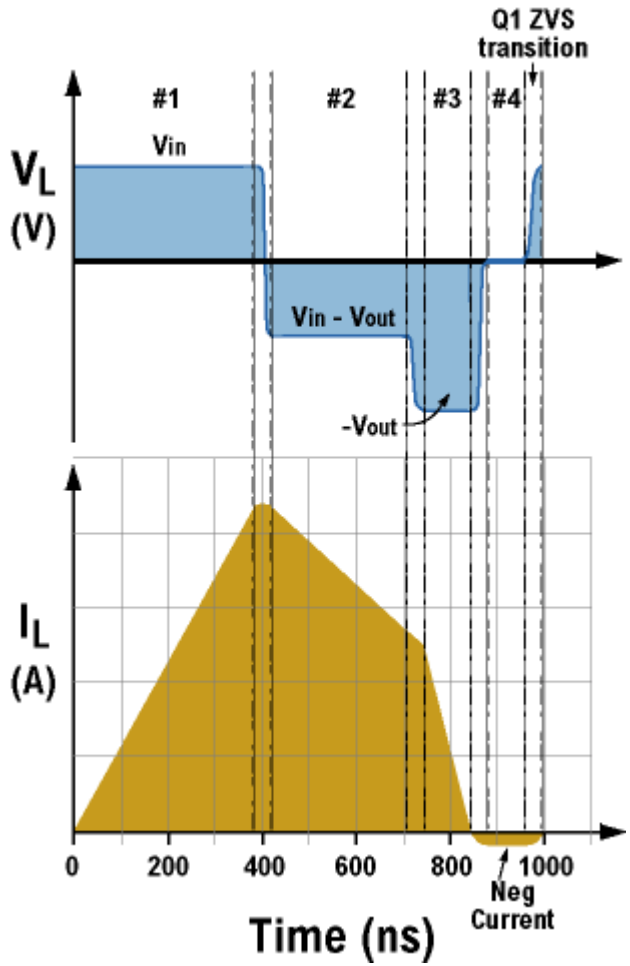

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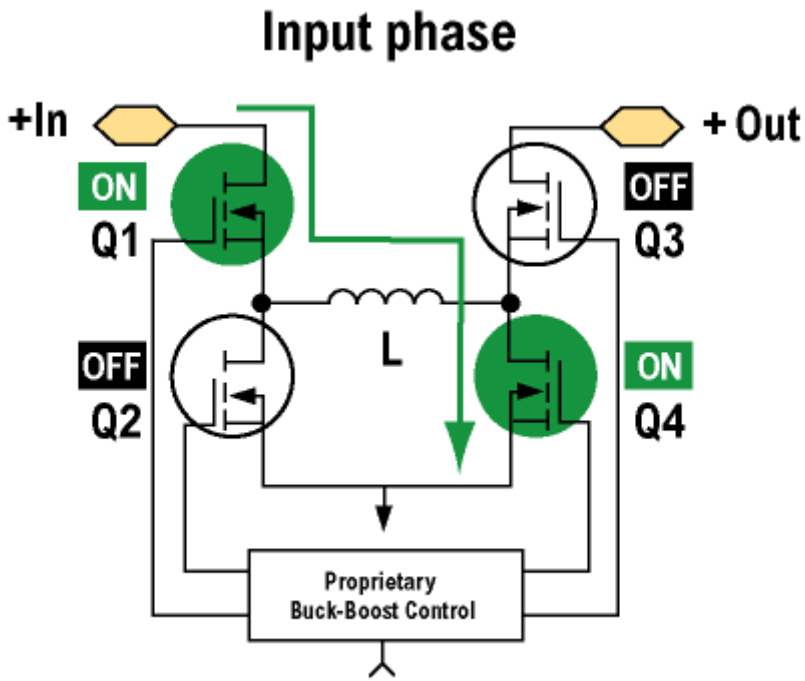

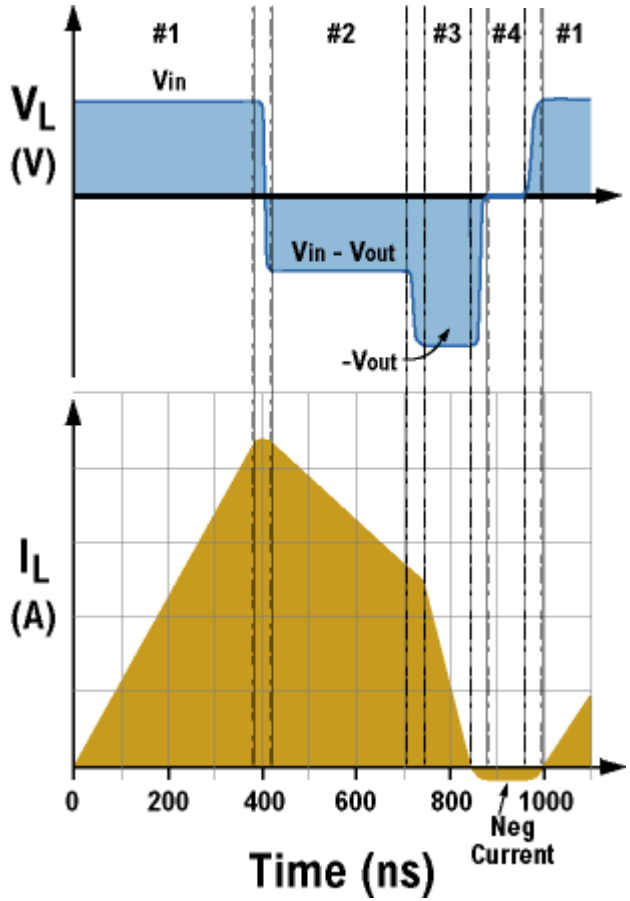

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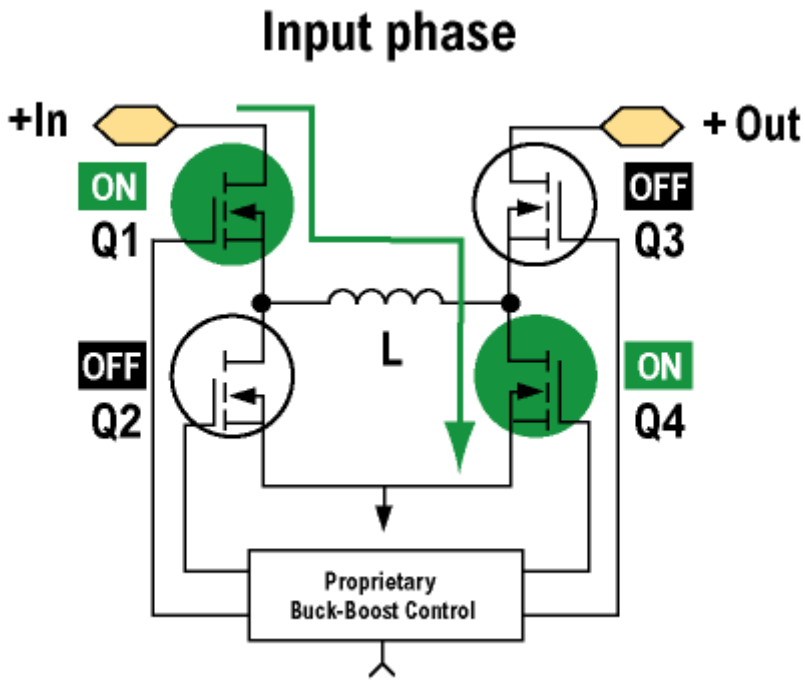

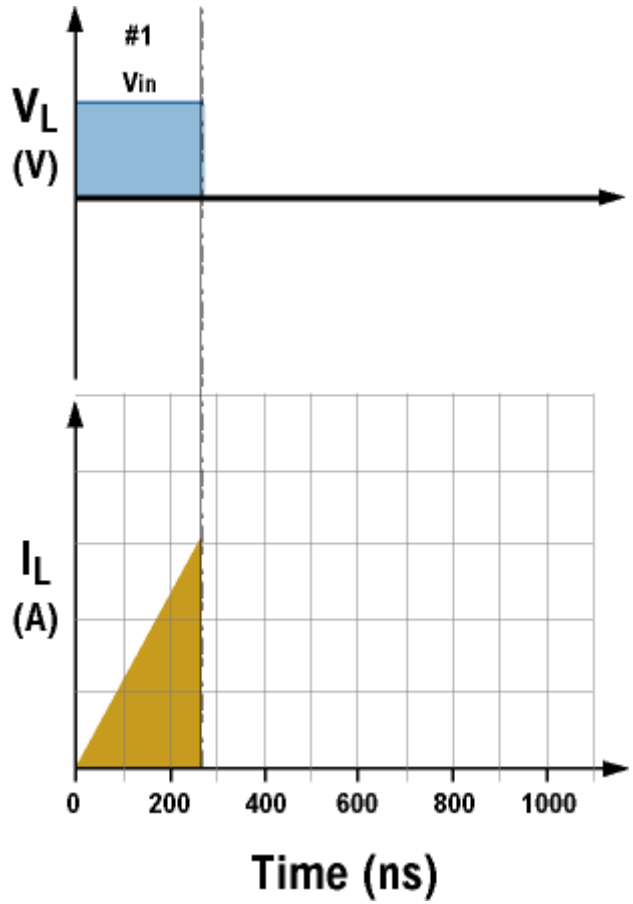

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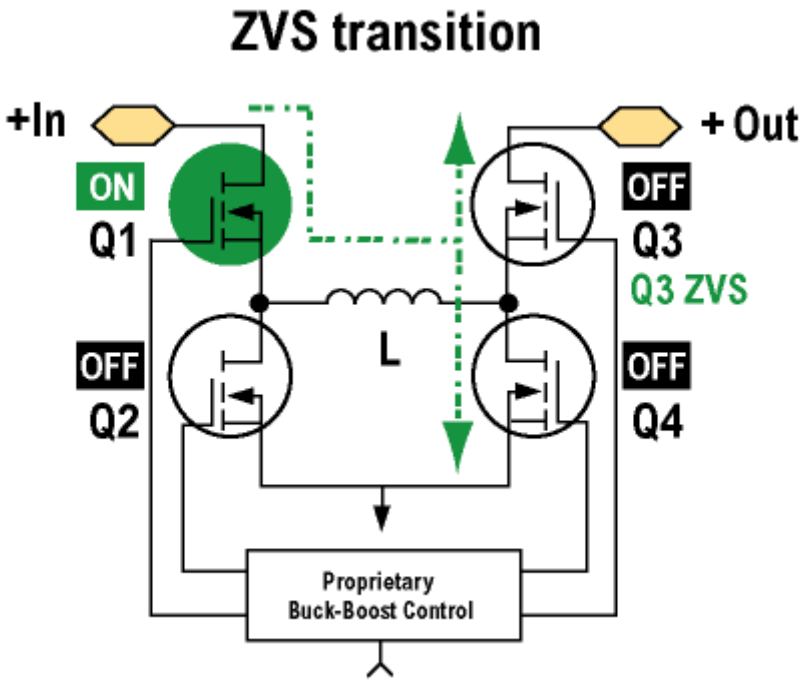

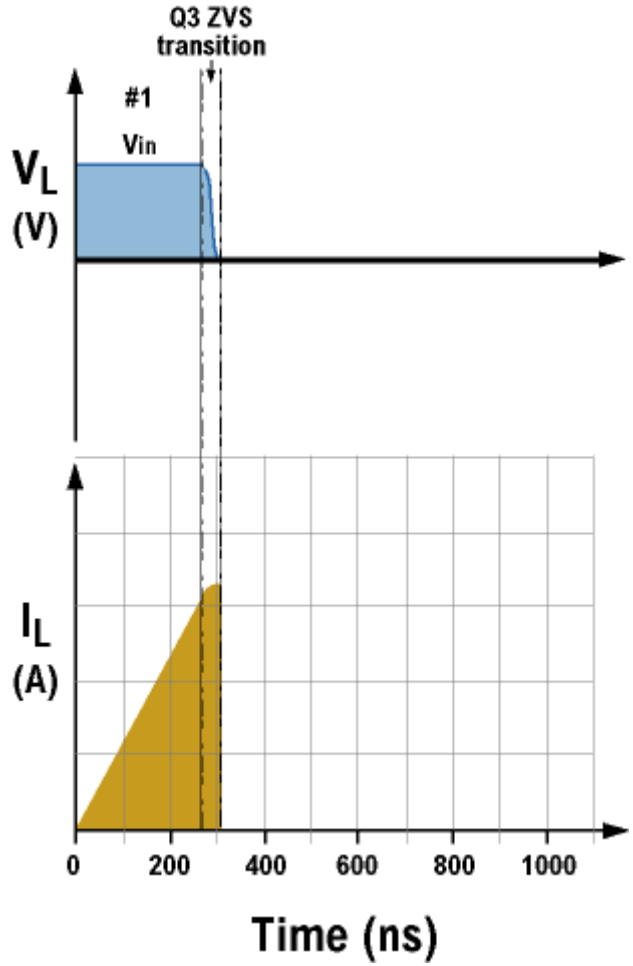

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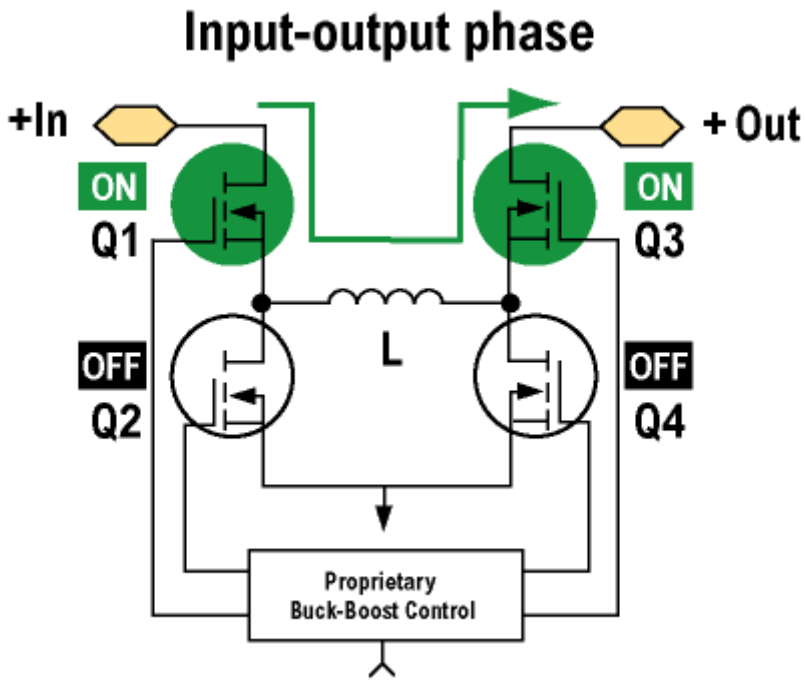

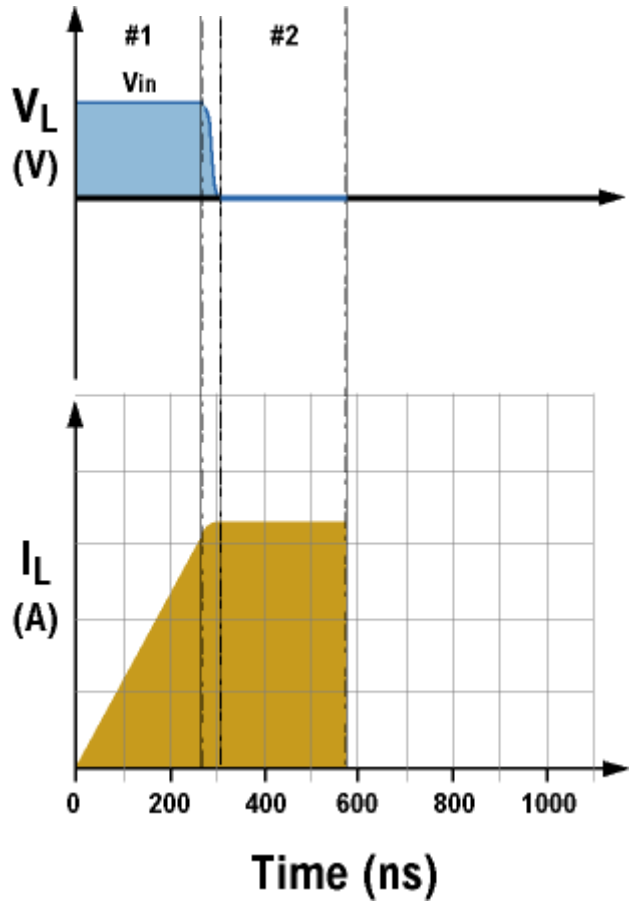

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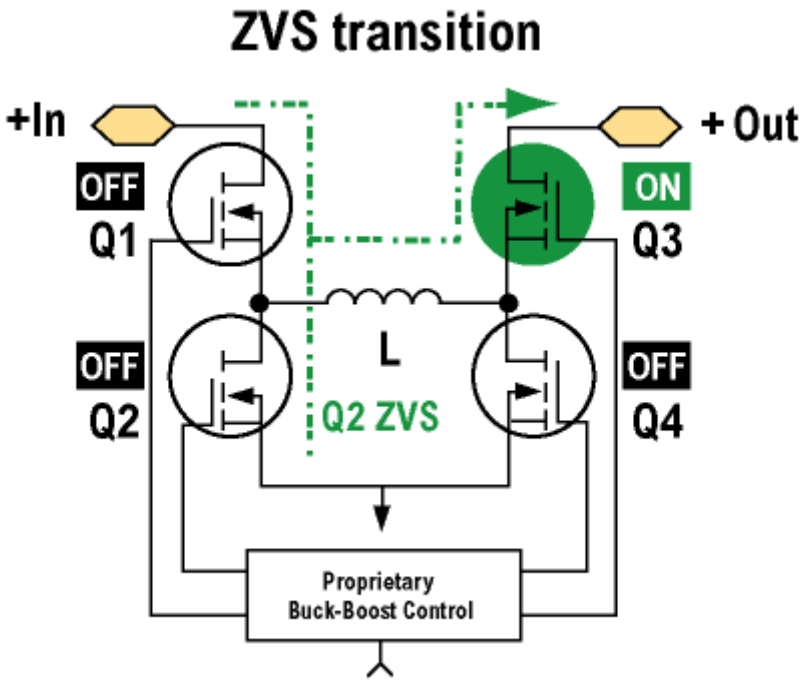

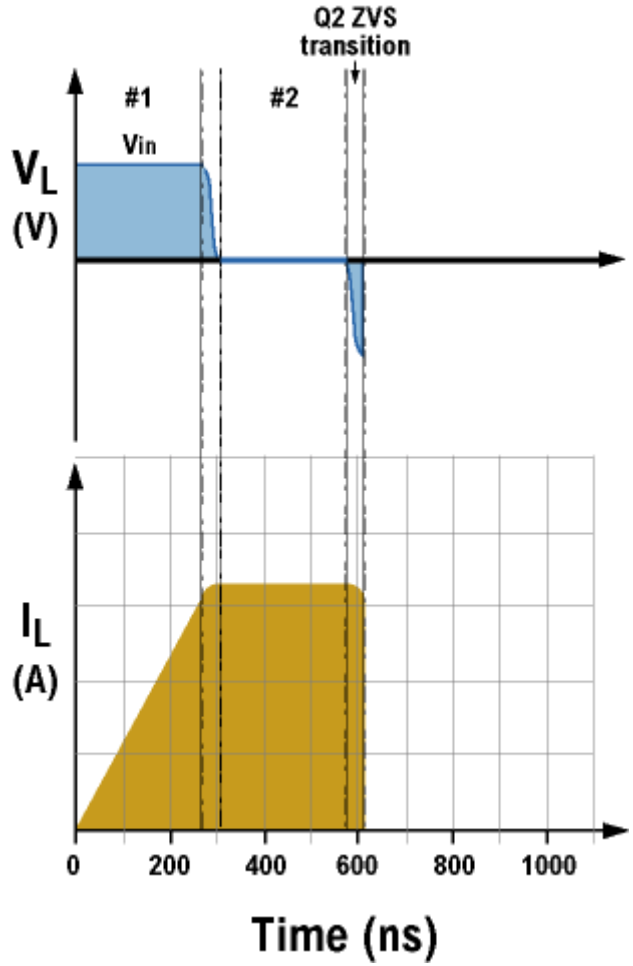

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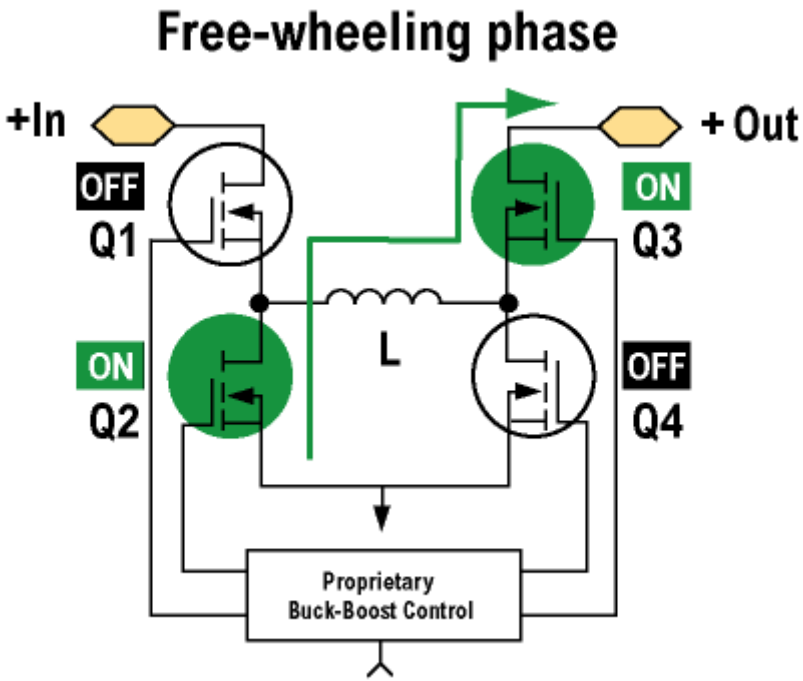

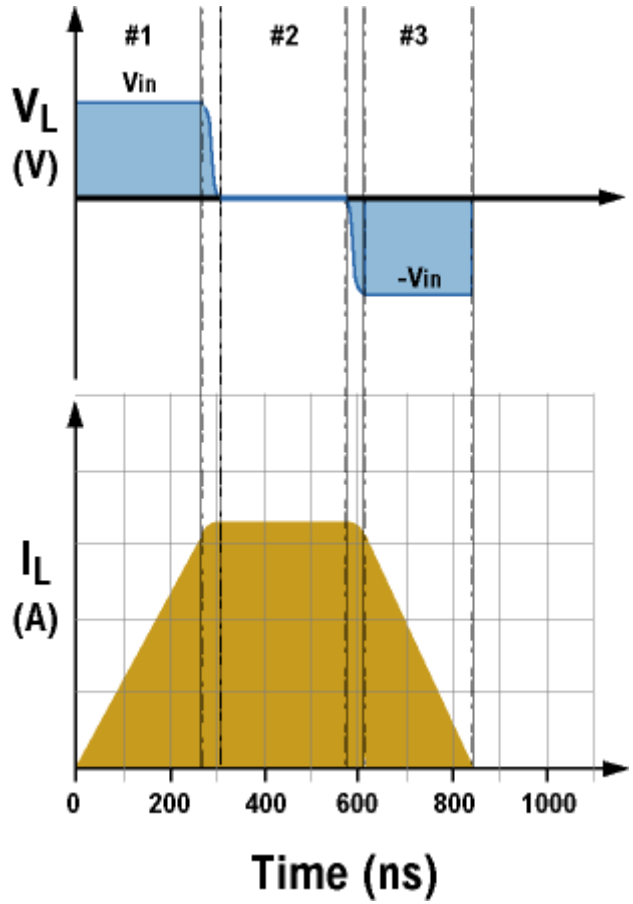

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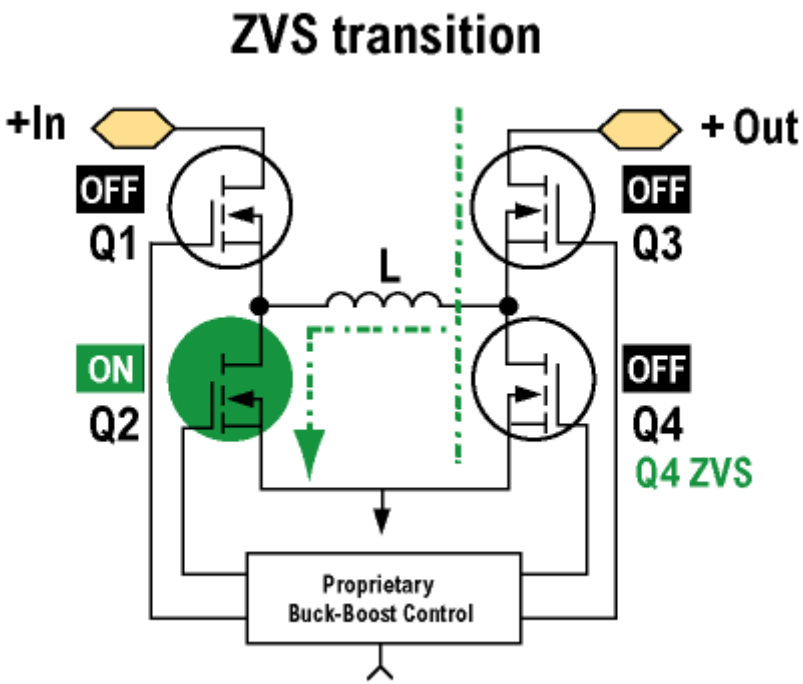

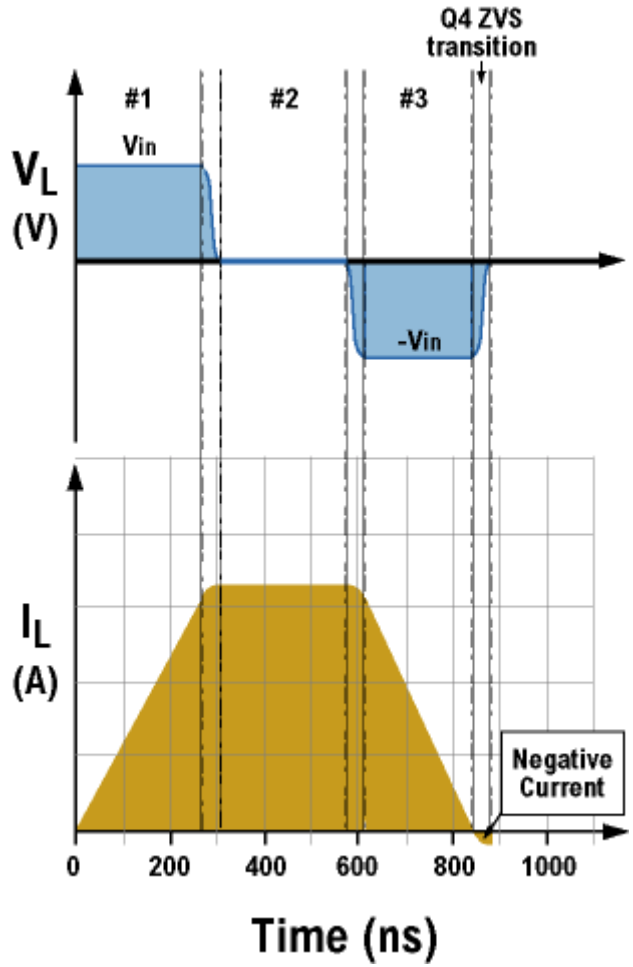

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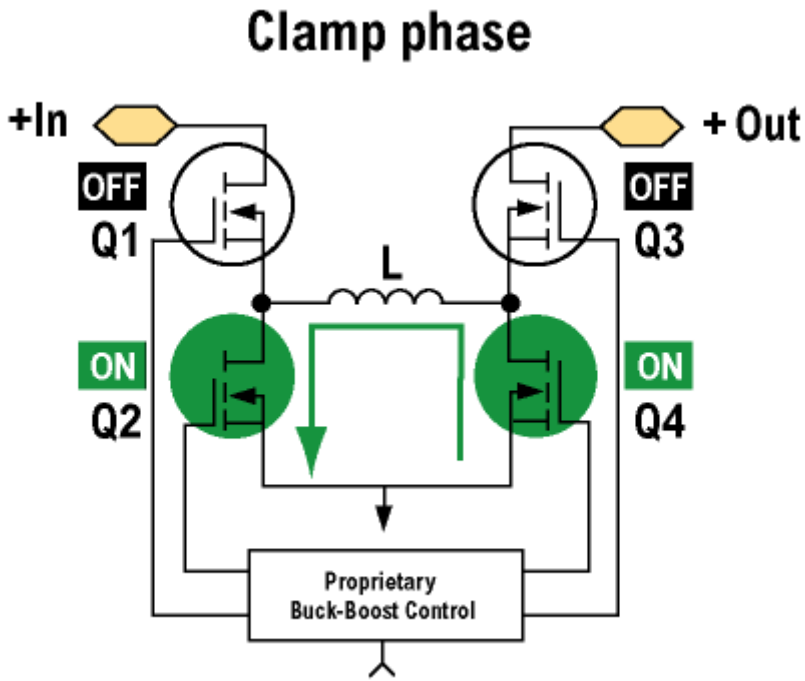

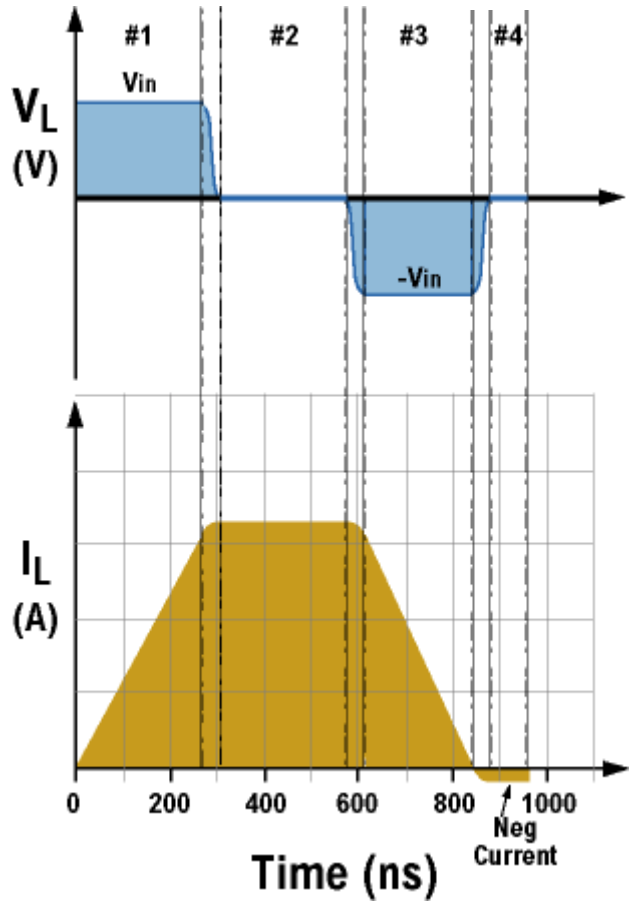

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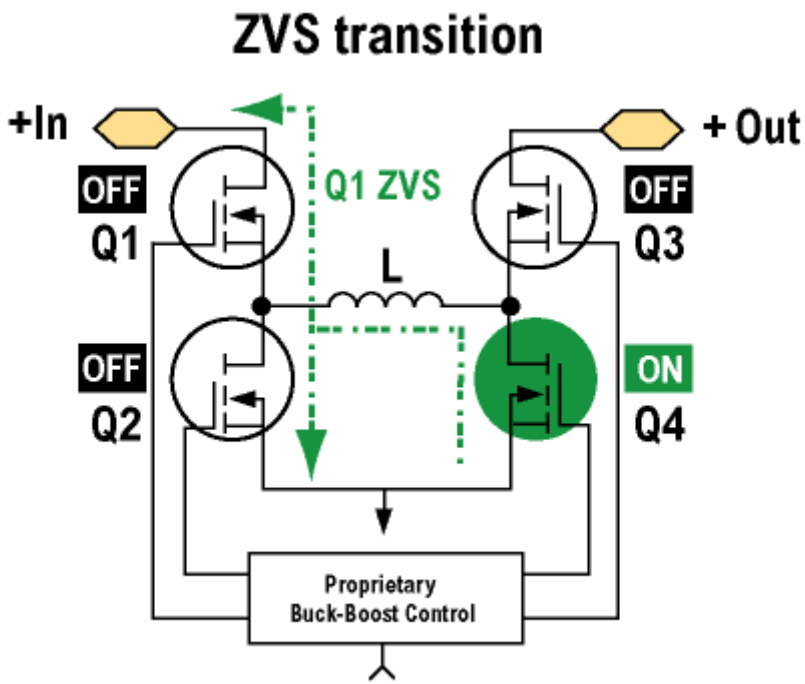
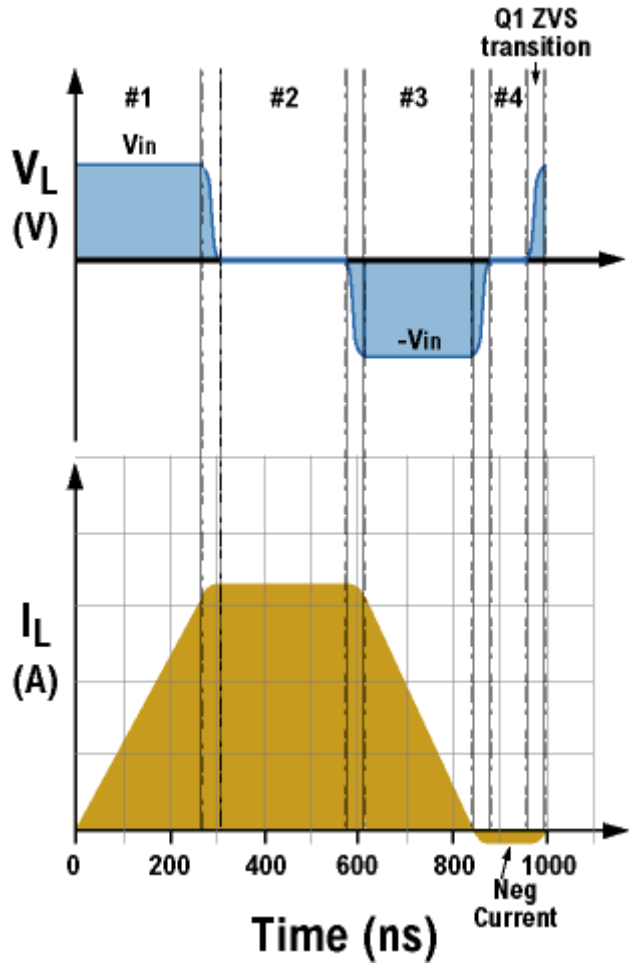
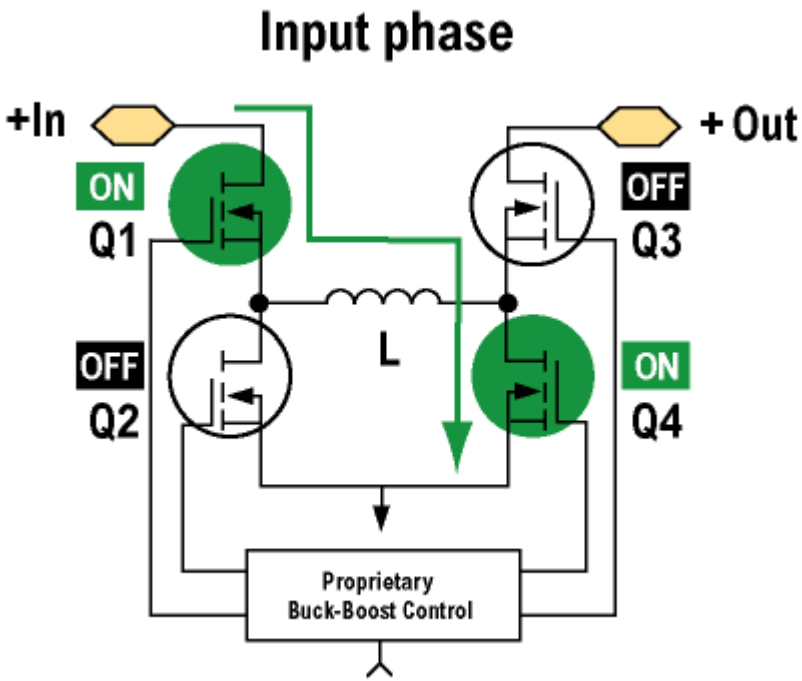
Vin ≅ Vout

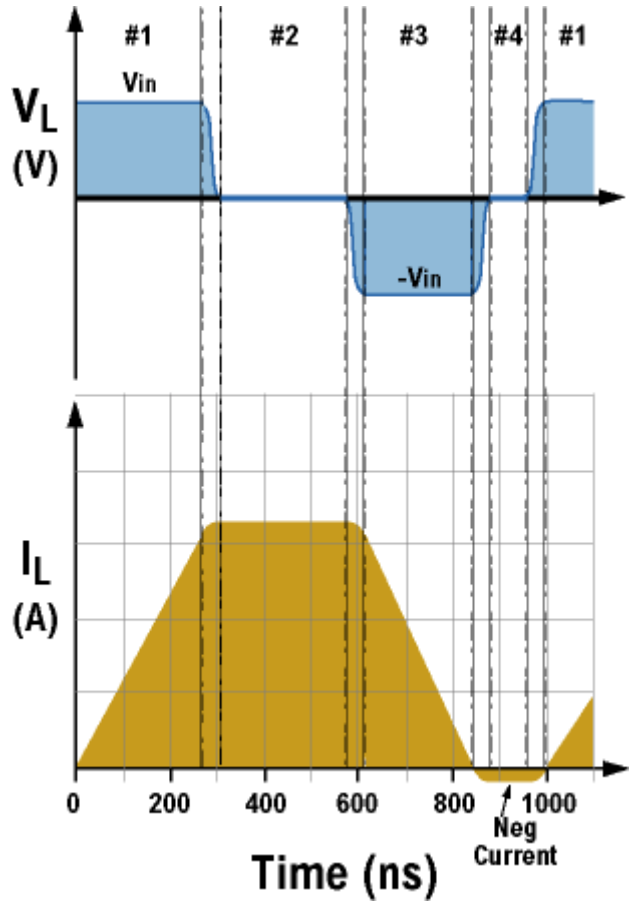




Patents and Patents Pending

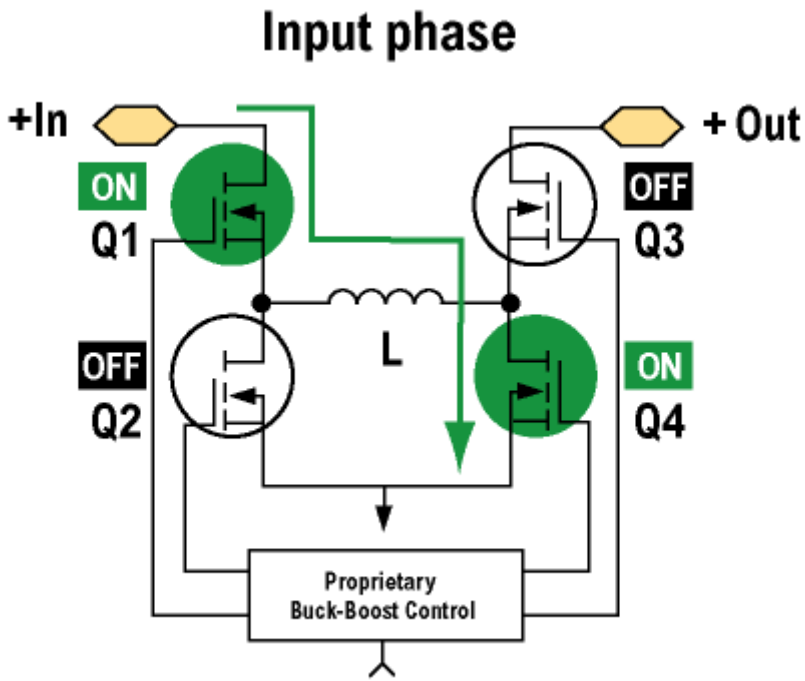
Vin ≅ Vout

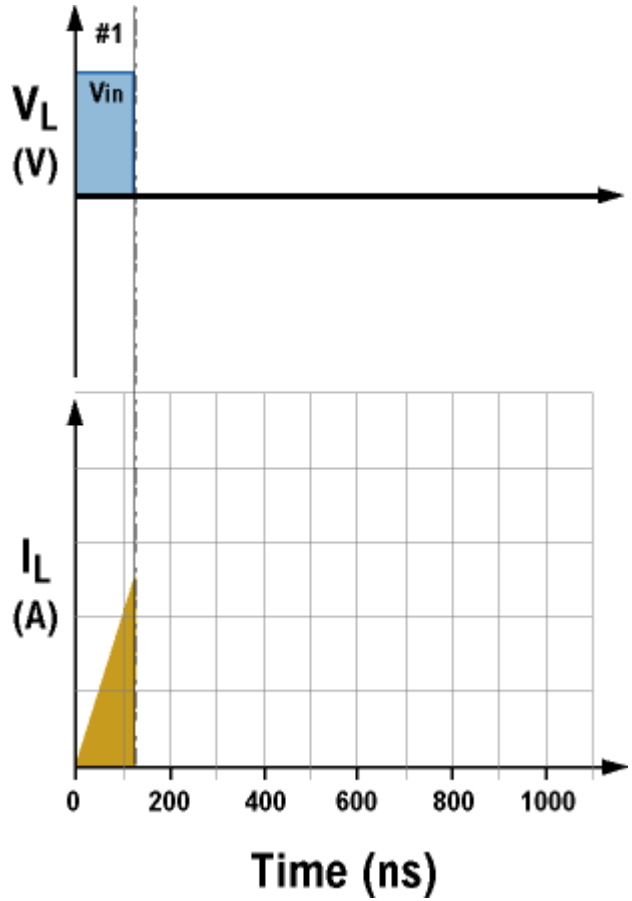




Patents and Patents Pending

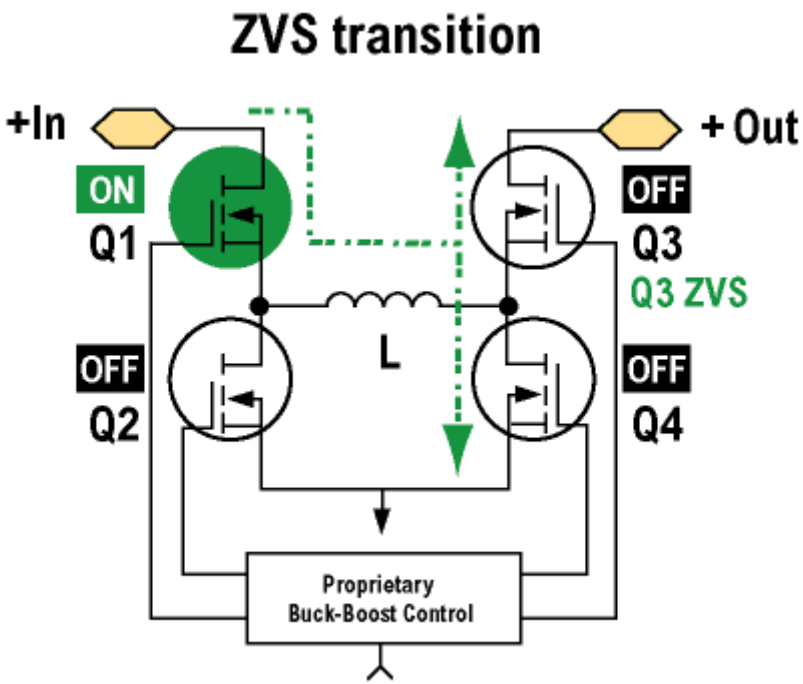
Vin > Vout

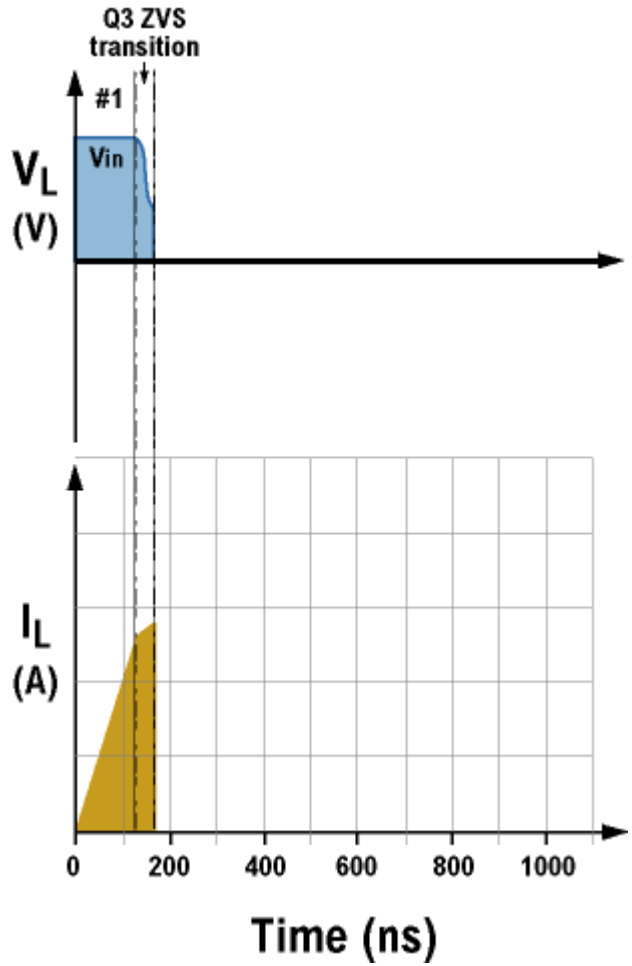




Patents and Patents Pending

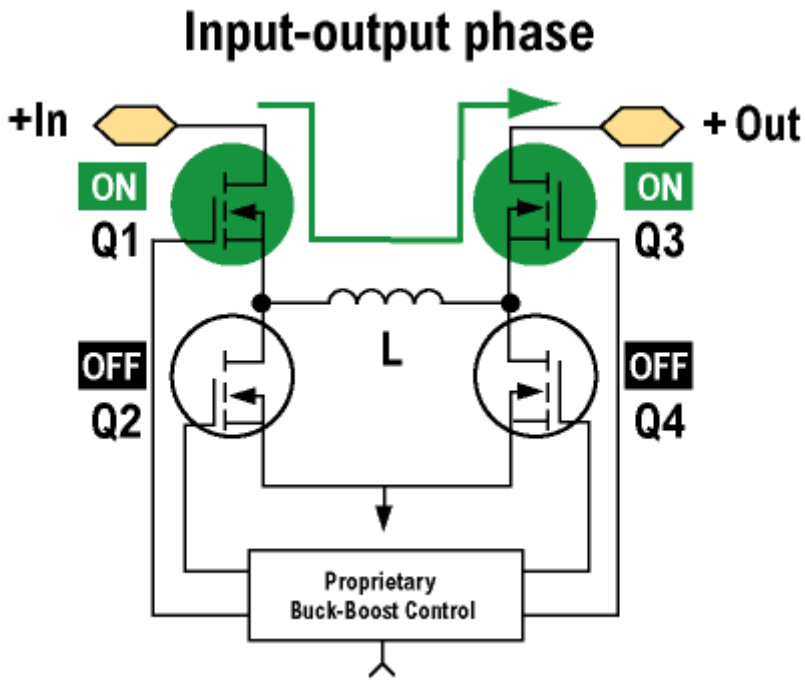
Vin > Vout

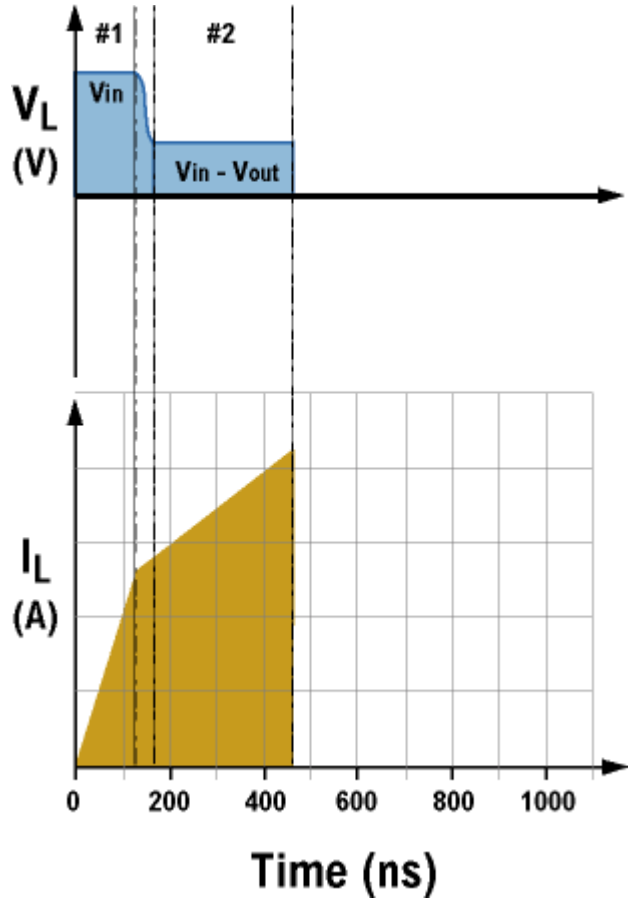




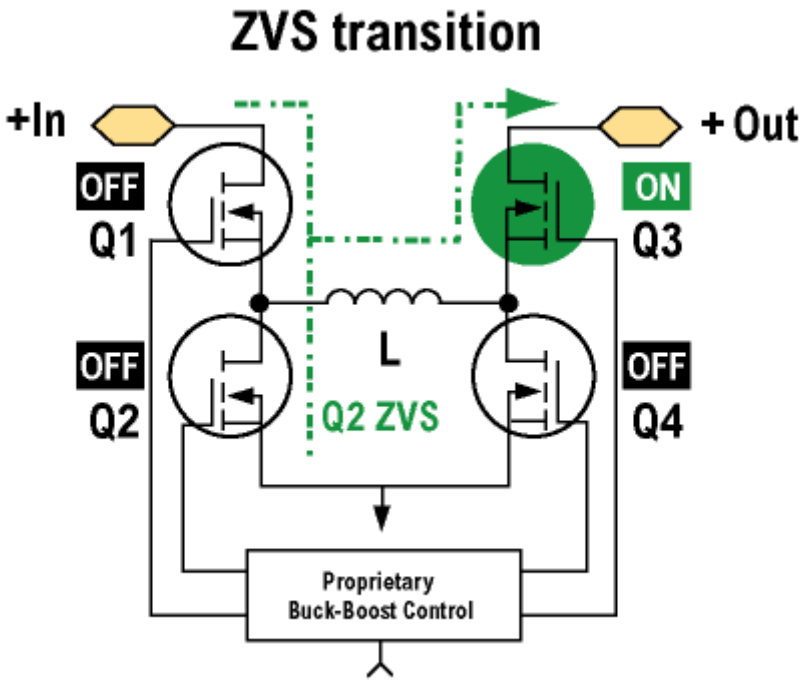
Patents and Patents Pending

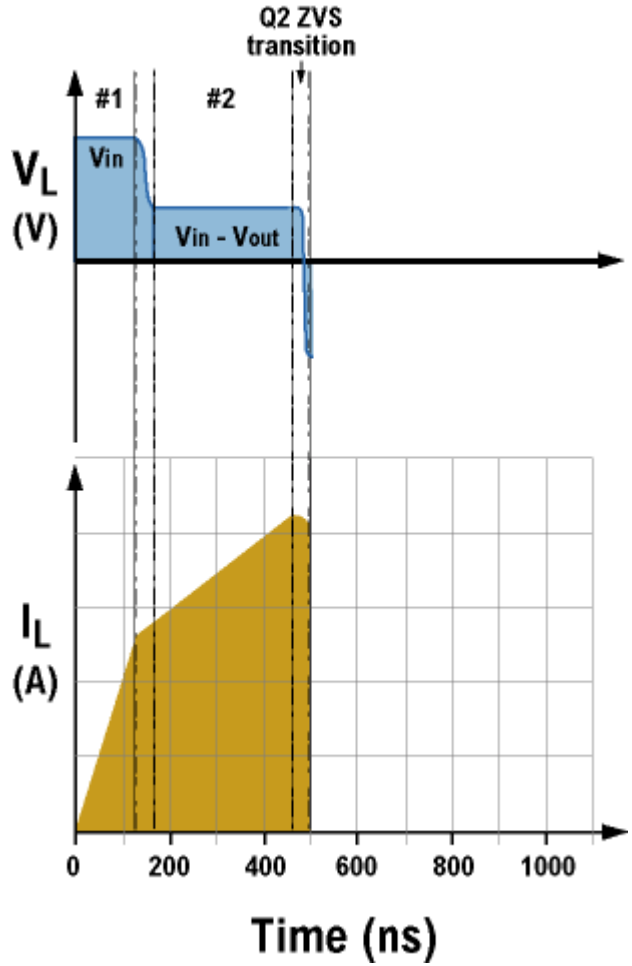
Vin > Vout


Input-output phase
+In
+ Out
ON
Q1
ON
Q3
OFF
Q2
OFF
Q4
L
Proprietary
Buck-Boost Control


#1
#2
VL
(V)
Vin
Vin - Vout
IL
(A)
0
200
400
600
800
1000
Time (ns)

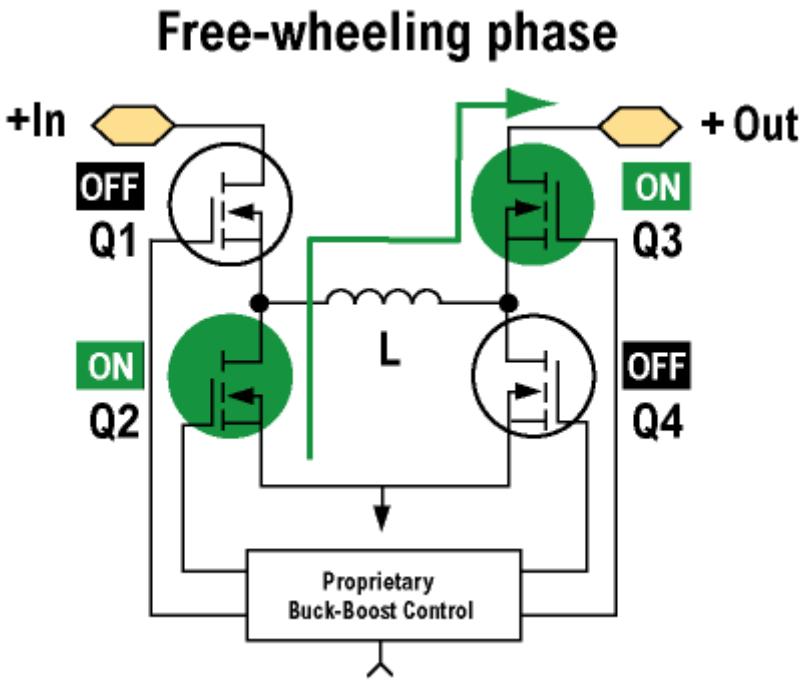
Vin > Vout

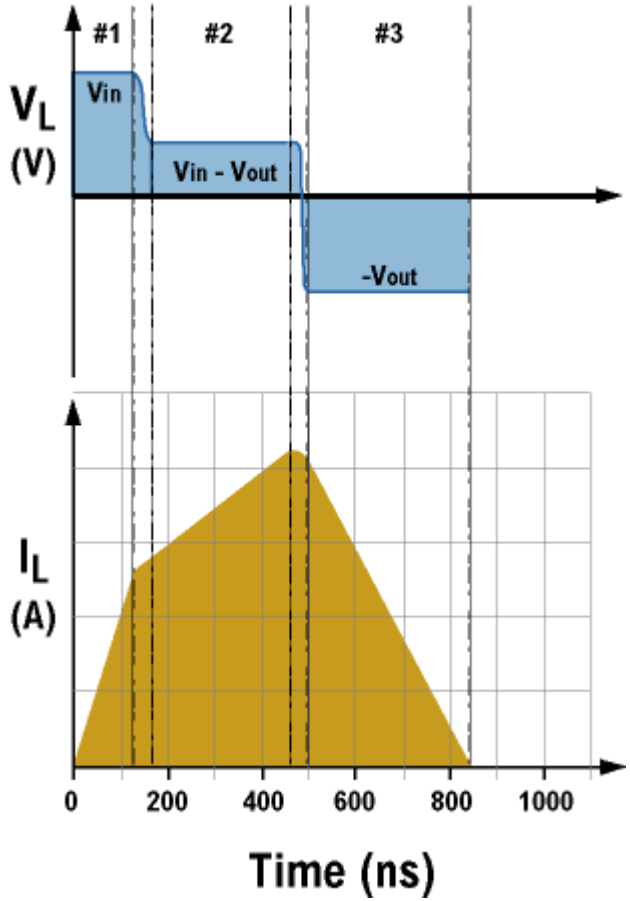




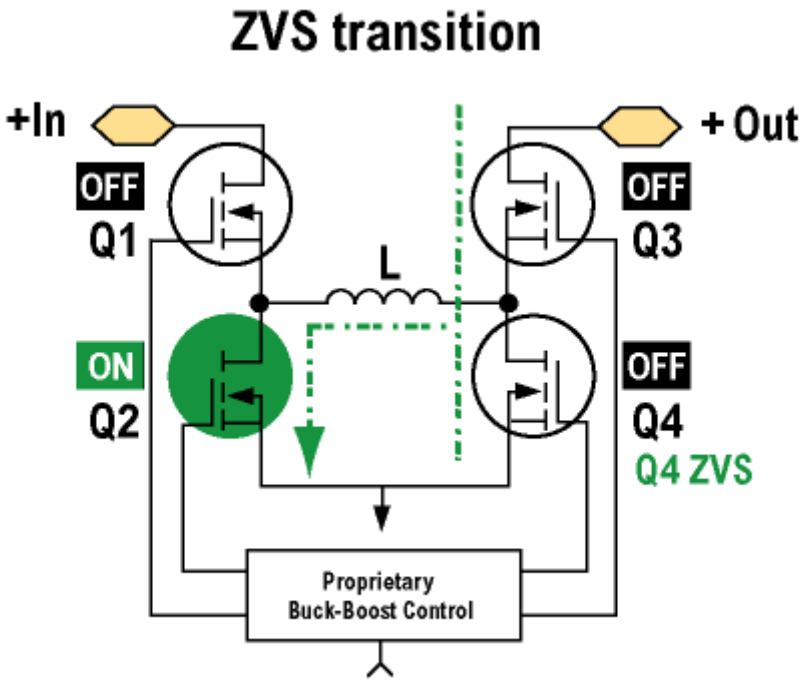
Patents and Patents Pending

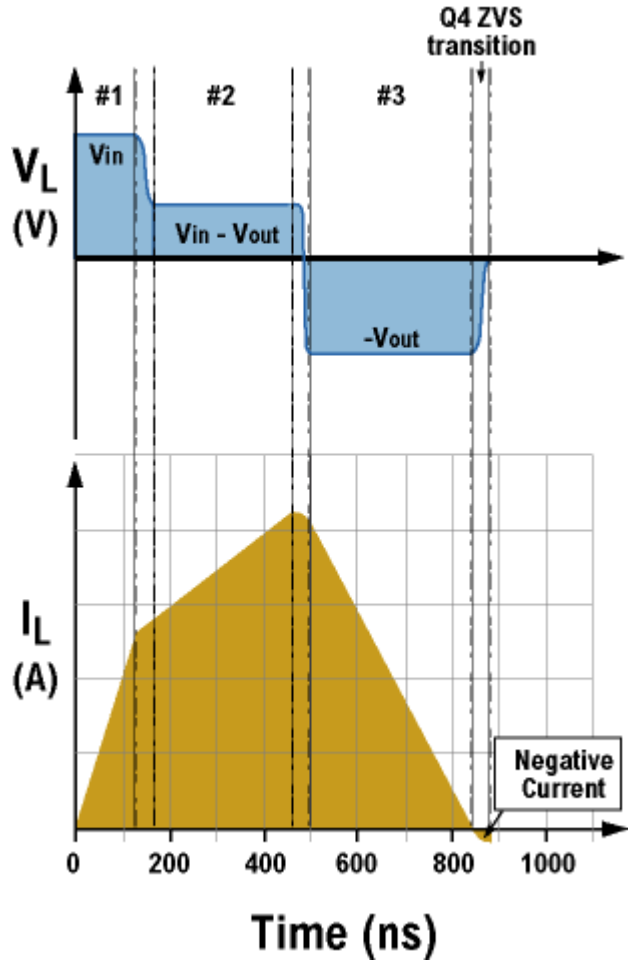
Vin > Vout


Free-wheeling phase
+In
+ Out
OFF
Q1
ON
Q3
ON
Q2
L
OFF
Q4
Proprietary
Buck-Boost Control


#1
#2
#3
VL
(V)
Vin
Vin - Vout
-Vout
IL
(A)
0
200
400
600
800
1000
Time (ns)

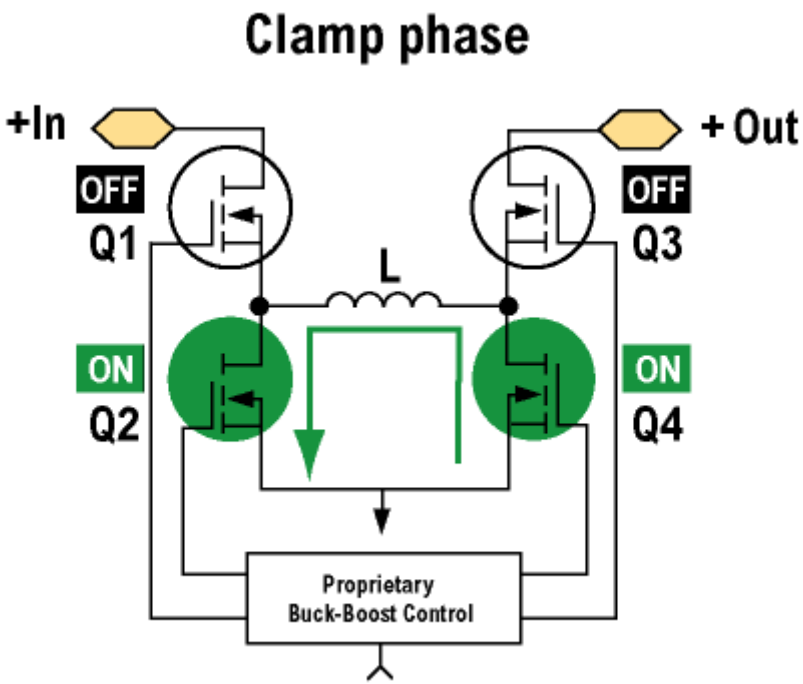
Vin > Vout

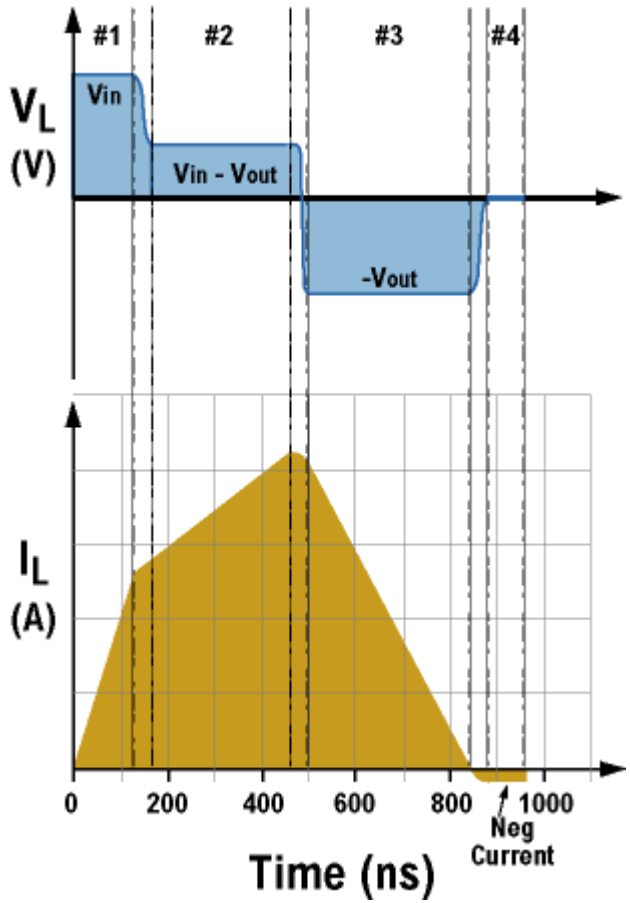




Patents and Patents Pending

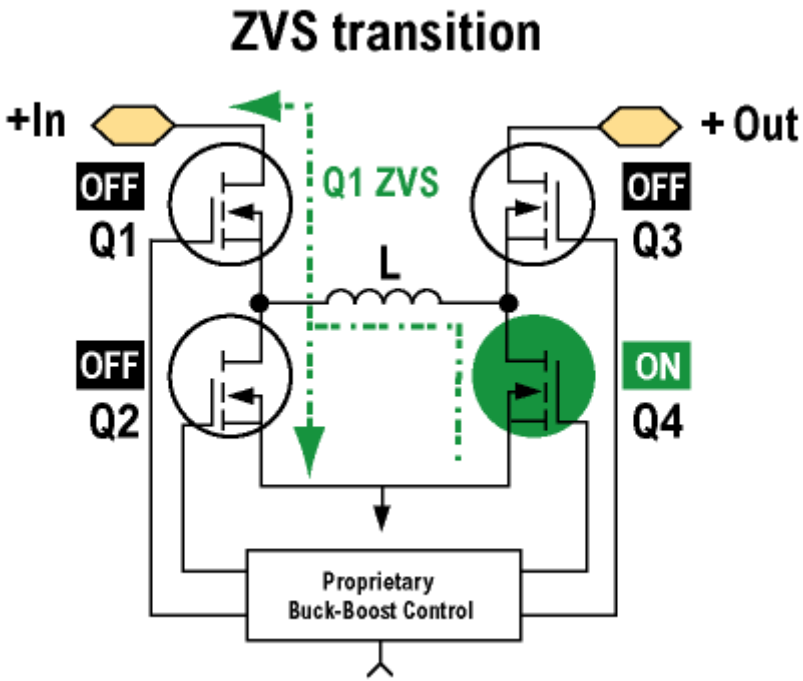
Vin > Vout

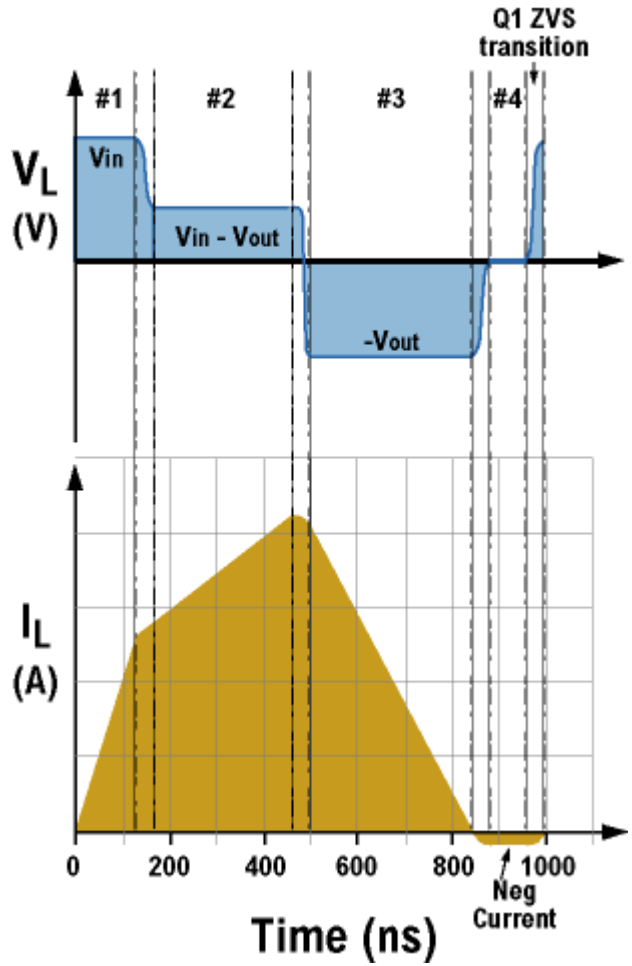




Patents and Patents Pending

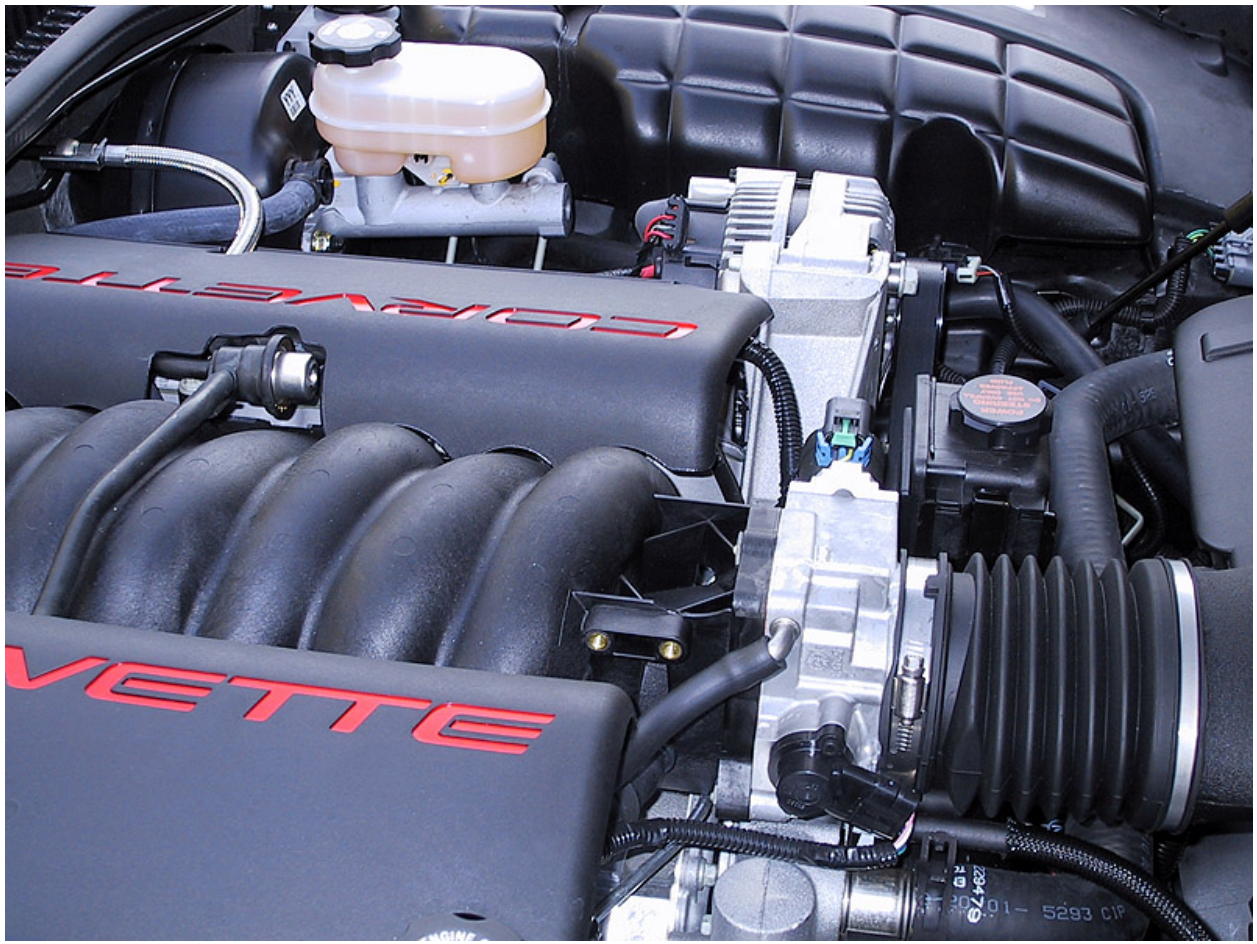
Vin > Vout





Patents and Patents Pending

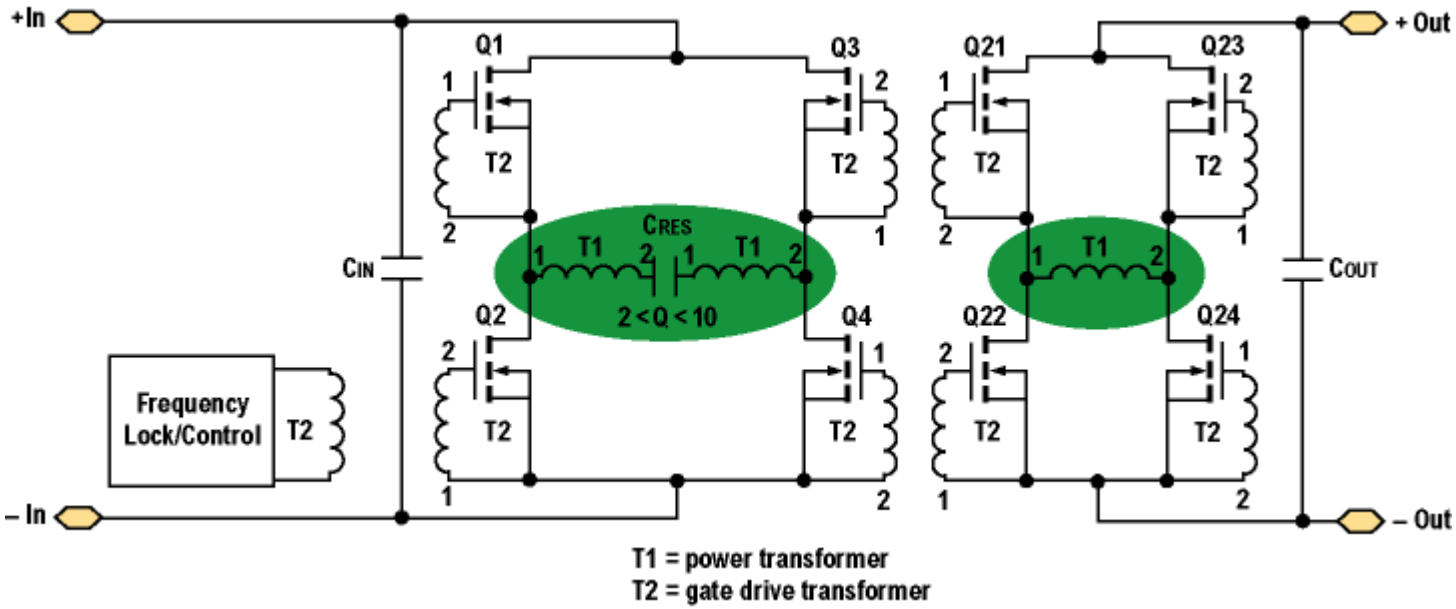
The Engine Under the Hood – VTM



“Full VIC” VTM Capabilities

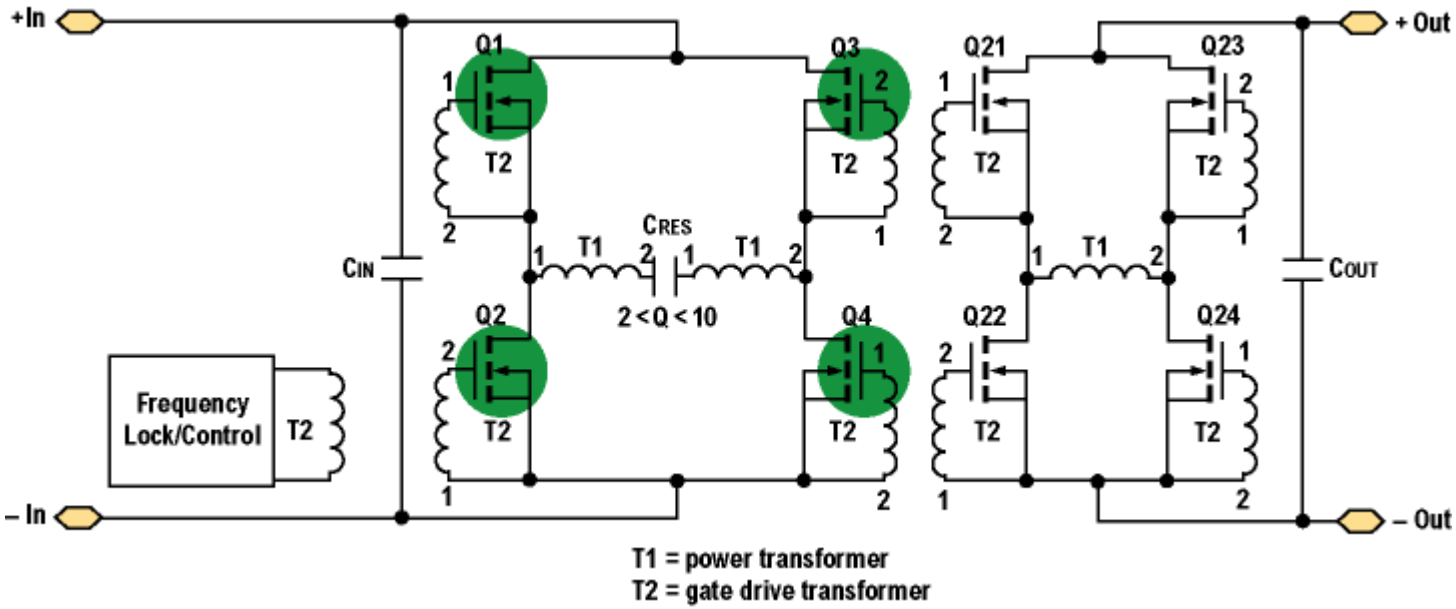
- ZCS / ZVS Sine Amplitude Converter (SAC)
- Input voltage: 0-400 V (up to 2:1 range)
- Output voltage: 0-400 V
- Transformation ratio (K): 1/200 to 200
- Output current or power: up to 100 A or 300 W
- Conversion efficiency: up to 97%
- Conversion frequency: up to 4 MHz, fixed

VTM / BCM SAC Power Train



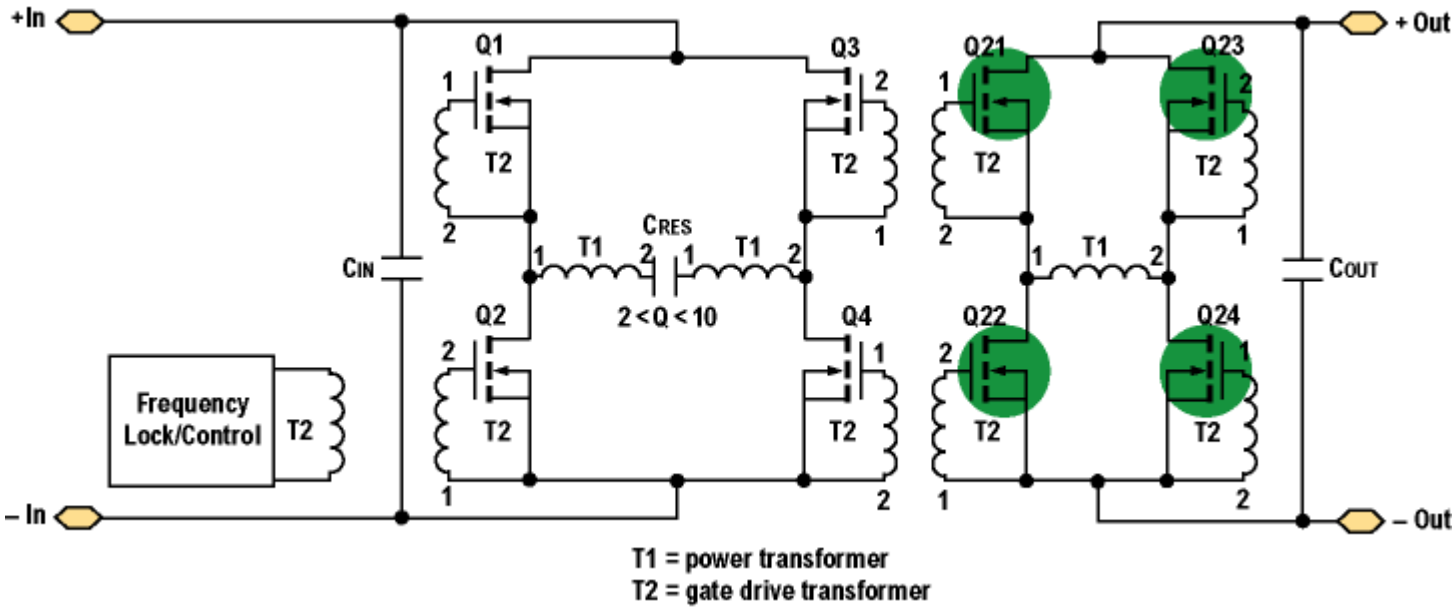
- Primary “Engine” is a Low Q oscillator formed by CRES and the leakage inductance of T1

VTM / BCM SAC Power Train



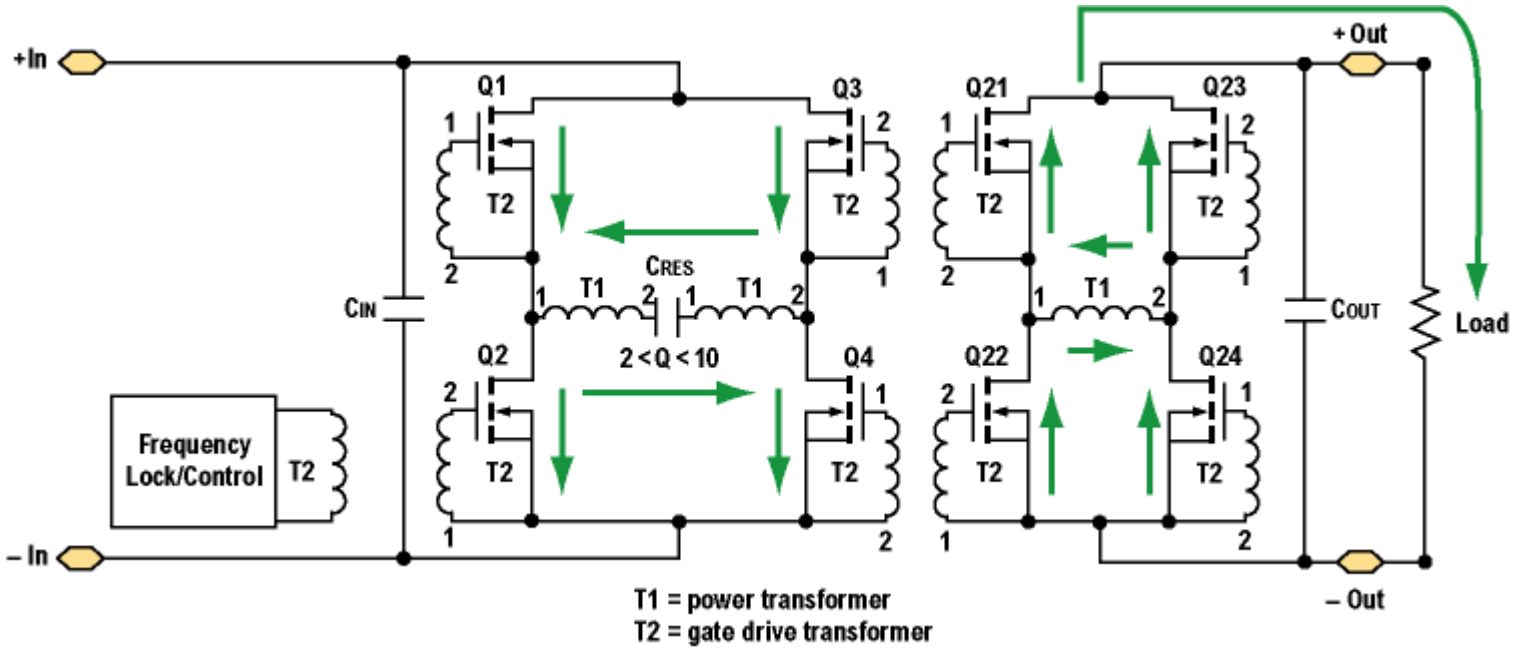
- The Low Q oscillator is driven by an H-bridge

VTM / BCM SAC Power Train



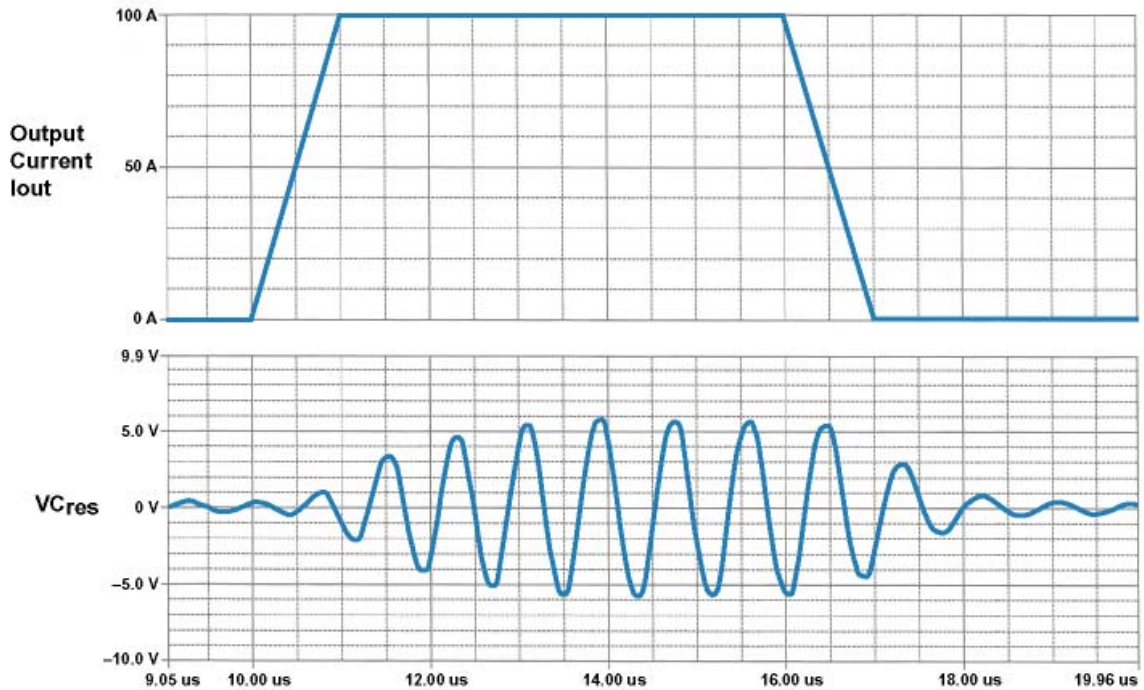
- In this particular example, secondary rectification is also performed using an H-bridge

VTM/BCM SAC Power Train



- Load current drives the Low Q oscillator by pulling primary current

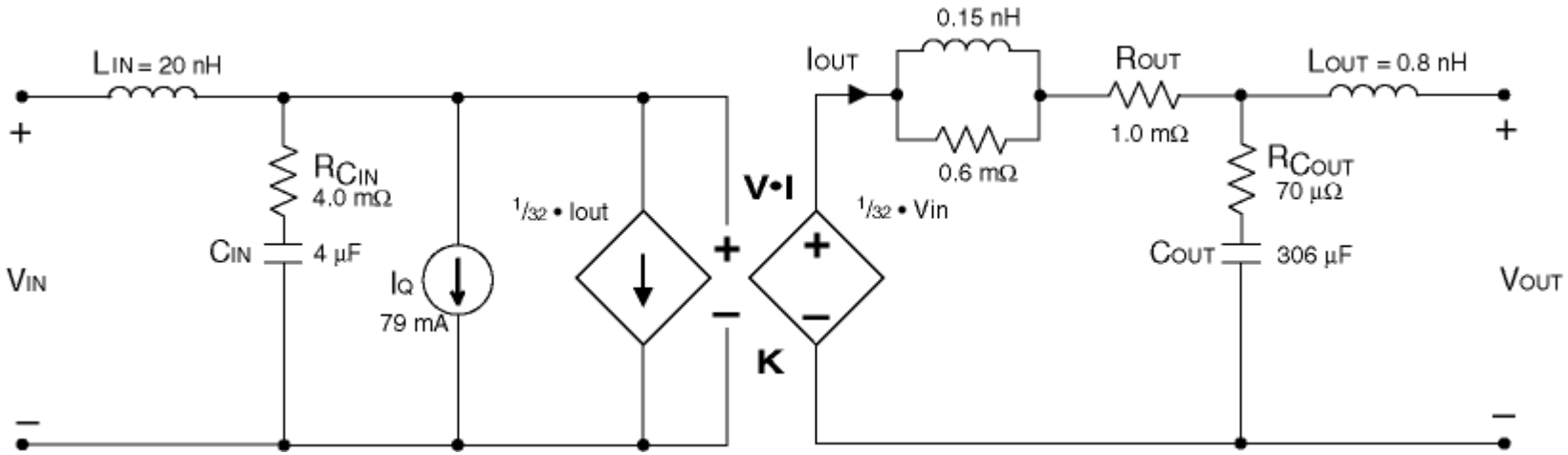
VTM / BCM Sine Amplitude Converter (SAC)



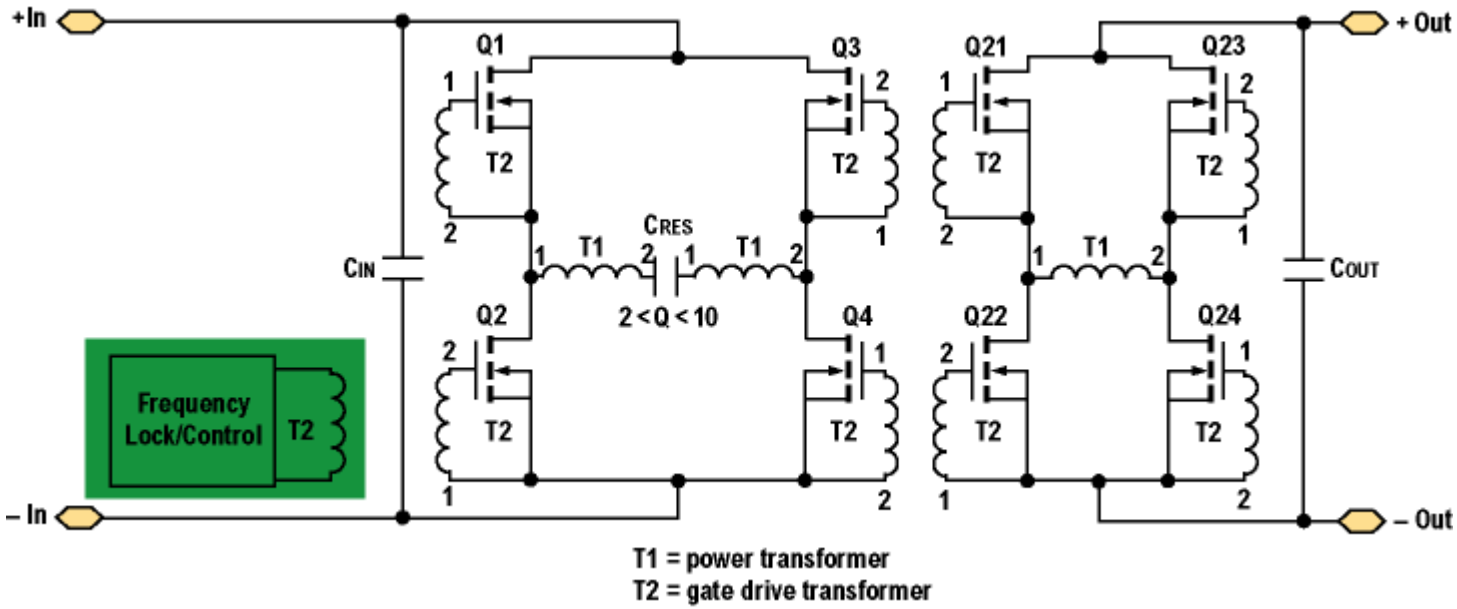
- The amplitude of the Low Q oscillator is proportional to the load current as reflected back to the primary

VTM / BCM Level 2 Behavioral Model

48 V to 1.5 V 100 A VTM

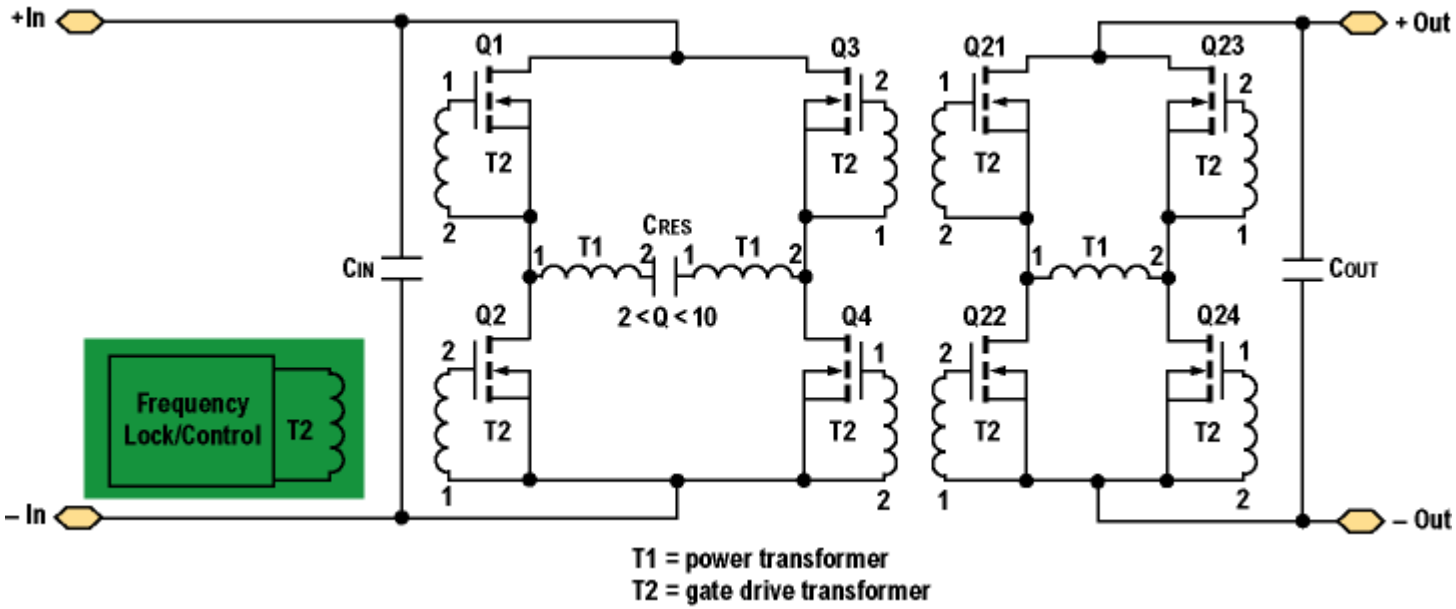


VTM / BCM SAC Control



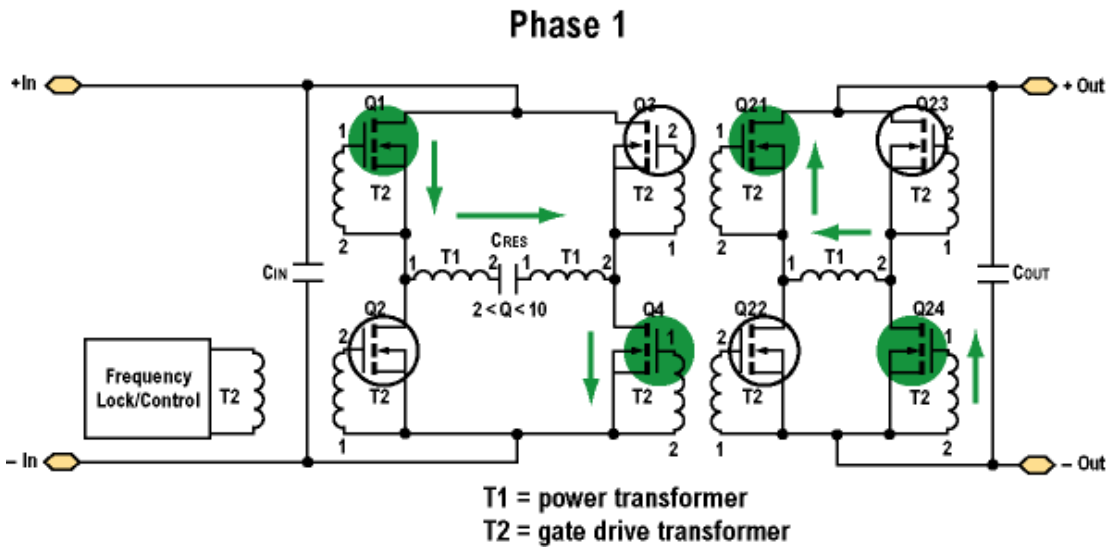
- The controller locks to the natural frequency of the Low Q oscillator and turns all switches ON and OFF under ZCS/ZVS conditions
- Conduction states result in a 100% effective duty cycle
- Control circuitry recycles the gate drive energy from each pair of switches

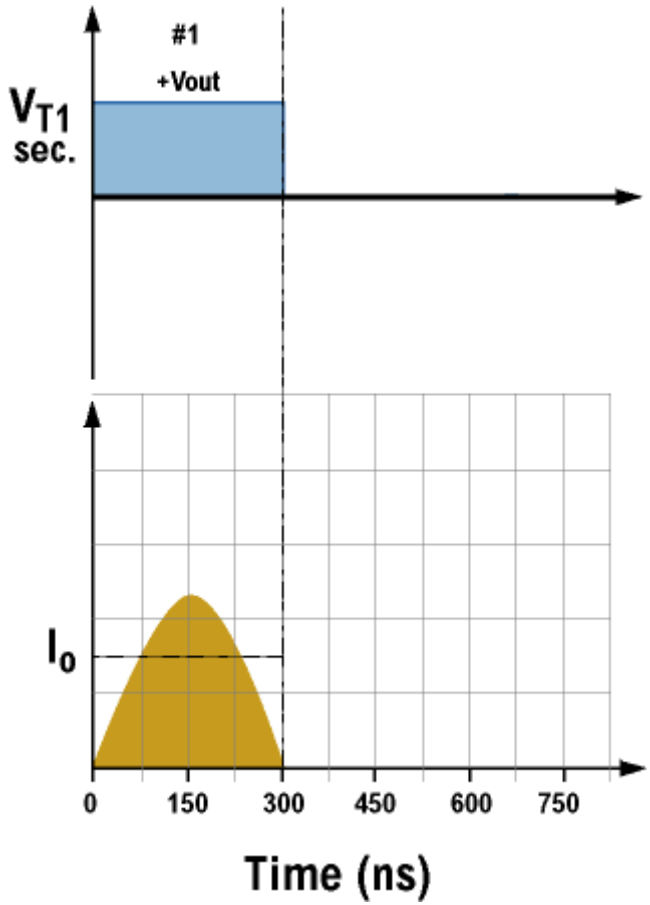
VTM / BCM SAC Control



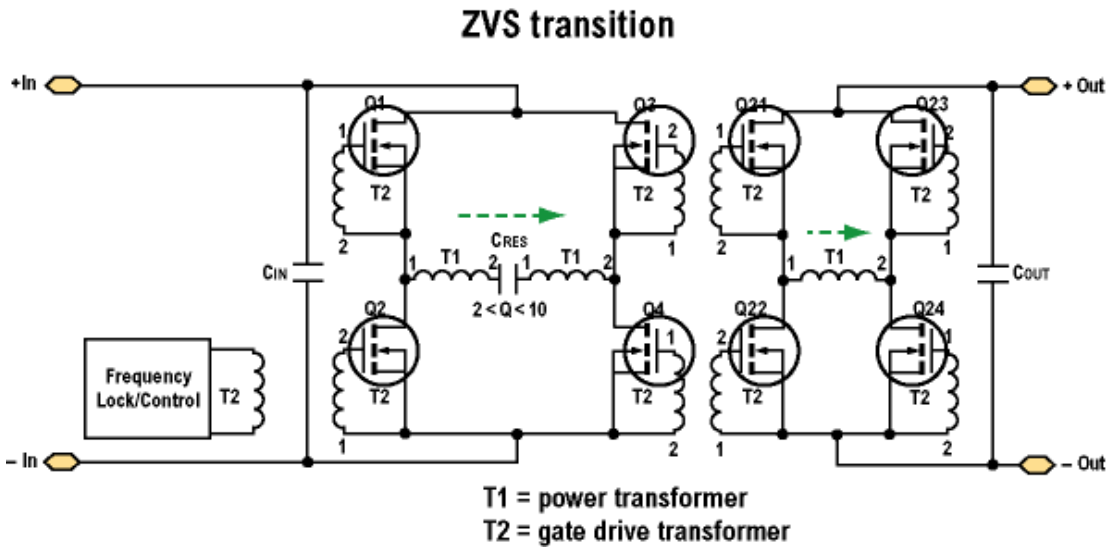
- Control Servo locks to Sine Amplitude Converter resonant frequency and phase, compensating for power train parametric variabilities
- Soft start, inrush control and Adaptive Loop Compensation of Rout

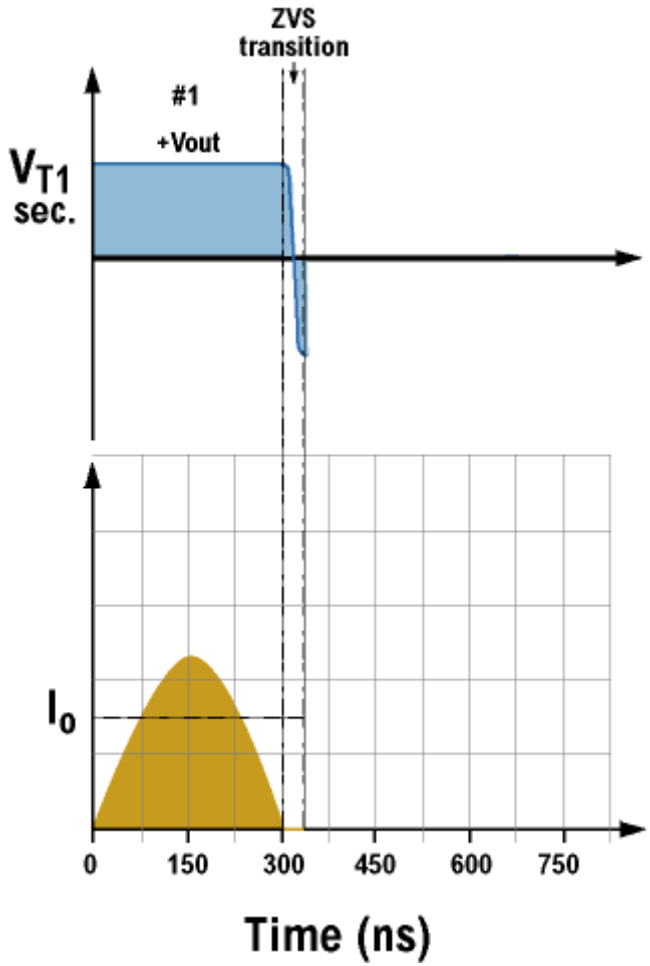
VTM Operation Phases



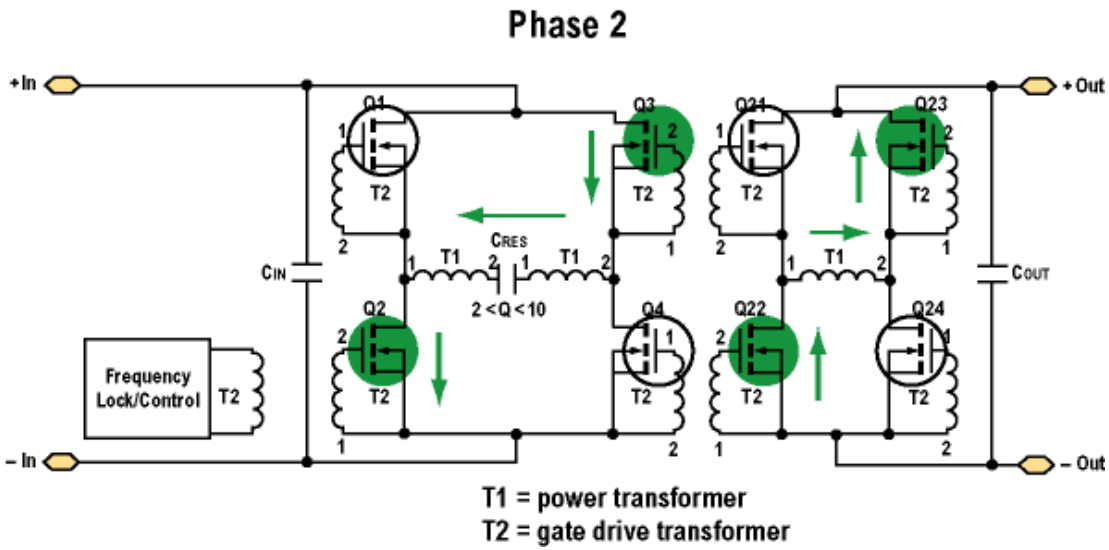


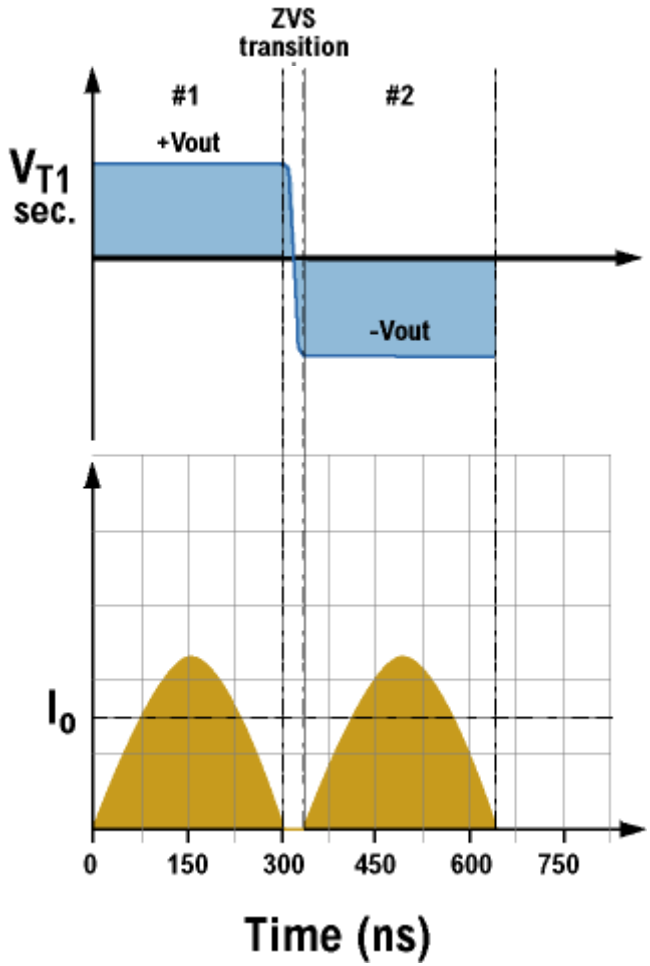
VTM Operation Phases



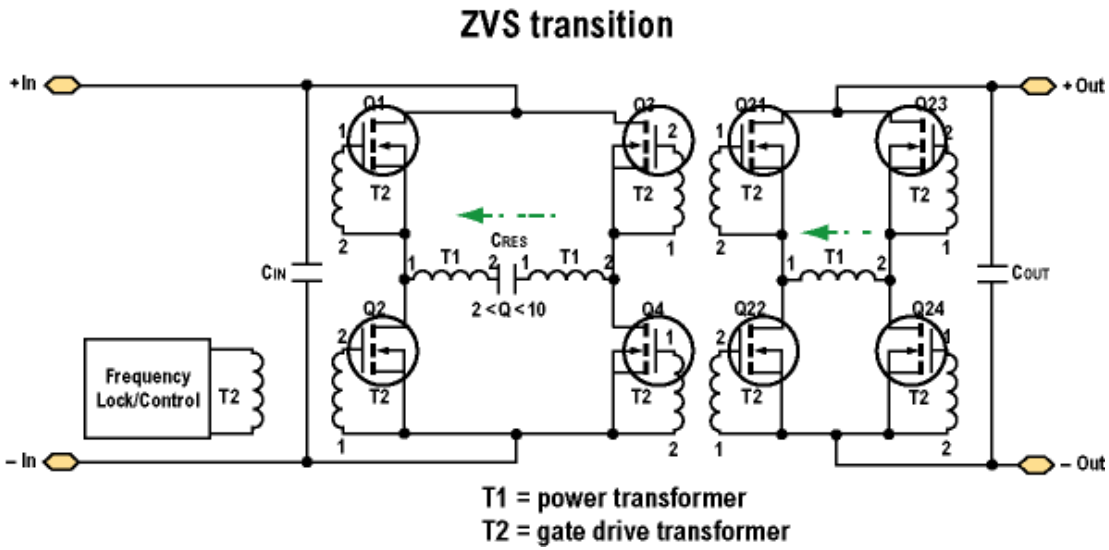


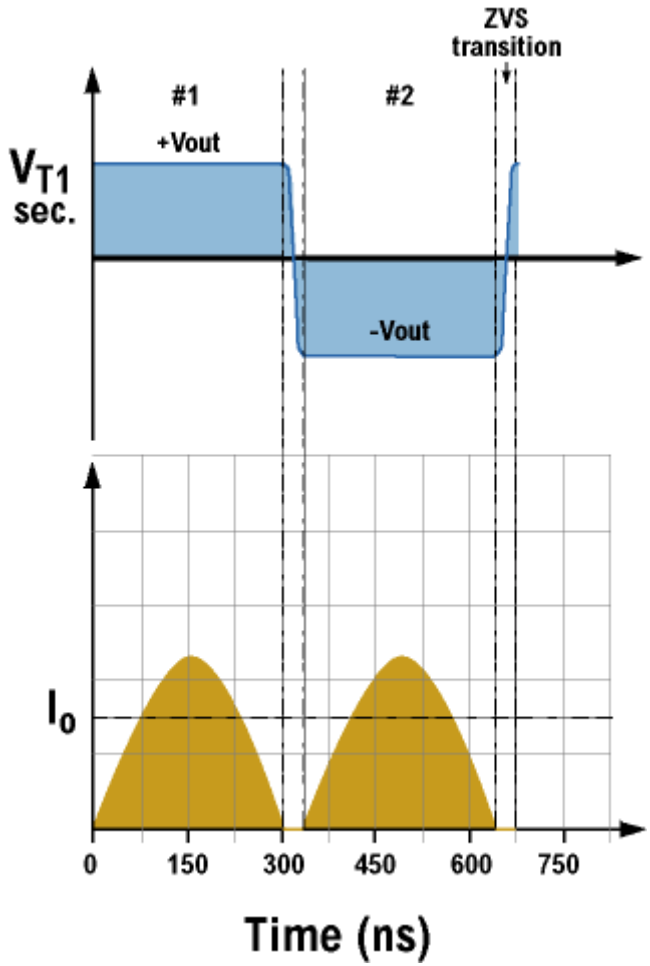
VTM Operation Phases



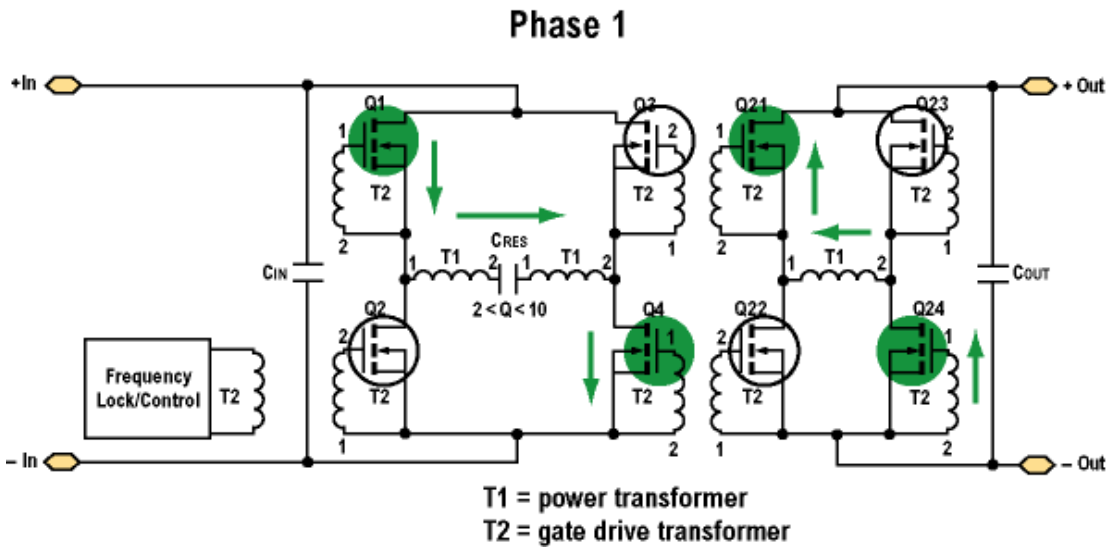


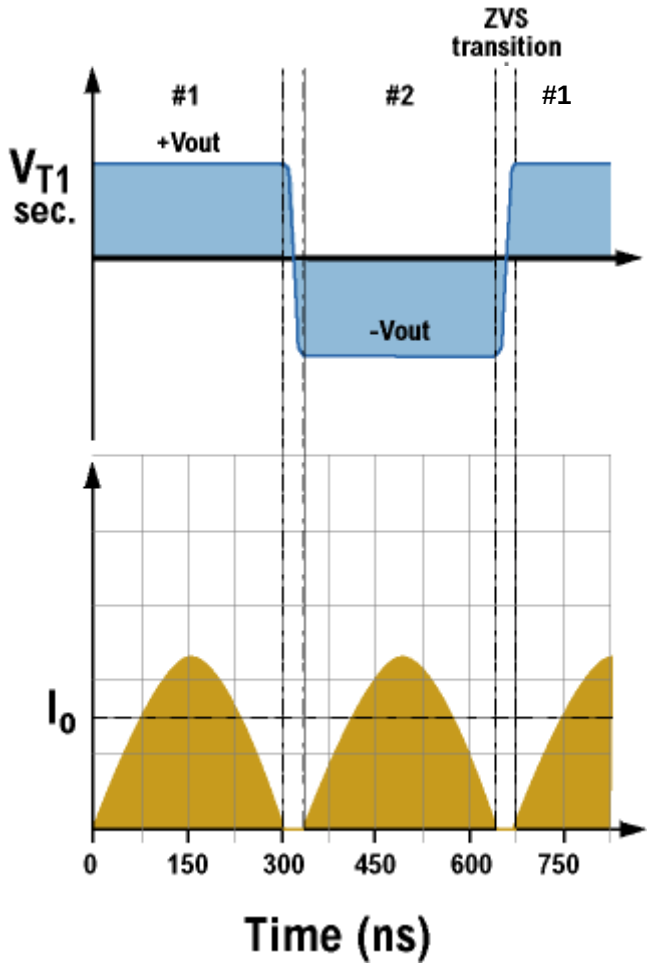
VTM Operation Phases





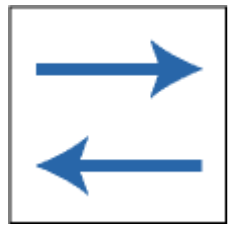
VTM Operation Phases



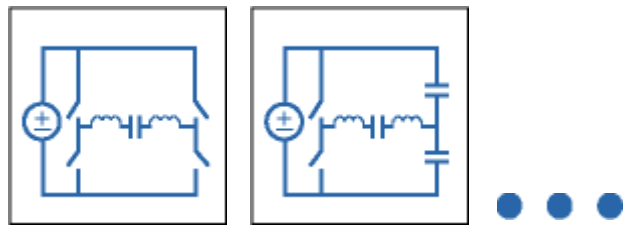


VTM / BCM SAC Engine – Additional Features

- Bi-directional power transfer



- Flexibility of topology



- Common-mode cancellation

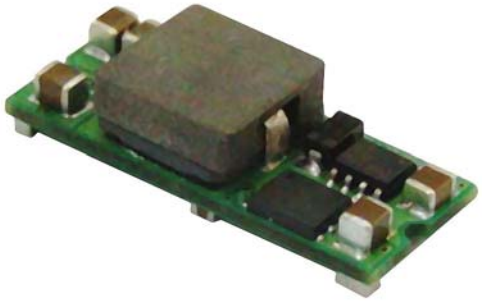
Superior System Performance

- Higher power/current density
  - Power conversion building blocks occupy less space
- Higher efficiency
  - Power conversion building blocks generate less heat
- Faster transient response
  - Overcomes processor/power technology gap
- Lower input and output noise
  - Reduced filtering frees up board space

SAC: Highest Power Density

- High fixed switching frequency (up to 4 MHz)
  - Reduces size of all reactive components
- Zero-current & zero-voltage switching (ZCS/ZVS)
  - Reduces stresses, losses and heat
- No serial energy storage
  - No output inductor
- 100% effective transformation duty cycle
  - Efficient power train utilization

From niPOLs to VICs



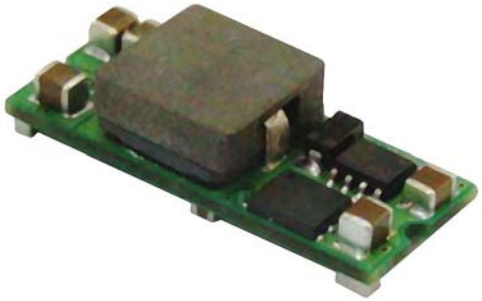
16 A / 80 W niPOL

- Surface mount
- Efficiency: 12 Vin to 1.2 Vout = 83%
- 1.30" x 0.53" x 0.37"
  (33,0 mm x 13,5 mm x 9,3 mm)
- Area: 0.7 in^2 (4,5 cm^2)
- Volume: 0.25 in^3 (4,1 cm^3)

100 A / 300 W V•I Chip

- Surface mount
- Efficiency: 48 Vin to 1.2 Vout = 91%
- 1.26 " x 0.85" x 0.24"
  (32,0 mm x 21,5 mm x 6,0 mm)
- Area: 1.1 in^2 (6,9 cm^2)
- Volume: 0.26 in^3 (4,1 cm^3)

From niPOLs to VICs



16 A / 80 W niPOL

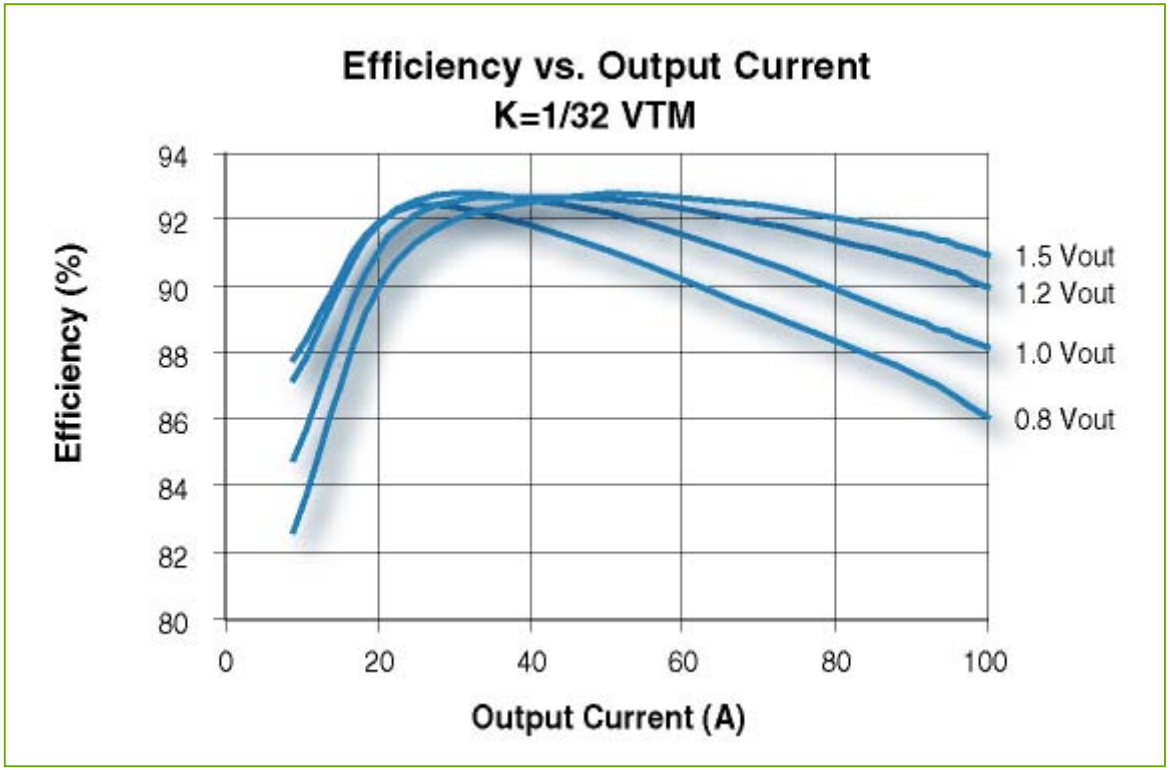
100 A / 300 W V•I Chip

320 W/in^3	→	1,095 W/in^3
64 A/in^3	→	365 A/in^3
114 W/in^2	→	270 W/in^2
23 A/in^2	→	91 A/in^2

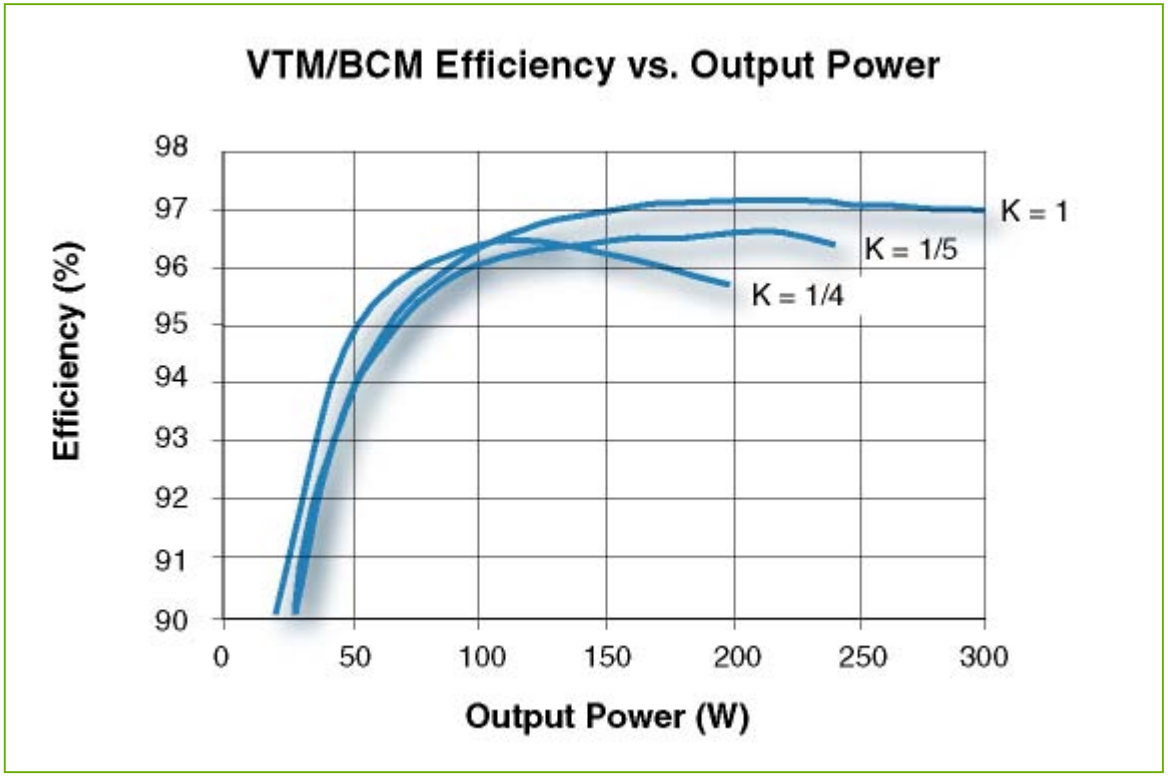
SAC: Highest Efficiency

- ZCS / ZVS
  - No switching losses
- Low Q transformer
  - Reduced winding losses
- No serial energy storage
  - No inductor losses
- 100% effective transformation duty cycle
  - Efficient power train utilization

Efficiency


Efficiency vs. Output Current
K=1/32 VTM
Efficiency (%)
94
92
90
88
86
84
82
80
0
20
40
60
80
100
Output Current (A)
1.5 Vout
1.2 Vout
1.0 Vout
0.8 Vout

Efficiency

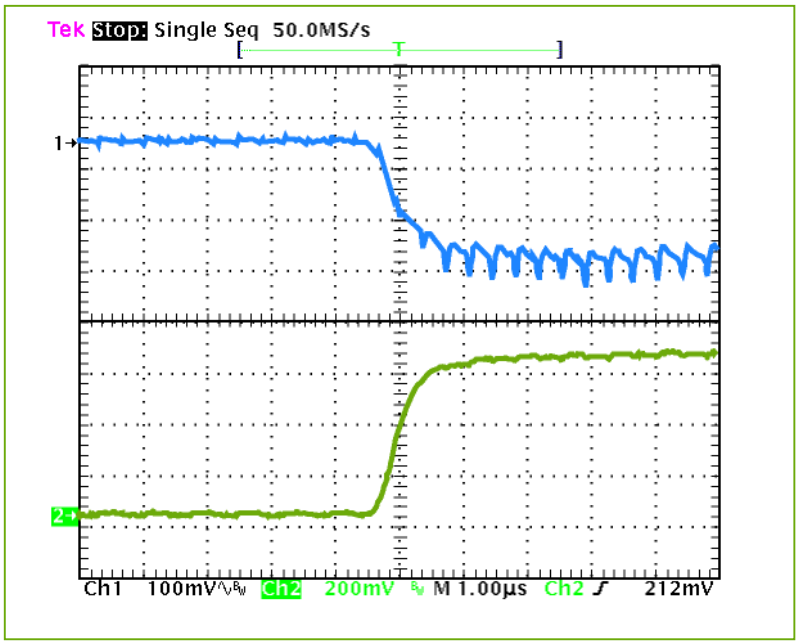

VTM/BCM Efficiency vs. Output Power
Efficiency (%)
98
97
96
95
94
93
92
91
90
0
50
100
150
200
250
300
Output Power (W)
K = 1
K = 1/5
K = 1/4

SAC: Fastest Dynamic Response

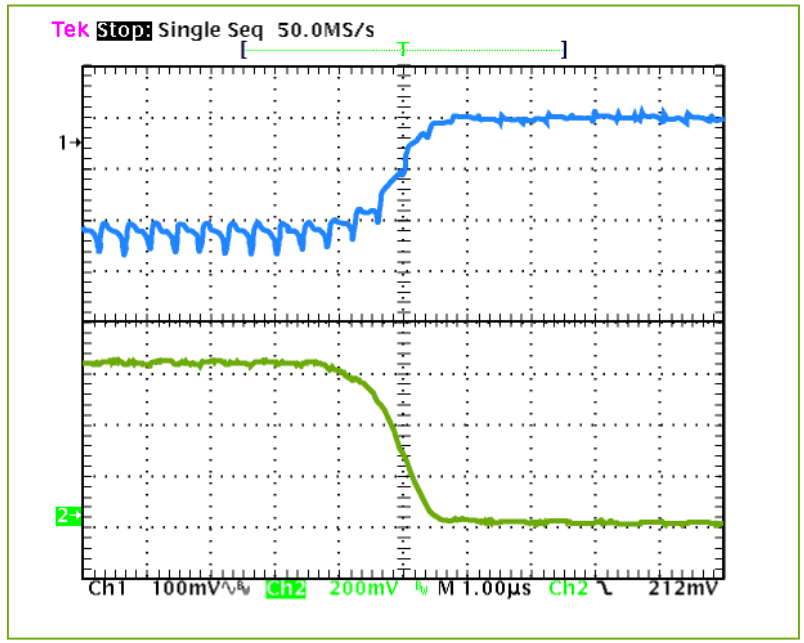
- No serial energy storage & Low Q transformer
  - No current inertia & quick settling
- High fixed switching frequency (up to 4 MHz)
  - Minimal cycle-to-cycle delay
- Load independent control
  - No lag due to control loop
- Bi-directional power processing
  - Load dump energy recycled to input
- Capacitance multiplication
  - High effective POL capacitance: $Cout_{(eff)} \sim Cin \bullet (1/K)^2 + Cout$

Dynamic Response

K = 1/32 VTM @ Vout = 1 V



0 – 100 A load step with 100 **µ**F input capacitance and NO output capacitance



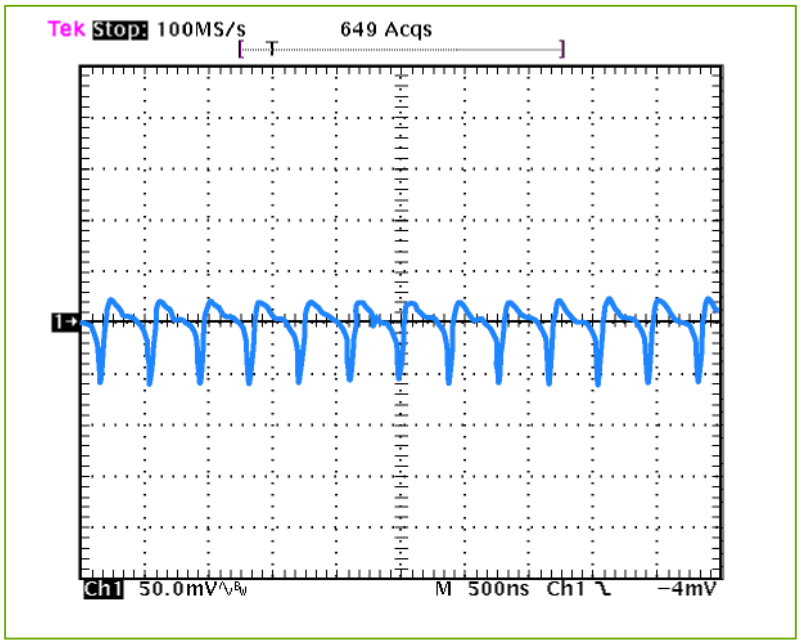
100 – 0 A load step with 100 **µ**F input capacitance and NO output capacitance

SAC: Lowest Noise

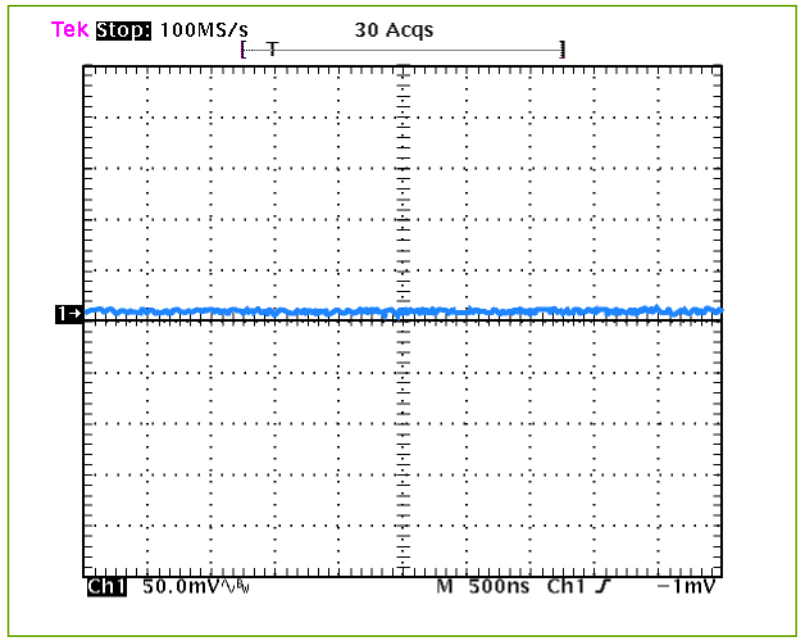
- ZCS/ZVS
  - Order of magnitude reduction in *dI/dt*
  - Significant reduction in *dV/dt*
- Symmetric power train
  - Cancellation of common-mode noise
- High fixed switching frequency (up to 4 MHz)
  - Easy to filter

Output Noise

K = 1/32 VTM @ 1.0 V & 100 A



Output voltage ripple @ 100 A
with NO bypass capacitance

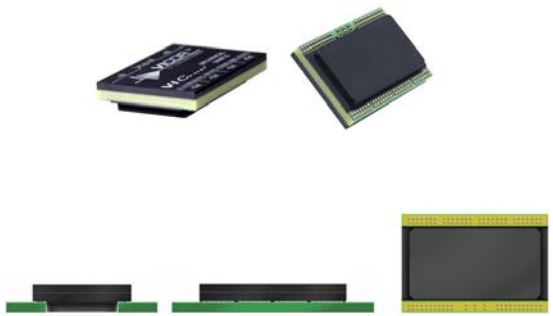


Output voltage ripple @ 100 A
with 200 **µ**F ceramic bypass capacitance and
20 nH distribution inductance

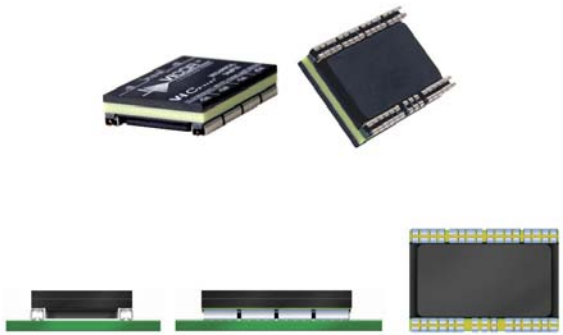
The Flexibility of FPA

- Most contemporary power systems are a hybrid of centralized, distributed and intermediate bus
- Factorized power building blocks support existing power distribution architectures

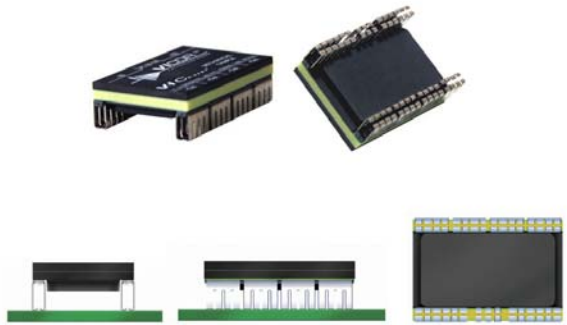
V•I Chip Package Flexibility



Surface mount BGA package
for in-board mounting



Surface mount J-Lead package
for on-board mounting



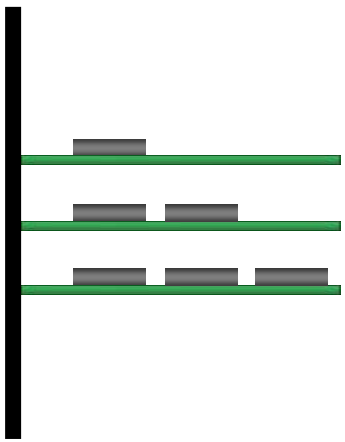
Surface mount extended J-Lead
package for on-board mounting

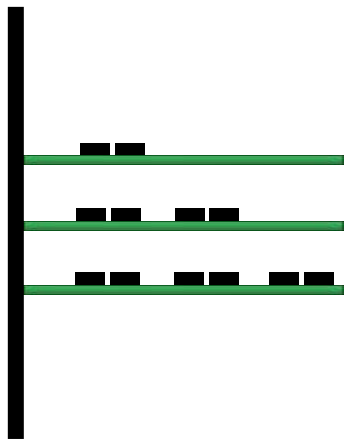
Intermediate Bus

- VTMs function as intermediate bus converters (BCMs)
- More power and more performance in less space

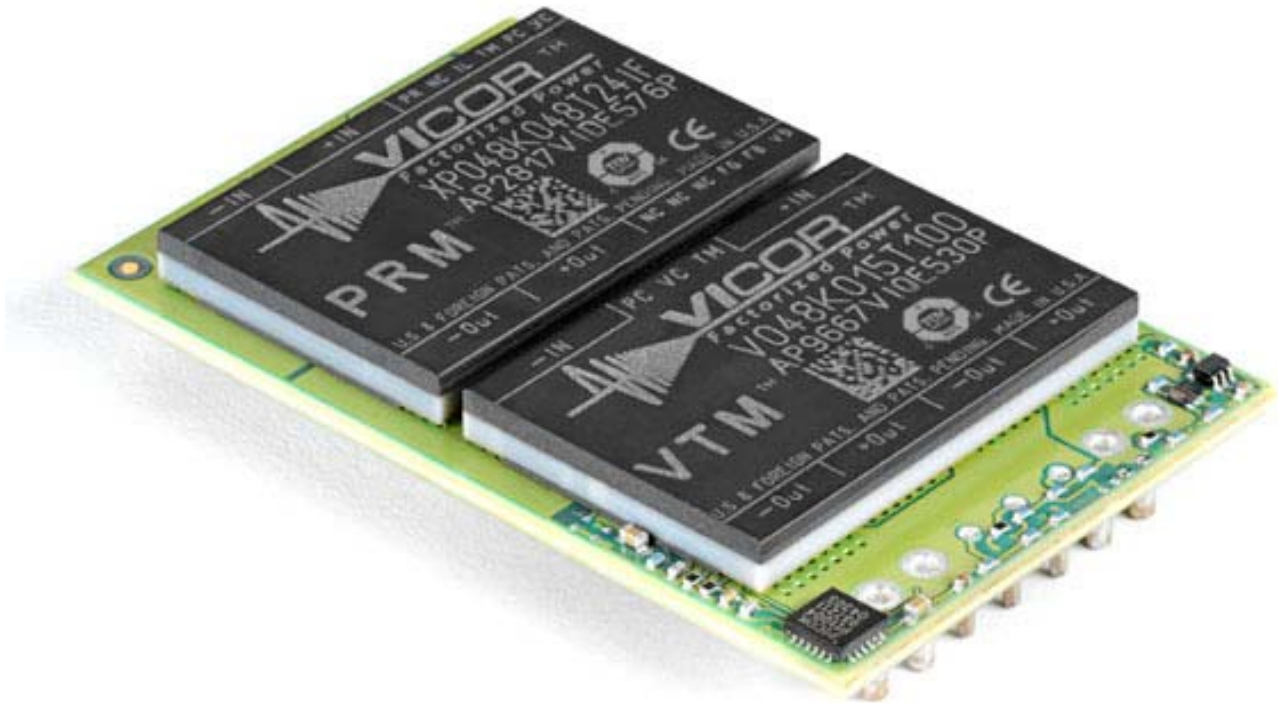
Distributed Power

- A PRM and VTM pair can replace bricks
- Superior performance at less cost



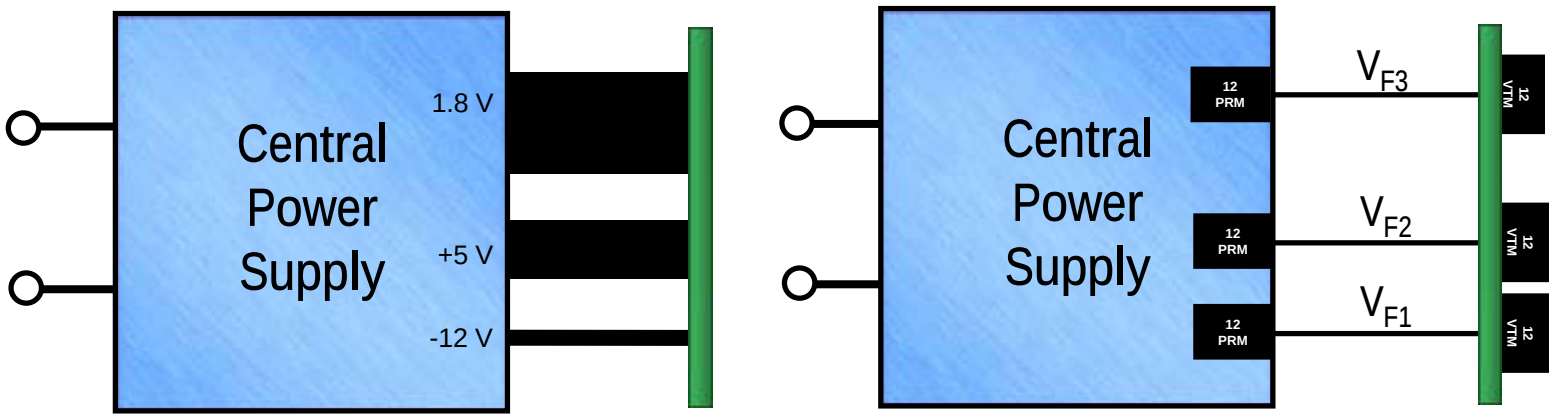


VICBrick – Up to 100 A in a 0.25" High Quarter-brick Package



Centralized Power

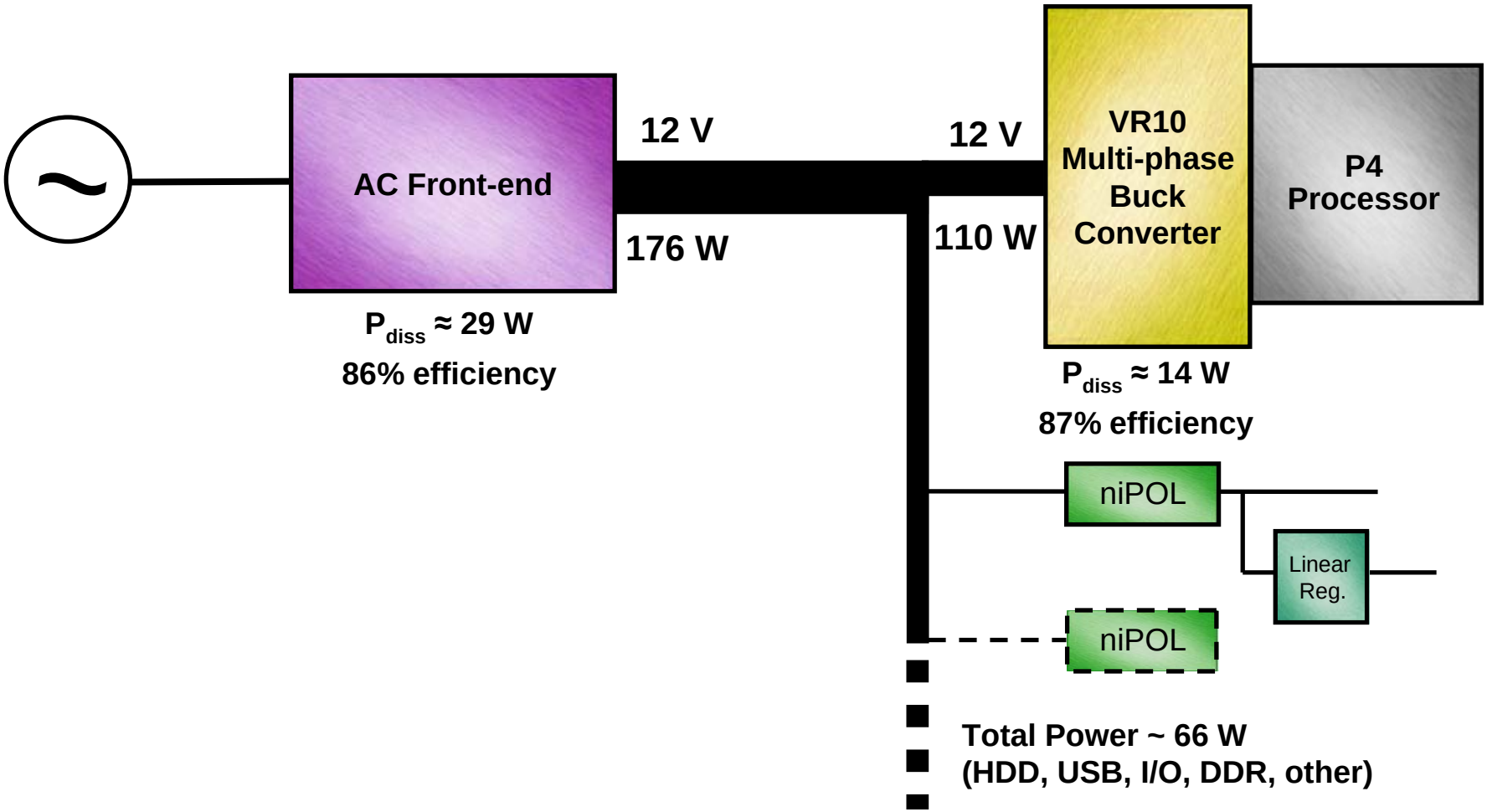
- PRMs can be remotely located
- Low current factorized buses can be easily routed throughout the system



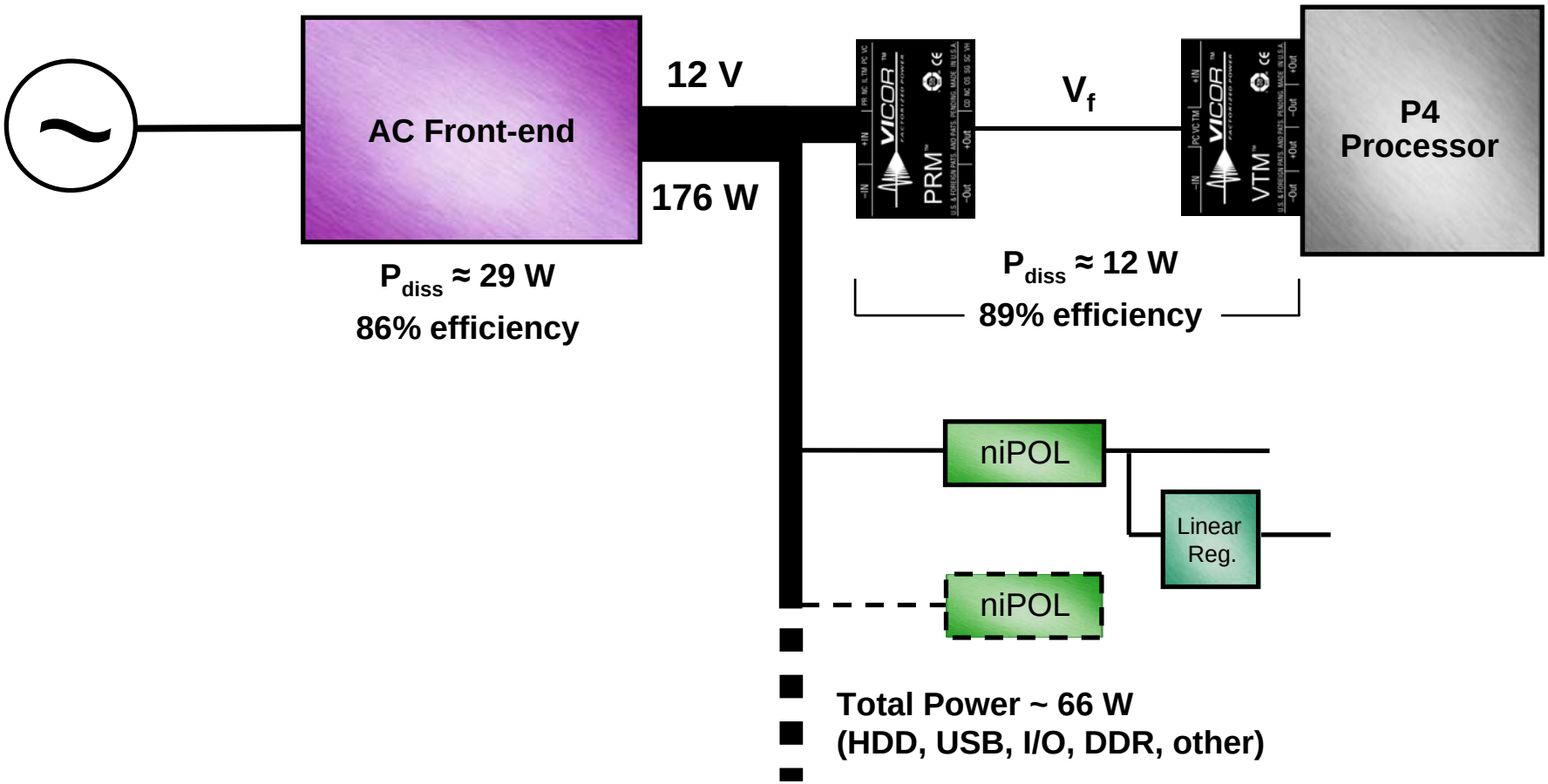
From the Wall Plug to the Processor Core

150 – 200 Watt FPA Solution

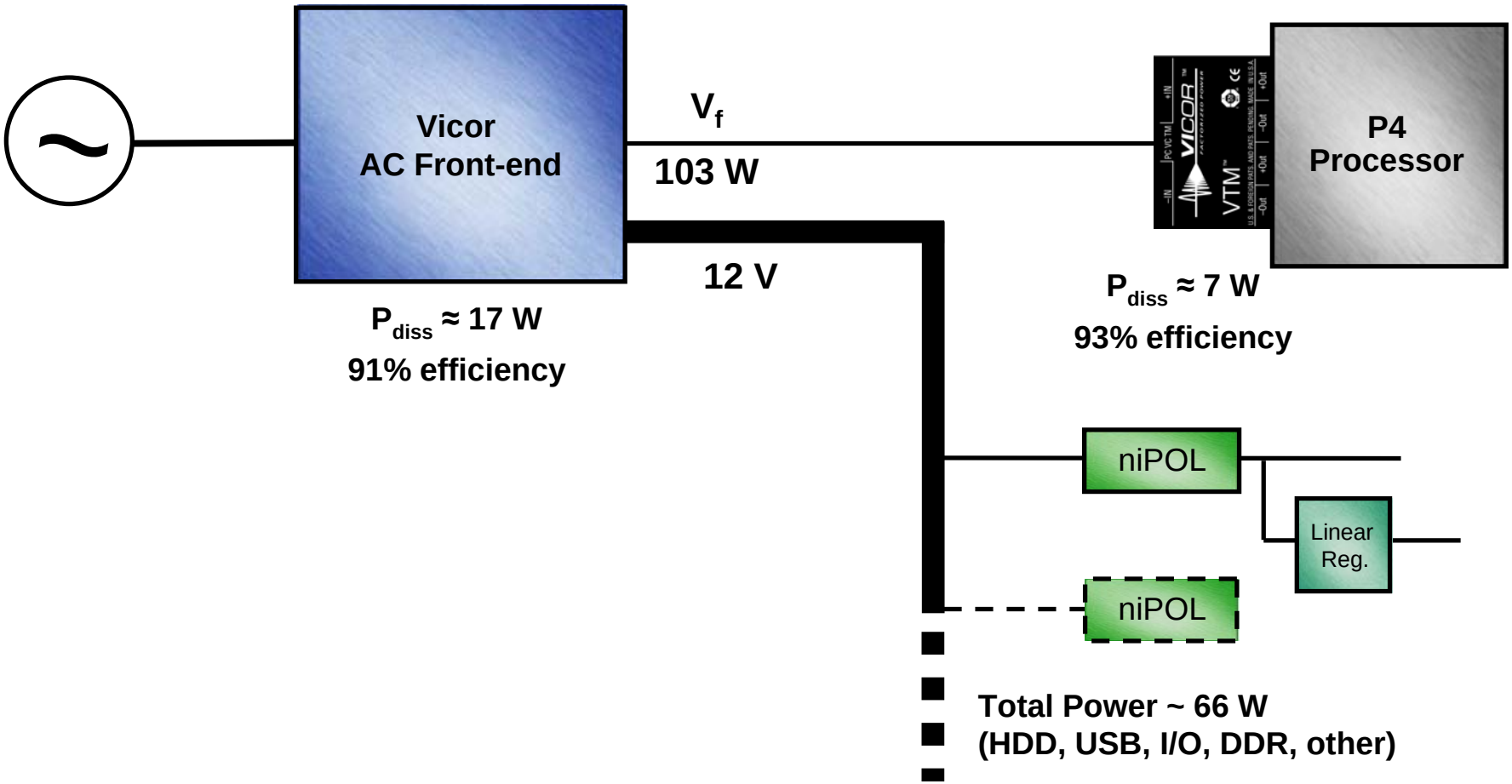
Conventional Power System Architecture
12 V Intermediate Bus



12 V Input PRM/VTM Sub-system



Advanced Processor FPA System



Comparative Benchmark

	Conventional Pentium 4 Power System	12 V Input PRM / VTM Sub-System	Advanced Processor FPA System
Front-end			
Efficiency	86%	86%	91%
Power dissipation	18 W	18 W	11 W
Power density	6.6 W/in^3	6.6 W/in^3	25 W/in^3
POL (processor)			
Efficiency (1.2V @ 80 A)	87%	89%	93%
Power dissipation	14 W	12 W	7 W
Power density	23 W/in^3	59 W/in^3	120 W/in^3
Total (without auxiliary outputs)			
Efficiency	75%	77%	85%
Power dissipation	32 W	30 W	18 W
Power density	3.2 W/in^3	3.3 W/in^3	11.5 W/in^3

Power Architecture Evolution

Centralized Power (CPA)

Distributed Power (DPA)

Intermediate Bus (IBA)

Factorized Power (FPA)

Which is the Future?

Power Architecture Evolution

Centralized Power (CPA)

Distributed Power (DPA)

Intermediate Bus (IBA)

Factorized Power (FPA)

Fast!
Efficient!
Dense!
From the Wall Plug… to the Processor Core!

FPA & V•I Chips

Power Paradigm of the Future

Questions?