# 350V to12V DC "Yeaman Topology" Power System

Maurizio Salato
Applications Engineering
V·I CHIP Inc., (a VICOR Company)
Andover, MA, U.S.A
MSalato@vicr.com

Peter Makrum
Applications Engineering
V·I CHIP Inc., (a VICOR Company)
Andover, MA, U.S.A
PMakrum@vicr.com

***Abstract*— This paper introduces a new DC/DC power supply architecture, called "Yeaman Topology". The main characteristic of this topology is to separate the output voltage regulation function from the bulk power conversion function, implementing two stages that share a common input, and have their outputs in series. Regulation is achieved by controlling only a fraction of the total output power. Trade-offs exists in optimizing the two stages for this purpose, but significant advantages can be achieved in terms of total efficiency, power conversion density, system life-cycle cost and total cost of ownership.**

## I. INTRODUCTION

High Voltage DC is rapidly gaining traction in industrial computing and telecommunication markets. New facilities are being built, often with 300-400 V DC distribution available. Undoubtedly, the ever increasing power demand of state of the art digital processors drives power system designers toward higher voltages, in order to minimize the distribution losses in large data-centers. This trend is clearly visible in the United States, where high-end computing equipment manufacturers have been adopting 360 V DC as their standard input supply voltage, as well as in some other countries, for example Japan, where important telecommunication companies are working on national code standards on the topic.

Loads in this field can be divided in three main categories: CPUs and memories, Communication Interfaces, and Data Storage. The common power supply architecture for the first category consists of an unregulated Intermediate Bus Converter, followed by a Point-of Load regulator. While this approach is the most viable for extra low voltage loads, it becomes less applicable when the load voltage ranges above 10 V, which happens to be the case for the last two categories.

## II. MOTIVATION

The Yeaman Topology has been conceived for all the applications requiring high efficiency and density for loads in the 10 V to 20 V range, for example Hard Disk Drive storage units. On one end, Intermediate Bus Converters offer isolation, high density and efficiency, because the magnetic and passive filters designs can be optimized for the chosen frequency, at fixed duty cycle. On the other end, regulated switching converters have inherent disadvantages in terms of density and efficiency, as PWM modulation techniques require corner-case magnetics and filters design in order to accommodate for input voltage and output current changes, while maintaining accurate regulation. The average difference in terms of power conversion efficiency performance between state of the art, isolated and regulated converter and an intermediate bus converter is 10%, which is a very significant gap in high density environments.

The proposed architecture optimally merges unregulated bus conversion advantages (efficiency, size, simplicity) with the benefits of classic regulation (dynamic response, accuracy); it relies on commercially available technologies, and can be built with off-the-shelf components.

## III. PROPOSED SYSTEM

In essence, the Yeaman Topology consists in processing majority of the output power through a single switching power stage, built as an Intermediate Bus Converter (BCA in Fig. 1). At any time and under any condition this unregulated "bulk" power conversion stage would reach the desired output voltage level. The regulated stage (FPA in Fig. 1) output is connected in series with the BCA output, sharing the load current but providing only the voltage needed to reach the desired level under any load, line and temperature condition. A differential remote feedback loop senses the total output voltage and, through the regulator, dynamically adjusts the load voltage to the target. The complete power system efficiency will therefore be the average of the two blocks (FPA and BCA) efficiencies, weighted by their individual output voltages, as shown in Eq. (1) and Fig. 2.

$$\eta_{Total} = \frac{V_{FPA} \cdot \eta_{FPA} + V_{BCA} \cdot \eta_{BCA}}{V_{OUT}} \qquad (1)$$

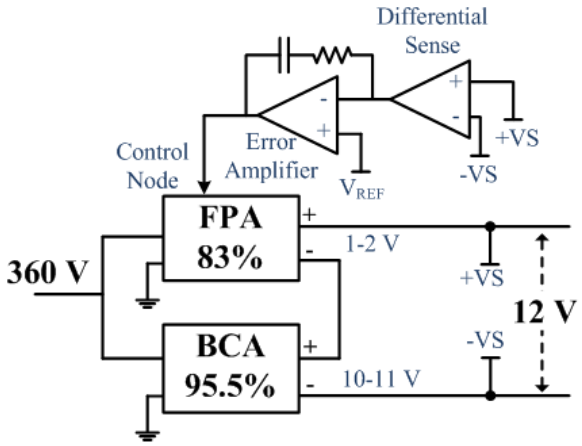


Figure 1. Proposed Architecture Block Diagram

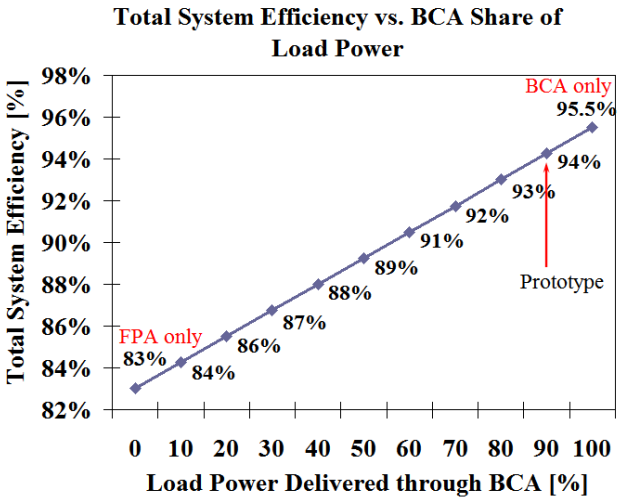


Figure 2. Total System Efficiency vs. share of Load power delivered through BCA

The proposed topology has some peculiarities that need to be considered for successful implementation.

1) *Output series connection and bypass*: because the two blocks have their outputs connected in series, it is very important to provide a path for the circulating load current, should any of the two blocks turn off for any reason. The simplest approach would be a by-pass rectifier; a more efficient approach can be a sustained operation of synchronous rectifiers on the output stage of each converter.

2) *Start-up sequencing and control:* because the control system relies on total output voltage feedback, it is important to coordinate the start-up sequence such that both converters contribute to the output voltage immediately. Alternatively, the feedback can be activated only when the regulator block is active, providing that the bus converter block is already operating.

3) *Supply line stability reflected on Load Voltage:* intermediate bus converters behave most of the time as broadband transformers. As such, they effectively transfer the input line characteristics to the output and vice versa. This needs to be accounted for in the regulated output voltage dynamic characteristic, as the equivalent voltage supply (in the frequency domain) applied to the load will be a combination of the input line complex impedance characteristic, as transferred by the bus converter, and the regulated supply complex output impedance characteristic, as provided by the PWM (or equivalent) control.

4) *Protections:* protections need to be coordinated between the two stages as well, as the regulator block has a limited dynamic range with respect to the output voltage, and the bus converter block typically has no current limit capabilities.

## IV. Experimental Results

An experimental system has been built, with the characteristics listed in Table I.

TABLE I. Experimental System Characteristics

| Specification | Value |
|---|---|
| Input Voltage Range | 350 – 365 V |
| Output Voltage | 12 V |
| Output Power | 1344 W |
| Regulation Accuracy | 0.5 % |

The system building blocks have been chosen within the V·I Chip family of standard products as following:

A. *Bus Converter Module*, BCM [3]: isolated, unregulated front-end electronic transformer Zero Voltage Switching (ZVS), Zero Current Switching (ZCS) enabled by resonant Sine Amplitude Conversion (SAC) topology, shown in Fig. 3.

B. *Pre-Regulator Module*, PRM [4]: non-isolated system regulator implemented with ZVS buck – boost topology, shown in Fig. 4.

C. *Voltage Transformation Module*, VTM [5]: isolated, unregulated point-of-load electronic transformer also implemented with SAC topology, shown in Fig. 3.

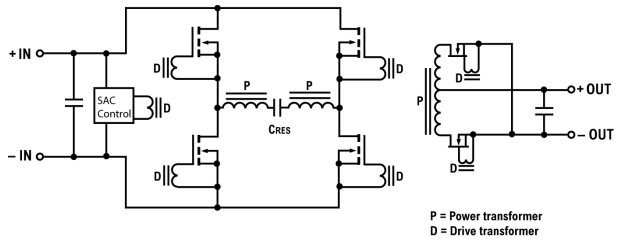


Figure 3. BCM and VTM Topology

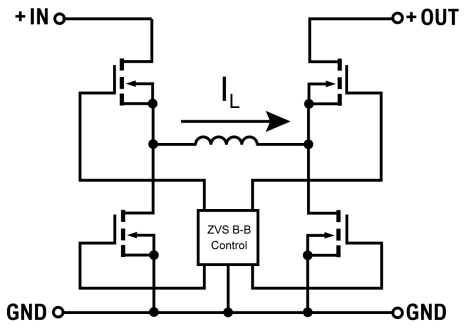


Figure 4. PRM Topology

With reference to Fig. 5, three devices constituted the regulated FPA block, built with V·I Chip Factorized Power modules ($BCM_2$ with a transformer ratio of 8 to 1, 38 V to 55 V $PRM_2$ and a 1-1.7 V output, 200W $VTM_2$) and four devices constituted the unregulated bus converter block, built with V·I Chip BCM bus converters modules (with a transformer ratio of 32 to 1). The BCA array outputs an unregulated voltage ranging between 10 V and 11 V; the FPA regulates between 1 V and 2V; the two provide 12 V, up to 112 A to the Load.

In the analyzed example, $VTM_2$ has been selected with a nominal output voltage of 1.5 V. If the entirety of the power was processed through the FPA the total efficiency would be 83%, which represents the lowest value that could be reached for the Yeaman topology. Similarly, for a single stage BCA array the efficiency is 95.5% which represent the highest efficiency achievable. Both BCA and FPA output voltage ratios with the total output define the amount of power flowing through each block, given that they are in series and share the current. Fig. 6 shows the obtained efficiency versus output power, which peaks at 94% for a 900W load.

The lower the BCA input voltage, the higher the contribution of the FPA. For this reason, a clamp circuit has been added to the control node in order to guarantee a maximum FPA output voltage across line and load. Fig. 7 shows that, at low line, the FPA output is clamped around 1.5 V and as the BCA input voltage increases, the total system output goes into regulation. It also shows the drooping characteristic for input voltages lower than 350 V, which is a desired feature in the analyzed case.

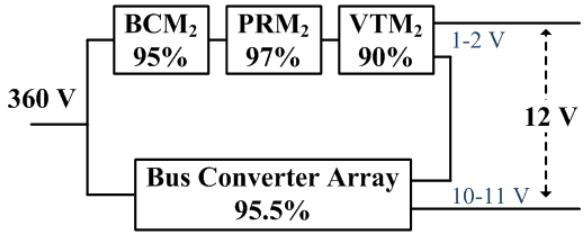


Figure 5. Proposed Architecture Block Diagram

Few considerations are worth mentioning:

- The input line range should be given first consideration when designing the Yeaman topology. The feedback loop, through differential remote sense, will manage the load regulation within target. The output voltage range of the BCA unregulated stage will naturally follow the input line range. The FPA output voltage is expected to compensate for this, therefore imposing a wider FPA output range. Given the same BCA transfer ratio and output voltage, the higher the FPA output voltage the less power transferred though the BCA stage which implies lower total system efficiency.
- Control logic is required to provide startup, shutdown sequencing and protection coordination between FPA and BCA. It is recommended to hold the regulating stage in the FPA disabled at startup. In the analyzed case, the $VTM_2$ are designed such that externally provided auxiliary power will maintain their output stage synchronous rectification active, therefore providing the bypass for the load current even in absence of regulated voltage.

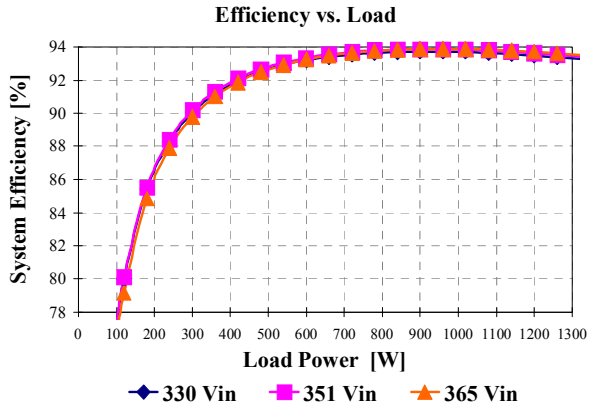


Figure 6. Experimental System Efficiency vs. Line and Load

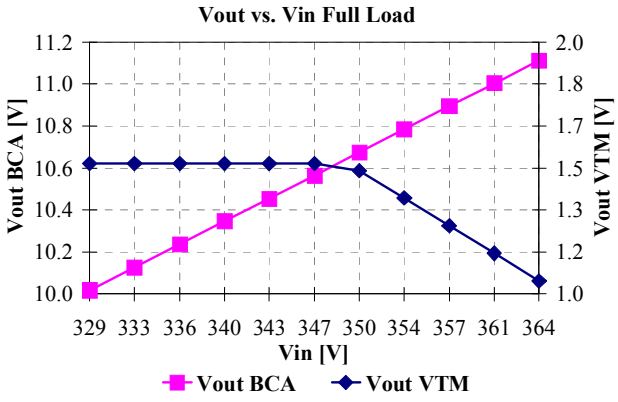


Figure 7. Experimental System Output Voltage vs. Input Line Voltage at Full Load

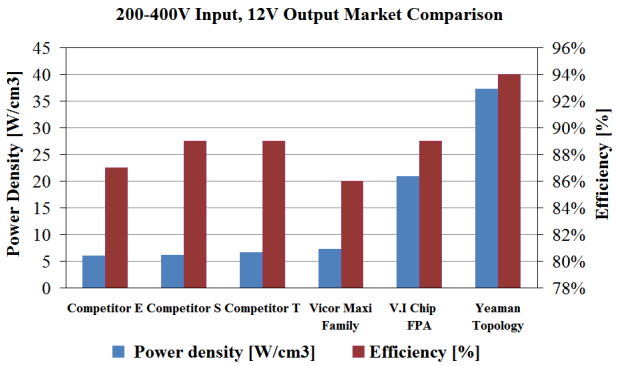


Figure 8. Comparison of solutions available on the market, 200-400 V input, 12 V Ouput, 500-1000 W

## V. COMPARISON WITH STATE-OF-THE-ART SOLUTIONS

A comparison in terms of power density and efficiency between the Yeaman topology prototype and equivalent products available on the market is shown in Fig. 8. While FPA alone can improve power density over industry standards by a factor of 4, the Yeaman topology offers an improvement by a factor of 7. On efficiency, the reduction in conversion power losses approaches 50%. This offers to system designers the opportunity to significantly reduce the total system cost, abating the size of the power system and, most importantly, the cooling requirements.

## VI. CONCLUSION

The Yeaman architecture is ideal for high power, high density applications where cooling is at a premium and efficiency is paramount. The experimental system was able to provide 1.3 kW at 12 V, 94% efficiency in less than 54cm$^2$ of PCB space


## ACKNOWLEDGMENTES

The authors would like to thank Paul Yeaman, for the original idea on the topology, and the Application Engineering Team at V·I Chip, for the support provided on this effort.


## REFERENCES


[1] V•I CHIP Inc., *Factorized Power Architecture and V•I Chips*, White paper, May 2007, (http://www.vicr.com/cms/home/products/vi-chip/vichip_app_notes_white_papers).

[2] Paul Yeaman, *Using BCM™ Bus Converters in High Power Arrays*, Application note, June 2010, (http://www.vicr.com/cms/home/products/vi-chip/vichip_app_notes_white_papers).

[3] V•I CHIP Inc., *BCM™ Converter Module*, Datasheet, (http://www.vicr.com/cms/home/products/vi-chip/vichipBCM).

[4] V•I CHIP Inc., *PRM™ Pre-Regulator Module*, Datasheet, (http://www.vicr.com/cms/home/products/vi-chip/vichip_PRM_regulators).

[5] V•I CHIP Inc., *VTM™ Voltage Transformer Module*, Datasheet, (http://www.vicr.com/cms/home/products/vi-chip/vichip_VTM_transformers).