POWER SOLUTION BRIEF

Leveraging Bus Converters in Regulated DC-DC Applications

–Comparative Study of Yeaman Topology vs. Factorized Power Architecture™

David Bourner
Maurizio Salato

Abstract

FPA™ (Factorized Power Architecture™) has provided leverage in solving demanding power challenges which call for high levels of efficiency, power density and superior power handling and dynamic load capability. A variant on FPA that utilizes a Power Component Methodology is described. Solutions framed within the FPA framework are compared against those instantiated in the YT (Yeaman Topology). A description of the investigation methods used and outcomes of various tests to establish performance metrics follow. Practical aspects of applying power components to both FP and YT architectures are followed by a summary of salient attributes for each system.

Background

The need for high-density, high-efficiency power conversion has led industrial research toward advanced power-system architectures.[a][b] These approaches involve optimized sub systems, often implemented as power components that out perform traditional, discrete designs from electrical, thermal and mechanical assembly standpoints.[c][d] This paper presents a comparison between Factorized Power Architecture (FPA)[a] and Yeaman Topology (YT)[e] in a regulated, high-density DC-DC application. YT can maximize the use of bus converters in array configuration[f], therefore achieving higher density and higher efficiency than FPA, if input and output voltage ranges in the application can be maintained relatively constant and their relative ratio is close to an even integer.

A building-block based approach to power converter design

Resonant converters have been known for quite long time[g] and most power supply designers have some level of experience with resonant topologies. A major drawback of such topologies lies in the parametric tuning required in order to guarantee performance over line and load ranges. With inexpensive digital controls being available, optimization of resonant converters has been simplified and algorithms have been built to support it, often in real-time fashion.[h] However, system scalability issues are present, as parametric distribution of standard discrete parts (and in particular their parasitic elements) is simply too large to allow for simple, linear scale design as the converter is sized for different power levels.

In order to overcome these issues, power components have been proposed, where typical power supply functions are implemented (like, for example, regulation, isolation, transformation, etc.) with highly efficient resonant topologies.[i] Tight control over converter parameters and tuning is performed at power component level; the same components are designed to easily operate in a variety of configurations, from simple arrays to completely new power conversion schemes. Let's briefly describe the attributes of the considered schemes: the FPA and the YT.

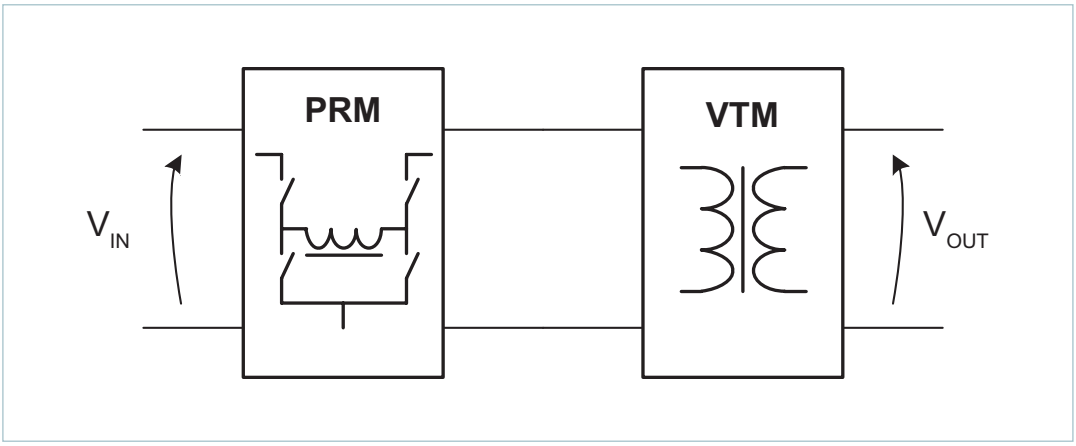
Attributes of the FP and YT architectures

For the purpose of this study, two classes of functionality are considered. The first class consists in a PRM™ (pre-regulator module); it provides non-isolated buck-boost conversion based on ZVS buck-boost switching. The second class consists in either a VTM™ (voltage transformation module) or a BCM (bus converter module); both are based on SAC™ (sine amplitude converter) topology: a soft-switching DC-DC fixed-ratio transformer offering galvanic isolation and a high-efficiency power processing architecture between their primary and secondary sections.

FPA is a system-partitioning rationale that exploits the functional concentration and heightened power density that this approach has demonstrated over CPA (centralized power architecture) or DPA (distributed power architecture) based solutions. The PRM may be its first stage, establishing a fixed voltage which is factored down by a fixed-ratio VTM.

Figure 1 shows the FPA 'kernel'. When a PRM and VTM are linked together, all the attributes of conventional step-down DC-DC conversion can be brought to bear in an environment that accommodates many different operating input voltage ranges, output voltage, current and output power levels.

Figure 1
Factorized Power Architecture block diagram



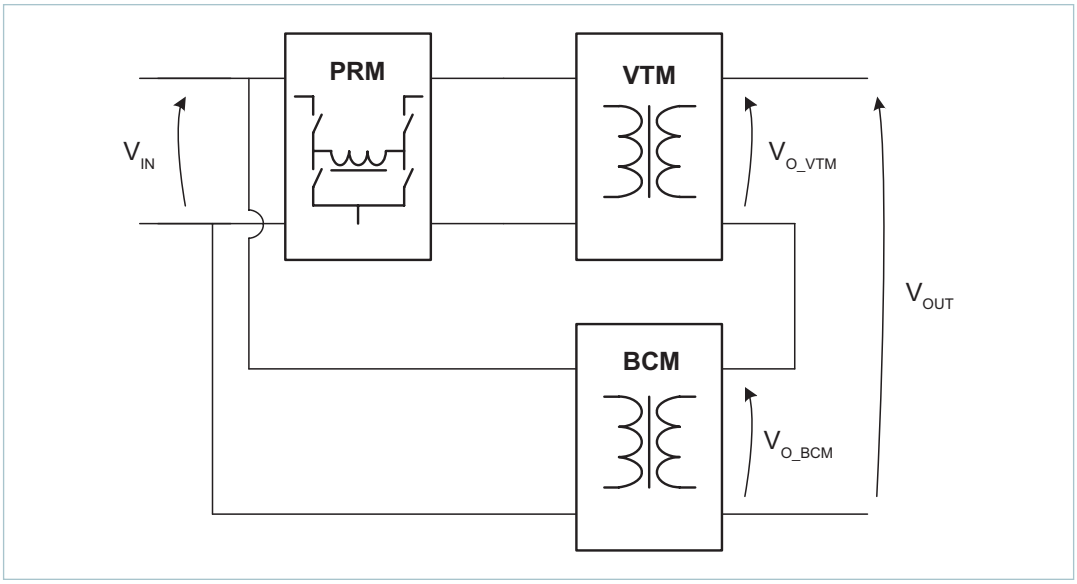
Obviously, the resulting efficiency will be simply the product of the two power components' efficiencies, as shown in Equation 1.

$$\eta_{TOT} = - \eta_{PRM} \bullet \eta_{VTM} \qquad (1)$$

YT exploits FPA as a foundation, adding an independent input-power-processing channel in series with the FPA's output power port. The PRM's regulation is now brought out on remote-sense lines to include the series-connected output ports of both the BCM® as well as the VTM output port. So, instead of processing all of the power through cascaded PRMs and VTMs, most of the power burden is taken up by the higher-efficiency BCMs that do not have regulation capability, leaving the regulation of voltage and the processing of a small part of the output power through the YT to the PRM, factored through the VTM.

Figure 2 shows the YT basic block diagram.

Figure 2
Yeaman topology block diagram



In this case, because the output current is common to BCM® and VTM™ stages, the resulting efficiency is an average of the two power paths (PRM™ + VTM and BCM) weighted by the portion of the output voltage that each path contributes, as shown in Equation 2.

$$\eta_{TOT} = \frac{\left(\eta_{PRM} \bullet \eta_{VTM}\right) \bullet V_{O_{VTM}} + \eta_{BCM} \bullet V_{O_{BCM}}}{V_{OUT}} \qquad (2)$$

The opportunity for YT is therefore to process majority of power through the single stage, highest-efficiency BCM, and "top-off" the output with enough voltage to achieve regulation.

Tests and outcomes

Description of two test applications

Power designers working in molecular computing, IC test equipment and military application areas seem to be on the leading edge of the search for a switched DC-DC converter system that is robust in its operation, yet performs with high precision and speed in the face of very demanding loads. They call for ideal load-line characteristics in both static and dynamic modes of operation.

There are two things that a power designer has to accomplish in order to get a power system to work optimally: Minimal hardware resources need to be matched against the customer's basic power and voltage input / output specification. The selected hardware option then needs to be arranged to be able to successfully start up autonomously into the load and to then perform in accordance with dynamic specifications associated with either a stepped or pulsed load.

Application #1

This application comes from the IC test arena. It is the principle subject of investigation in this study. The customer had a plan to incorporate the same power cell in different parts of the tester: One for a lower load than the other, saving cost as a universal block that could resource both test-head requirements. One of the test-head loads calls for a power solution to source a continuous maximum steady-state load current of 75A at 7.4V, sourced from a 38 – 55V DC power supply. In the other test head, a continuous peak current of 112A is needed. Figure 3 shows the YT topology and component resource allocation required in order to match the needs of the application. Figure 4 shows the corresponding FP configuration.

Application #2

This application is focused on servicing a dynamic load requirement in which a heavily-loaded power system, already drawing 120A at $6V_{DC}$, needs to provide a 65A step in load current within 8.7µs or at a rate of 7.5A/µs, with output voltage varying during the onset of load by no more than ±100mV. The issue of the transient response capability of the topologies can be addressed from the viewpoint of the first application.

Figure 3
YT experimental-set-up block diagram, showing DC voltage ranges across various devices

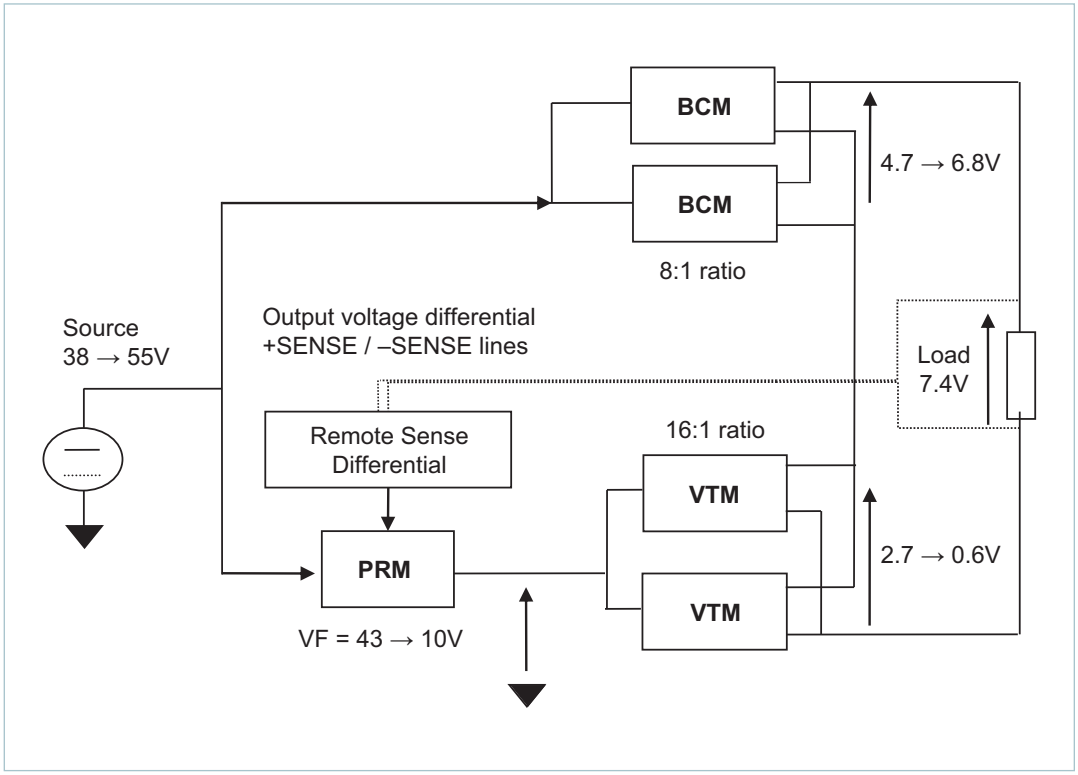
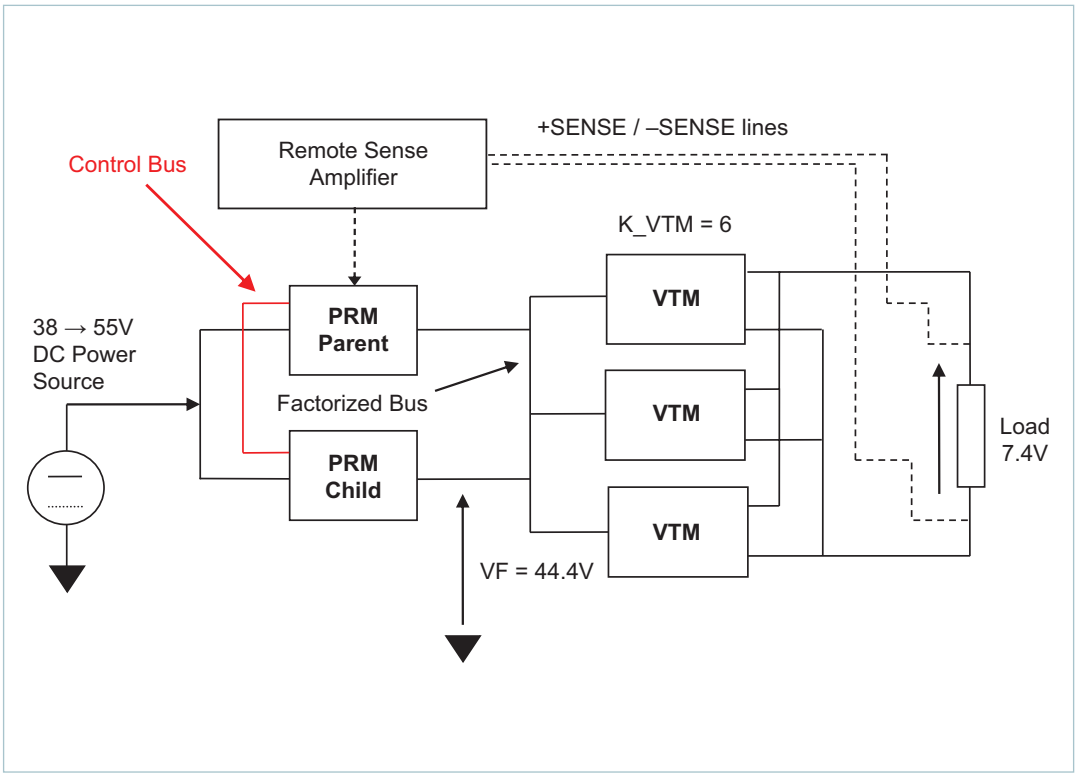


Figure 4
FP experimental-set-up block diagram, showing DC voltage ranges across various devices



Summary of experimental results

Table 1 shows a summary of metrics for both FP and YT topologies drawn up for the 75 and 112A continuous-current-draw scenarios sketched out as part of options in the first application. The targets are couched in terms of the final area and volume of the power solution. These are exceeded by both topologies.

Table 2 compares the performance metrics for the systems whose physical attributes are detailed in the previous table.

These data are interesting to examine, because the power component requirement i.e., the number of devices used is the same irrespective of architecture. So we can continue on with a fair comparison of the solutions along the lines of SWaP (Size, Power Output and Cost), a clear indication being that the YT is more power dense.

It can be seen in Table 1 that the YT configuration can provide higher levels of DC current compared with the FP arrangement.

At the lower average current, the FP can support a higher transient capability. In the higher continuous DC demand scenario, the maximum transient limits are the same.

Table 1
Salient target specifications and attainable physical metrics

V_{IN} Range 38 – 55V_{DC}						
Peak Loads (A) DC / 10msec tran			Total Area (cm^2)		Total Volume (cm^3)	
Target	FP	YT	Target	FP & YT	Target	FP & YT
75 / 112	90 / 135	94 / 120	38.2	35.7	48.2	23.1

Table 2
Performace metrics for each power system implementation

Measurement	Examined Systems	
	FP	YT
Peak Efficiency (%)	92	93.6
No-load Power Dissipation (W)	11.2	11.9
Max Continuous Output Power (W)	664	811
Voltage Regulation (% error)	0.0026	0.004
Current Slew Rate (A/µsec)	9.2	8.7
Post-load Voltage Control Settling Time (µsec)	200	80

In spite of the non-optimal architecting of the YT in this application, it was found that there is an efficiency advantage when using the YT instead of the FP architecture. Figures 5 and 6 show the efficiency characteristics of the FP, YT systems working across their permitted ranges of line and load conditions.

Figure 7 shows the transient characteristics of the YT system to give the reader a picture of the dynamics associated with startup as well as the system's dynamic response. These deserve some comments before summarizing the salient aspects of the different topologies, the subjects of this paper.

Figure 5
Efficiency characteristics vs. line and load

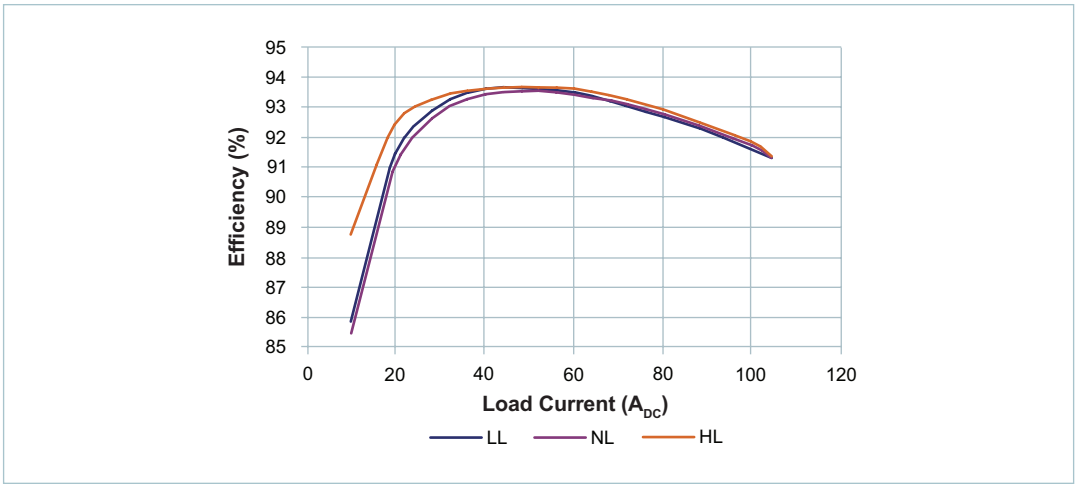


Figure 6
Module line and load efficiency characteristics

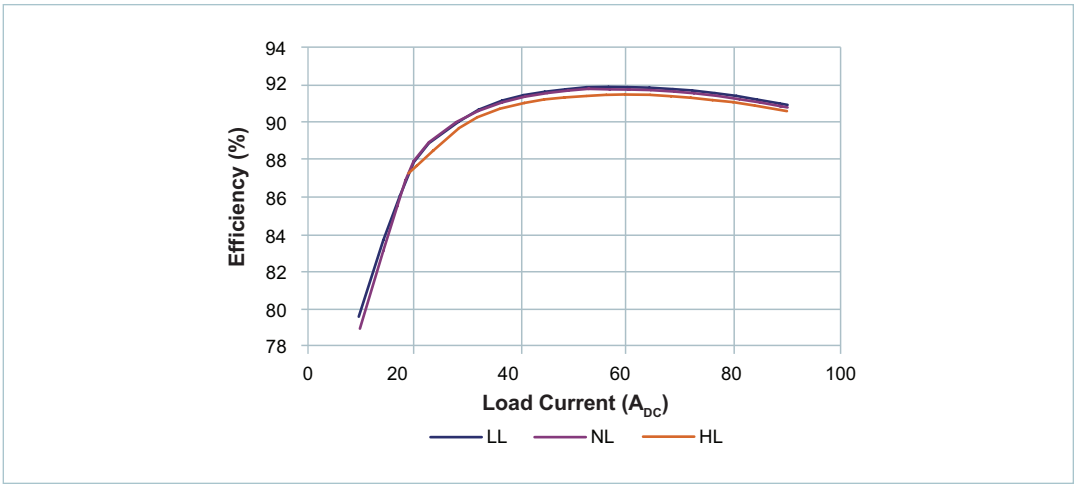
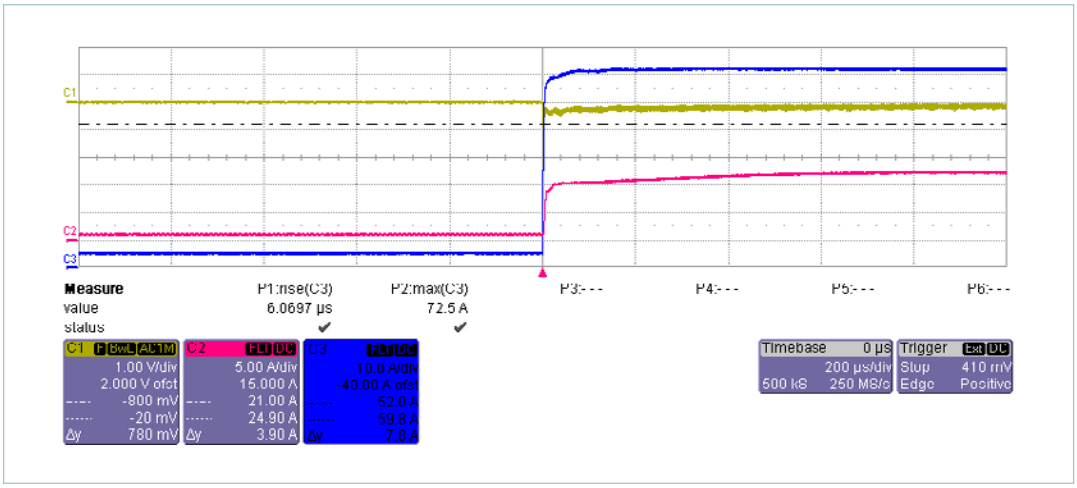


Figure 7
Stepped-load test of YT example hardware. Trace C1 (olive) shows output voltage, C2 (red trace) the input current and C3 (blue trace) output load current



References

[a] Vicor Inc., "Factorized Power Architecture and VI Chips", VICOR White paper, October 2013

[b] Vinciarelli, P., "Power Components Come of Age," *2013 Twenty-Eight Annual IEEE Applied Power Electronics Conference (APEC)*, Long Beach, CA, March 17 – 21, 2013, Opening Plenary Session

[c] Salato, M., "Datacenter power architecture: IBA versus FPA," *2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC)*, pp.1 – 4, 9 – 13 Oct. 2011

[d] Russell, A.T.; Oliveira, E.M.A., "Sine Amplitude Converters for efficient datacenter power distribution," *2012 International Conference on Renewable Energy Research and Applications (ICRERA)*, pp.1 – 6, 11 – 14 Nov. 2012

[e] Salato, M.; Makrum, P., "350V to 12V DC "Yeaman Topology power system," *2010 International Conference on Energy Aware Computing (ICEAC)*, pp.1 – 4, 16 – 18 Dec. 2010

[f] Yeaman, P., "Using BCM® Bus Converters in High Power Arrays", Vicor Application Note, February 2011

[g] Mamon, M.; Hiramatsu, R.; Harada, K.; Sakamoto, H., "A Resonant Converter with PWM Control," *Third International Telecommunications Energy Conference, 1981. INTELEC 1981*, pp.247 – 249, 19 – 21 May 1981

[h] Weiyi Feng; Mattavelli, P.; Lee, F.C.; Dianbo Fu, "LLCconverters with automatic resonant frequency tracking based on synchronous rectifier (SR) gate driving signals," *Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2011*, pp.1 – 5, 6 – 11 March 2011

[i] Salato, M., "Datacenter power architecture: IBA versus FPA," *IEEE 33rd International Telecommunications Energy Conference (INTELEC), 2011*, pp.1 – 4, 9 – 13 Oct. 2011

Contact Us: http://www.vicorpower.com/contact-us

Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715
www.vicorpower.com

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com