

Using the Non-Isolated DCM™ in High-Power Arrays



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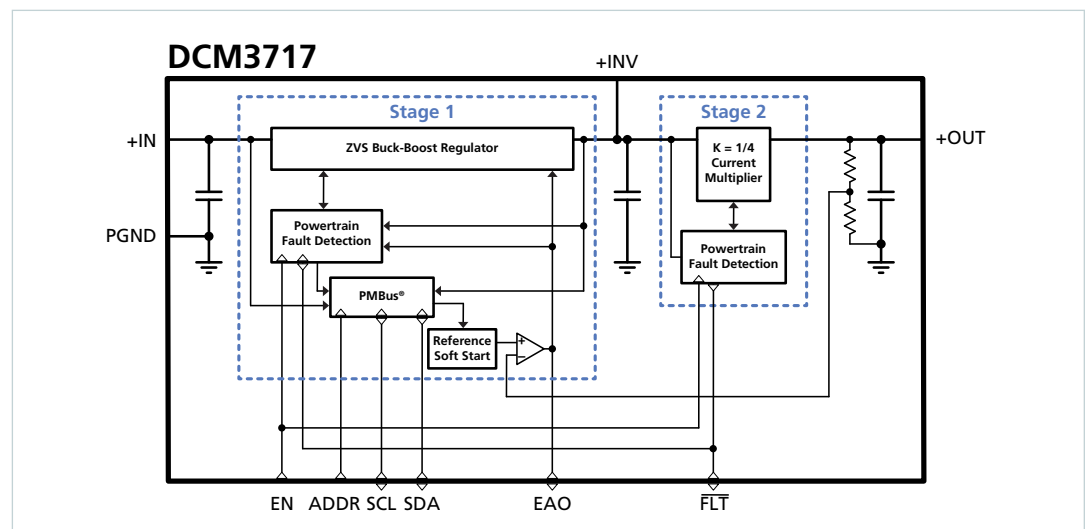


Introduction

This application note applies to the non-isolated SM-ChiP™ DC-DC Converter Module (DCM) family of products targeted for data center applications. A list of these products is provided in Appendix-1. These DCMs consist of Vicor patented zero-voltage switching (ZVS) Buck-Boost regulator followed by a Sine Amplitude Converter (SAC™) current multiplier. DCMs have an internal control loop and operate from a semi-regulated input to generate a regulated point-of-load (PoL) output. No additional external compensation components are required, resulting in substantial savings in application board space and cost. DCMs also feature the thermal density benefits of the Vicor SM-ChiP packaging technology, which offers flexible thermal management options with very low top and bottom side thermal impedances.

Figure 1

Functional block diagram
DCM3717 1kW and 750W



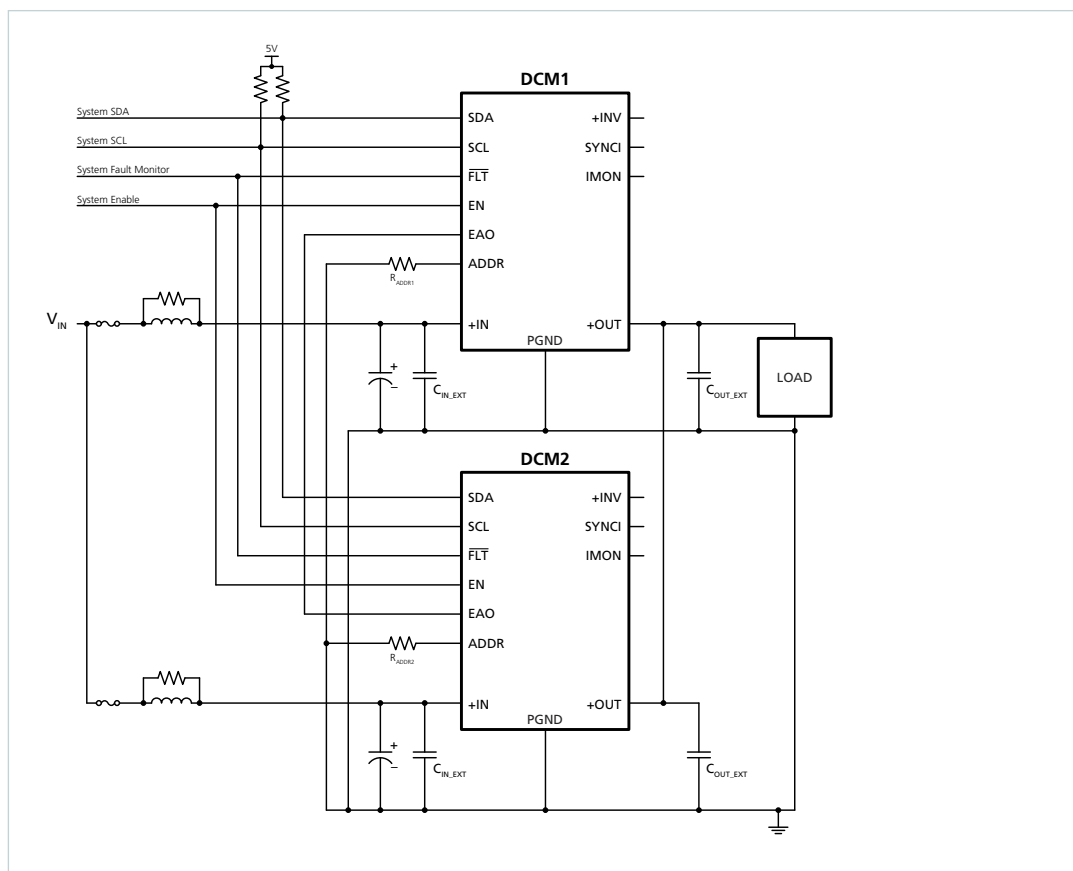
When load requirements exceed the rated current or power of a single DCM, the load can be powered by an array of DCMs with a maximum array size (N_{ARRAY}) as defined in the product datasheet. This application note focuses on the operation of the DCM when used in an array configuration.

Please note that this application note does not cover redundant arrays, fault tolerant arrays, phase shedding, independent enabling, independent fault management or interleaving.

Array Configuration

A properly configured parallel array of N_{ARRAY} DCMs provides the rated power or current of a single module times N_{ARRAY} , with no electrical de-rating required. Figure 2 demonstrates a typical application for an array of two DCMs. This arrangement can be extended for up to N_{ARRAY} DCMs in parallel.

Figure 2
Typical application of an
array of two DCMs



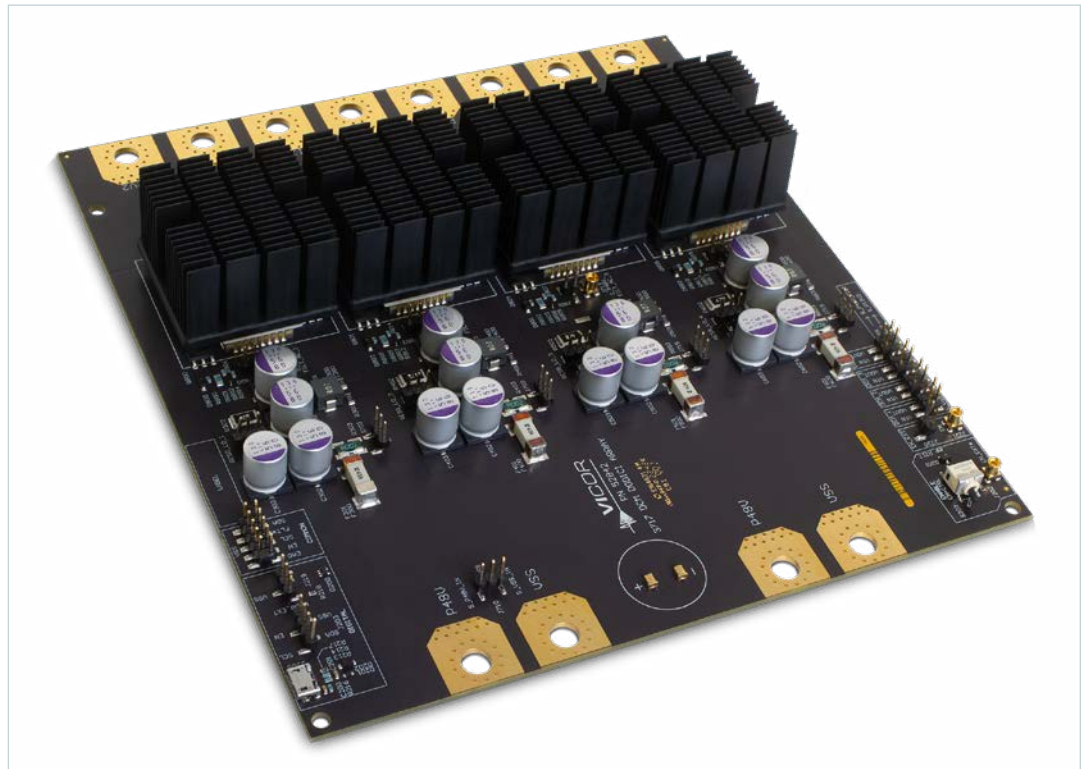
To properly configure a DCM™ array please adhere to the following guidelines:

1. Assign a unique PMBus® address to each DCM by choosing the appropriate resistor for each module's ADDR terminal as specified in the product datasheet.
2. Each of the following power and control terminals from each DCM **must be connected together** for proper array operation:
 - EN terminals to synchronize start up of the array and ensure that any one module does not momentarily take up a large share of the load. Independent EN signals are not recommended.
 - $\overline{\text{FLT}}$ terminals to synchronize start-up and for proper fault response. If one of the modules is in a fault condition, it will assert the $\overline{\text{FLT}}$ line alerting the other DCMs of the fault condition so that each DCM may take action to stop processing power. During start-up, the common $\overline{\text{FLT}}$ line will signal soft-start upon de-assertion of the line by the last DCM.
 - EAO terminal for output current sharing.
 - Use one PGND and connect to each DCM™ through a contiguous copper plane or multiple planes.

3. Any external multi-layer ceramic capacitors at the +IN and +OUT terminals for locally bypassing the high frequency noise currents, should be allocated per DCM™.
4. Each DCM must have a dedicated input fuse and filter.
5. Each DCM +OUT terminal must be directly connected, preferably through a solid copper plane.
6. Each DCM +IN terminal must have the same effective voltage.
7. Attention should be paid to the layout recommendations provided in the “Layout Guidelines” section.
8. The +INV, SYNCI, and IMON terminals **must not be connected** as part of the array.

Figure 3 shows an example of the DCM3717 used in an array configuration.

Figure 3
DCM3717 Dodici
4-up array PCB



System Behavior

For the following discussion, any terminal that is connected to the equivalent terminal for other modules in the array such as EN, $\overline{\text{FLT}}$, EAO, and +OUT will be referred to only by its terminal name. For the sake of simplicity, it is understood that the terminal name applies not to the individual terminal but to a common node shared by all the DCMs. When referring to the voltage, for example, nomenclature such as V_{OUT} for all +OUT terminals will be used. Additionally, V_{IN} refers to the voltage at each +IN terminal as if they were all driven together. In reality, each terminal has an input filter back to one common power supply.

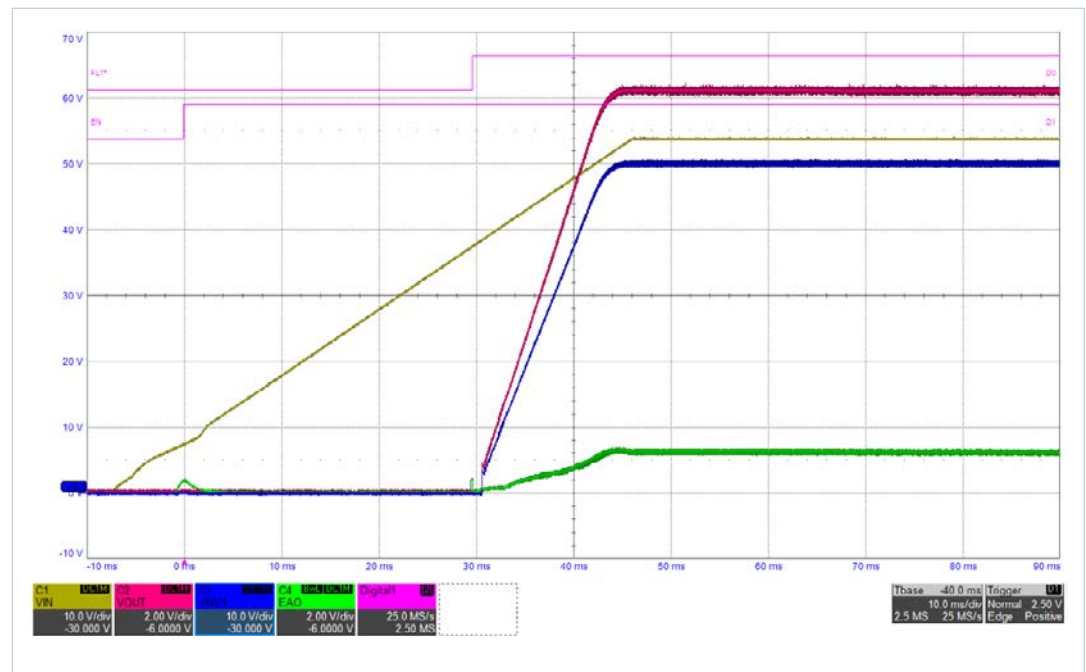
Start Up

- There are two methods for starting up the array:
 - EN floating** — V_{IN} is ramped past the V_{IN} UVLO rising threshold. The user must limit the slew rate of V_{IN} as specified in the product datasheet. Each DCM™ will pull up the voltage on its EN terminal with an internal current source and start up itself.
 - EN driven** — V_{IN} is ramped up past the UVLO rising threshold with the EN signal driven low. Once V_{IN} is at the desired voltage, EN is released and each DCM will start up itself.
- In general, a given DCM will attempt to start if the following conditions have been met:
 - The DCM has not been disabled via EN, or $\overline{\text{FLT}}$.
 - The DCM has recovered from any previous faults.
- Once EN is in a high state, each DCM's $\overline{\text{FLT}}$ will de-assert / pull up. The $\overline{\text{FLT}}$ signal has an open-drain output with an internal 10k Ω pull-up resistor to the DCMs internal regulator. When both of these conditions have been met and V_{IN} is above the V_{IN} UVLO rising threshold, the array enters soft start.

Soft Start

At start up when all $\overline{\text{FLT}}$ signals have de-asserted, the current-multiplier stage within each module begins switching. Each DCM's buck-boost stage is also enabled and their references rise to generate the soft-start ramp-up of the array's output voltage. The rise is monotonic once V_{OUT} exceeds roughly 1V, provided that the module has been disabled for at least $t_{\text{OFF_MONO}}$ as specified in the product data sheet. The error amplifiers within each module drive current into the common EAO node in response to the output voltage error, and the resulting EAO voltage causes the buck-boost stages to process power in response.

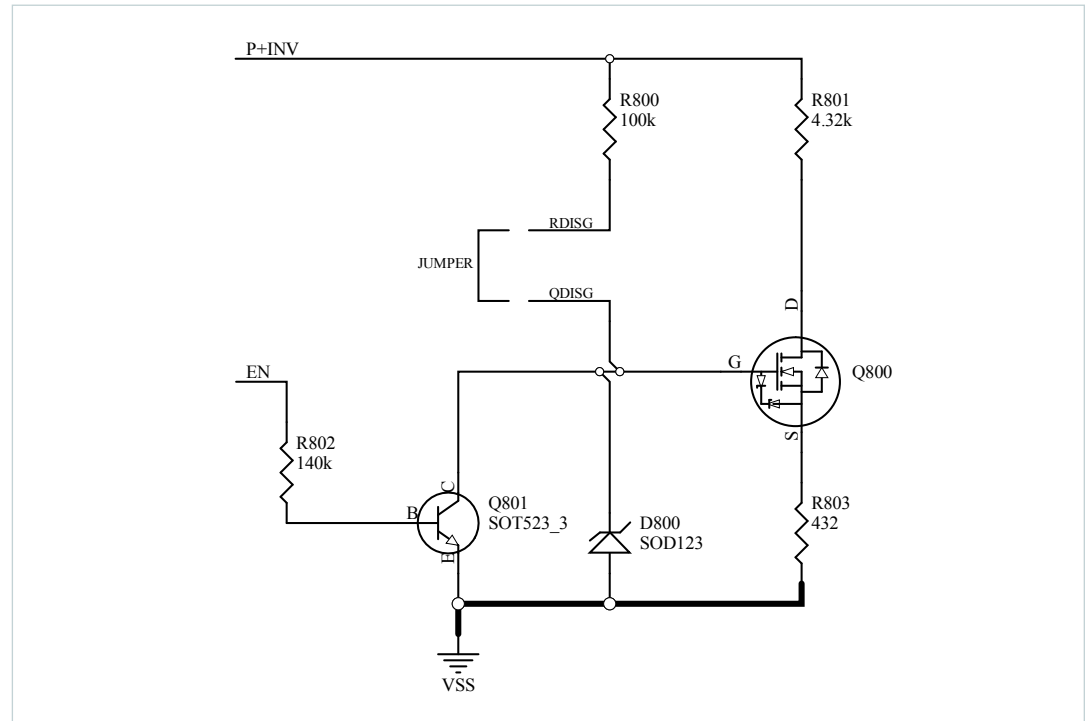
Figure 4
Example of DCM 4-up array
start up from V_{IN} into full load



+INV Discharge

For applications that require re-start $< t_{\text{OFF-MONO}}$, an optional discharge circuit can be used to discharge the +INV bus each time the EN pin is pulled low. Since the +INV terminal of each module in the array must not be connected to the others, a separate discharge circuit is required for each module. Figure 5 shows a schematic example that could be used for this purpose.

Figure 5
+INV discharge circuit



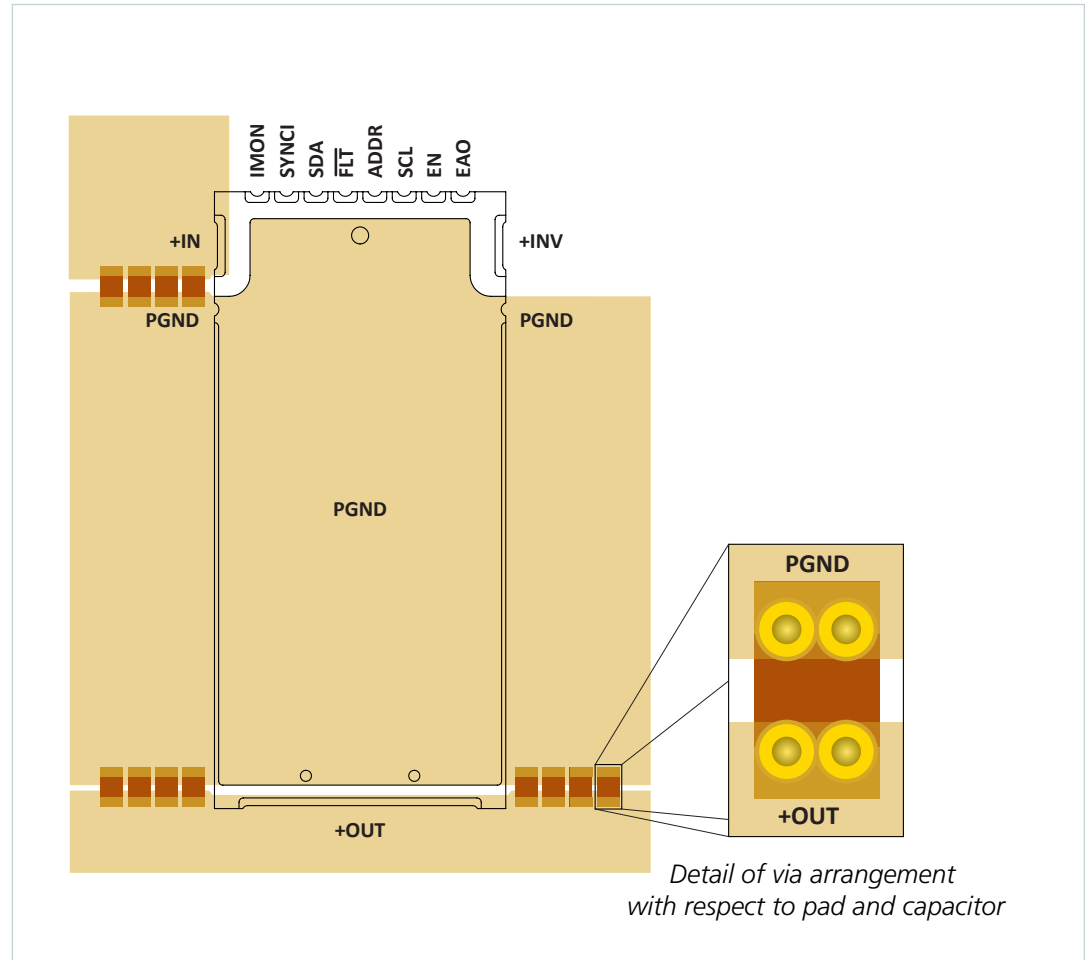
Start Up into a Pre-Charged Output

The array can turn on into a pre-charged output as described on the product specification with no additional considerations. Starting the array into a pre-charged output higher than the voltage specified in the product specification is not recommended due to the risk that the ring-up could trigger a $V_{\text{OUT-ovp}}$ fault. Each module output is capable of a full-rated continuous output current during soft start.

Layout Guidelines

Multi-layer ceramic capacitors are recommended at each DCM™ +IN and +OUT terminal as shown in Figure 6. This capacitance is needed to bypass the high-frequency ripple at its source. The amount of capacitance needed varies by design and should be distributed as shown in Figure 6.

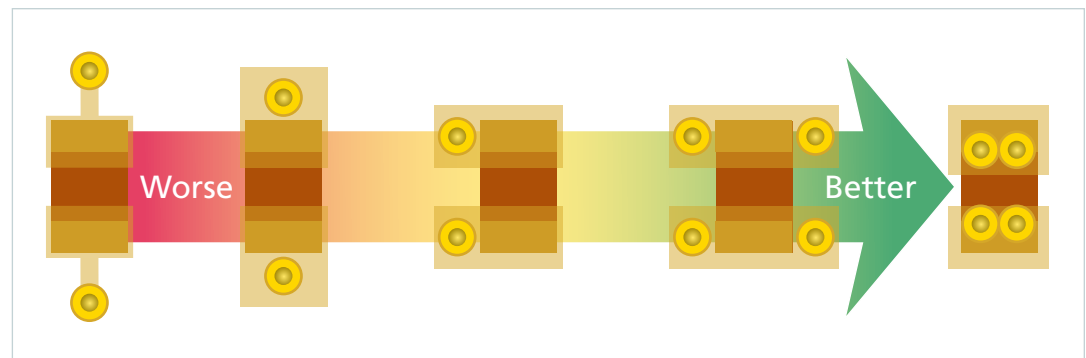
Figure 6
Recommended placement of
capacitance relative to +OUT
and PGND for DCM3717



The pours on each capacitor's terminal should be pulled in as far as spacing rules will allow in order to minimize inductance.

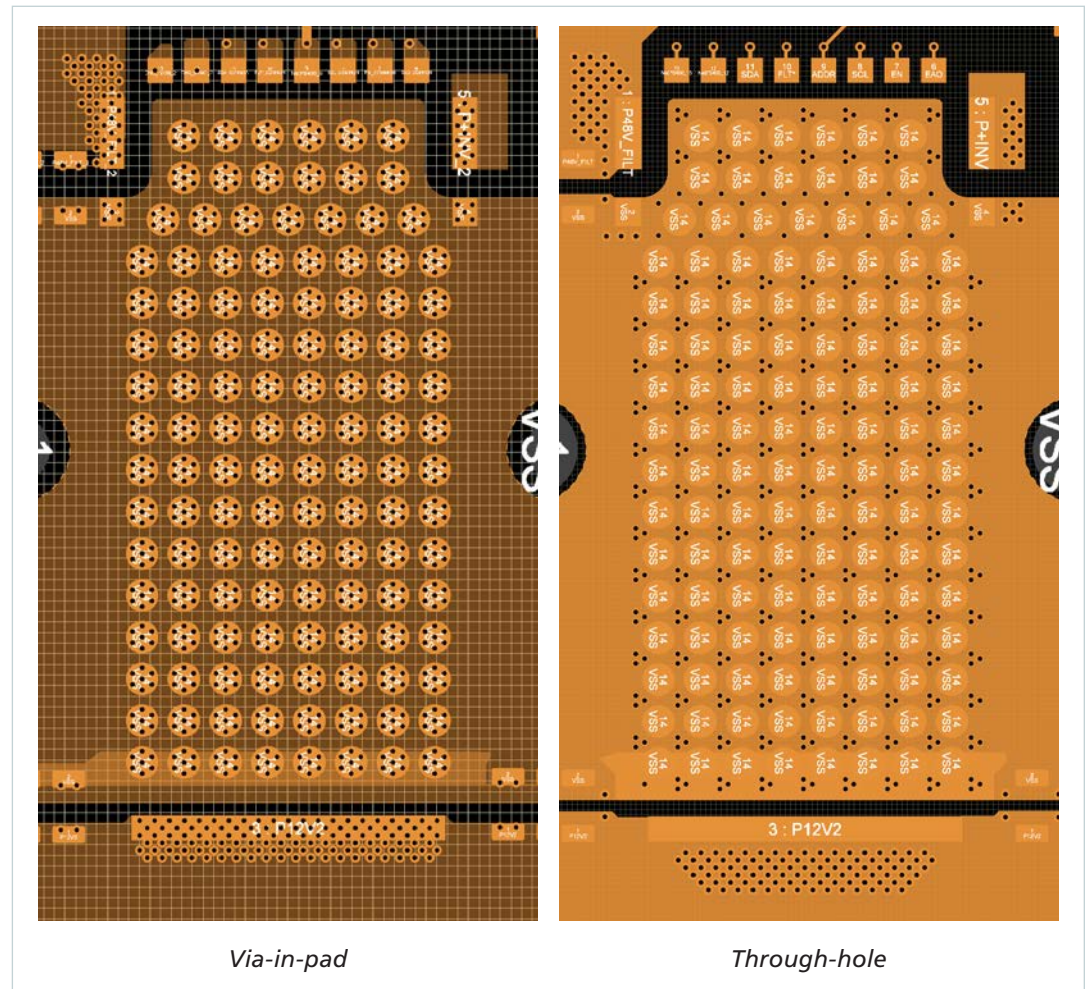
Vias should be placed near both terminals of each capacitor as close as possible to the center of each PCB pad. If possible, via-in-pad technology can be used so vias can be placed directly on the component pads. By adding additional vias in parallel for each capacitor, the performance of the capacitor can be further improved. This will produce the minimum loop-area and resulting parasitic inductance.

Figure 7
Examples of various via types
and placement patterns for
decoupling capacitors



A side-by-side comparison of DCM™ thru-hole with via-in-pad land patterns is shown in Figure 8 and demonstrates placement of vias for each type.

Figure 8
Example of DCM landing
pattern: via-in-pad and
through-hole



All DCM +OUT terminals must be connected and should also be on plane layers to minimize inductance and PCB losses between DCM outputs.

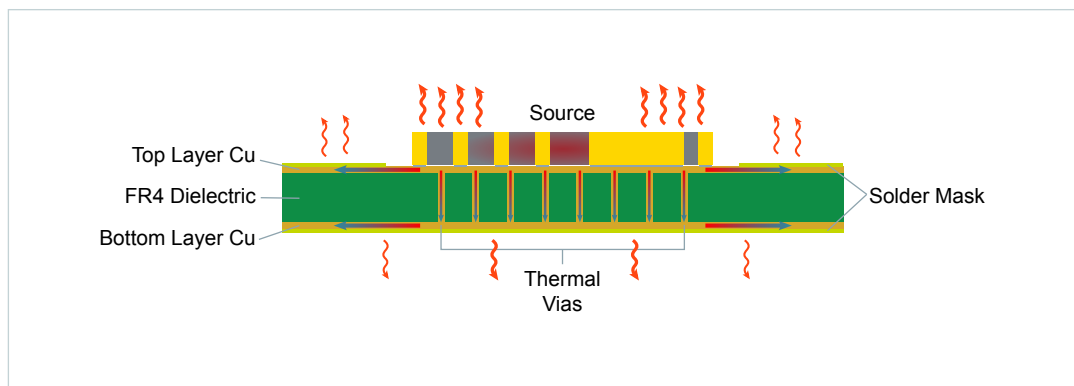
The DCM +IN terminals should not be directly connected; each should have its dedicated fuse and input filter as shown in Figure 2.

The fuse and filter of each DCM in the array must be powered from the same voltage source. Arrays with different input voltages are not permitted. For more details, refer to the “Load Sharing” section, Figure 14.

For a detailed view of the DCM landing pattern and layout, please refer to the product datasheet.

Reserve area under DCM for PGND plane and thermal vias to conduct heat away from the DCM and to other layers. Especially the opposite side of the PCB. Please see Figure 9.

Figure 9
Thermal via usage



With power connections (planes) located on the top layer, layer 2 should be dedicated to PGND. This minimizes the loop area (and inductance) from the DCM to the PoL, as well as from the source to the DCM™.

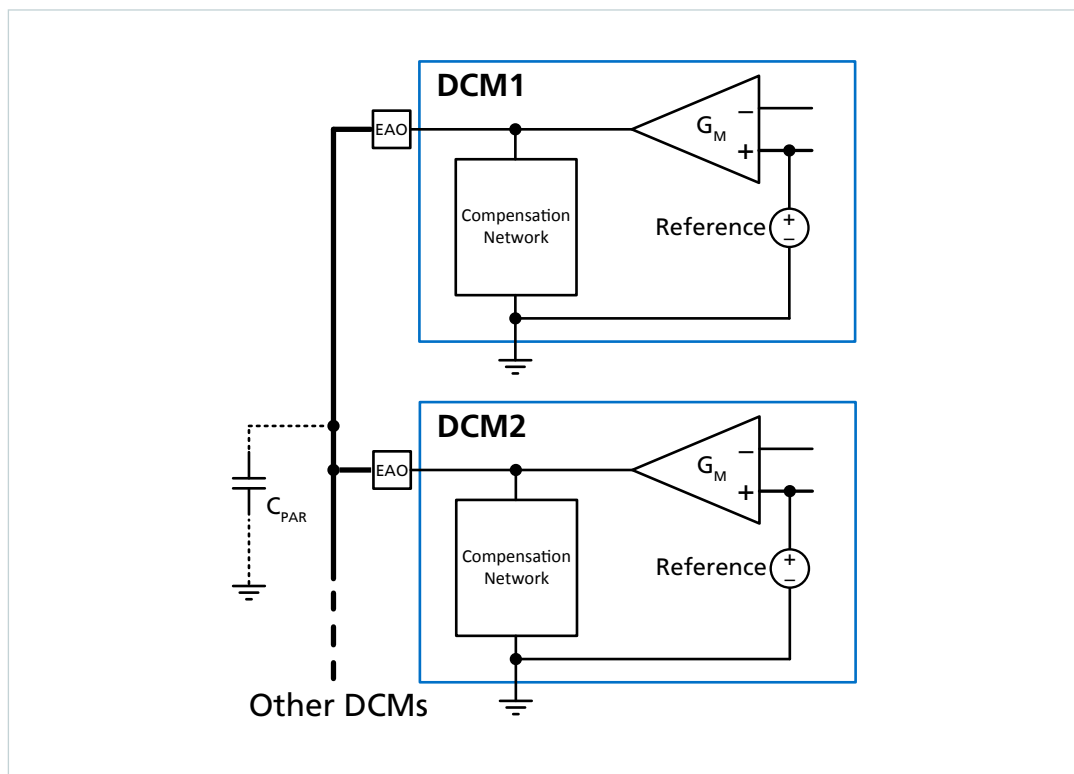
Route signals between ground planes to shield them from electric field coupling on adjacent layers; care should be taken to ensure signals are routed over continuous planes with no breaks.

Sensitive signals such as EAO should be routed away from the PMBus® signals (SDA, SCL) or any other traces that have high dV/dt which could couple switching noise onto the EAO signal and disturb the control loops.

Avoid routing EAO or any other DCM control signal under the DCM modules. DCMs may have a closed magnetic field present directly above and below the package. Noise may be coupled into components that intercept this field which cannot be shielded by ground planes.

EAO is the output of the control loop error amplifier which drives the compensation network. With that in mind, parasitic capacitance (C_{PAR}) on the EAO lines should be minimized as much as possible to not affect the location of the poles and zeros of the compensation network which can potentially affect the phase margin of the control loop. Keep the EAO traces as short as possible and keep the trace width to a minimum.

Figure 10
Example of EAO sharing



The examples in Figures 11 – 13 show the effect that C_{PAR} can have on the internal compensation network's pole (f_p) and zero (f_z) for $0 < C_{PAR} < 50\text{pF}$. Results are displayed for an array of $N = 2$ and $N = 4$. These simulation results are for illustrative purposes.

Figure 11
Effect of C_{PAR} on
internal compensation network
pole f_p , for array of $N = 2, 4$

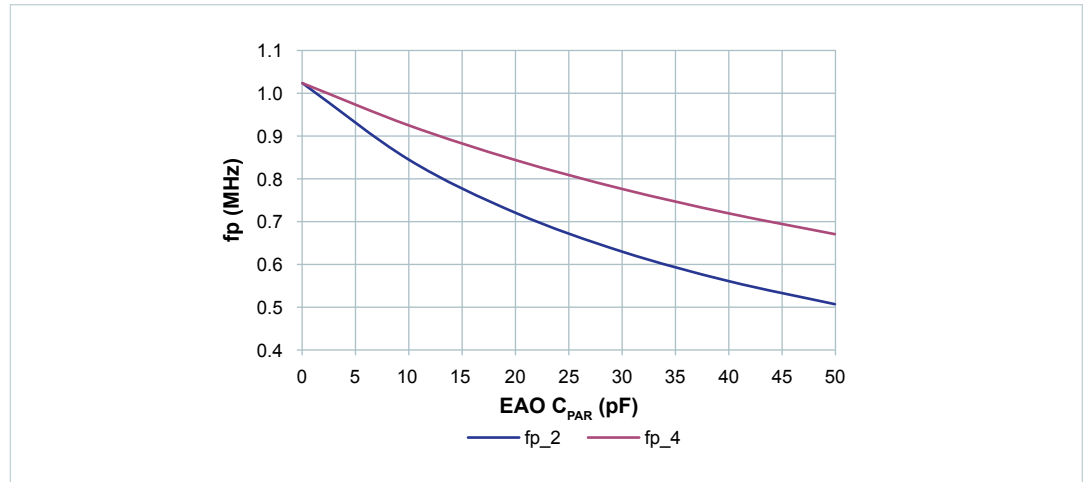


Figure 12
Effect of C_{PAR} on
internal compensation network
zero f_z , for array of $N = 2, 4$

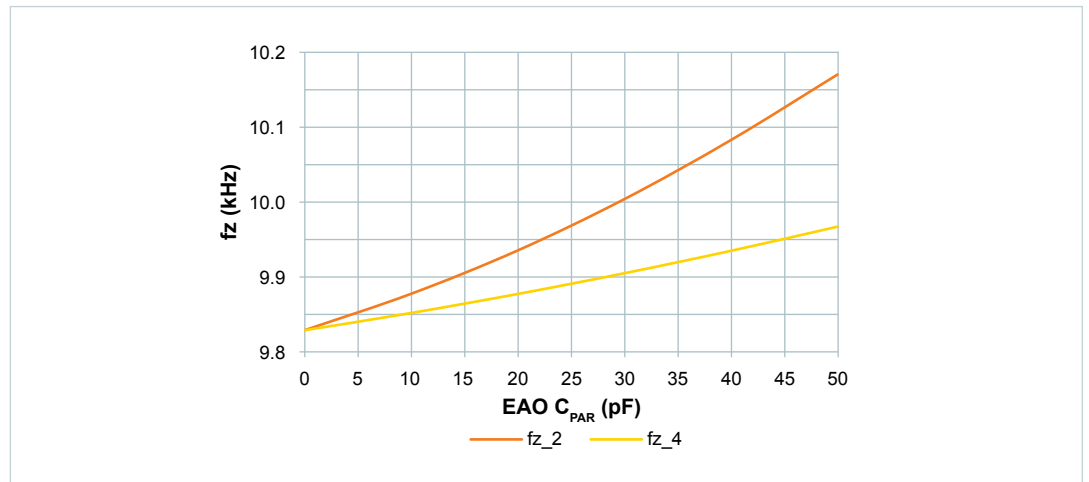
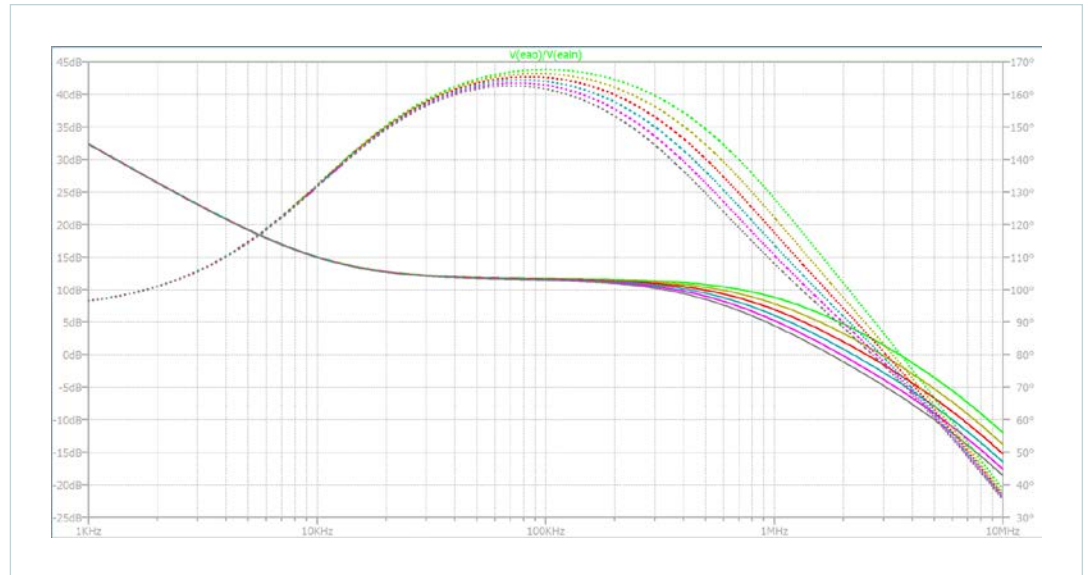


Figure 13
Effect of C_{PAR} on
internal compensation
network response



PGND should be carried on contiguous plane layers to optimize the effectiveness of high frequency bypassing, filtering, and to optimize the EAO connection between each DCM™ for good load sharing and minimized ripple. Note that PGND is the reference for each DCM receiving EAO, and is the reference for the compensation components.

Maximize copper pours on power nets: +IN, +OUT, and PGND.

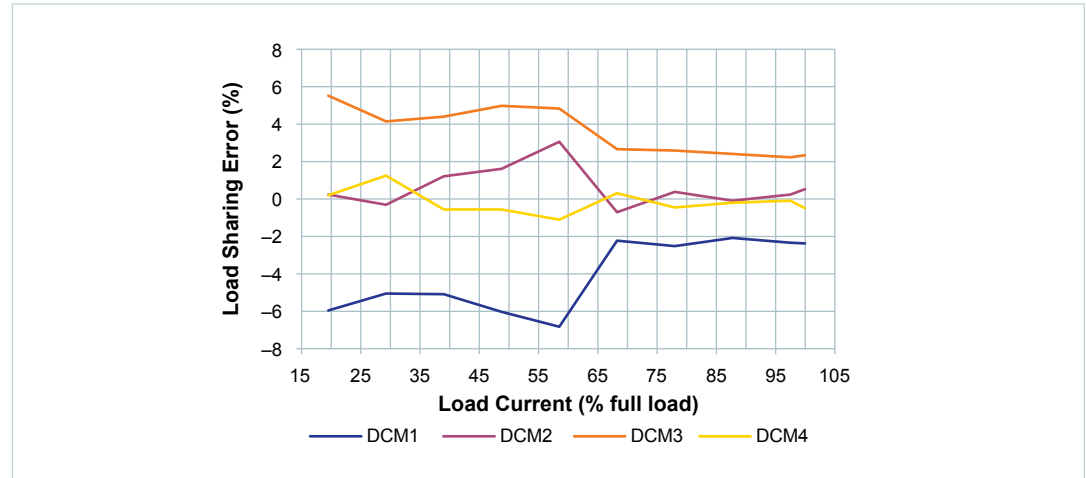
For best array performance utilize symmetry with respect to +IN and +OUT. Specifically, match / replicate the local layout around each DCM for all other DCMs in the array. Use the same input filter / fuse layout and copper pours for each DCM input path. Use the same ceramic input and output bypass cap placement for each DCM in the array.

The DCMs should be placed in close proximity so that interconnected control signals can be short, which improves stray capacitance and minimizes pickup of noise. However, there are also thermal considerations regarding spacing of the modules. Please refer to the "Thermal Considerations" section for more information.

Current Sharing

To increase the load capability beyond a single module, the outputs of multiple DCMs can be connected in parallel. For a given V_{IN} and output set-point (V_{OUT_SET}), V_{EAO} determines the output power and current delivered to the load. To achieve the best possible current sharing between the modules in the array, the EAO terminals of all modules must be tied together. Figure 14 shows an example of DCM3717S60E13G5TN1 sharing data taken on the 52842 4-up array PCB that was shown in Figure 3. Since the internal voltage loop of the DCM™ is closed at the +OUT terminal, the current measurement shunts are placed on the input side of the DCM in order to minimize the resistance to the load.

Figure 14
Example of
DCM3717S60E13G5TN1 load
sharing at nominal line and V_{OUT}

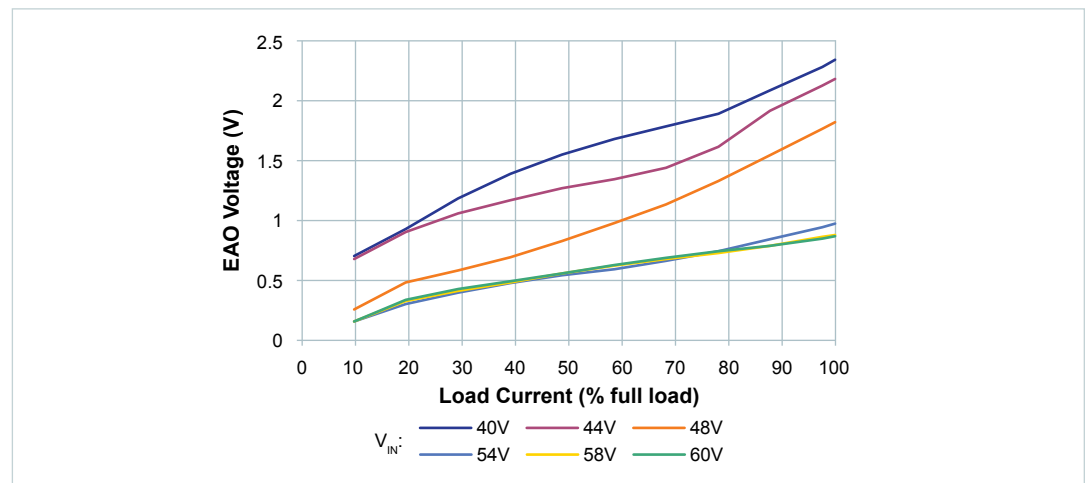


Tying all EAO terminals together ensures that the load sharing error will be minimized so that one DCM does not supply the large share of the load. This is an important point since the DCM supplying the large share of the load would run hotter and be subjected to higher stress than the others in the array. If the error is large enough, the DCM(s) carrying the large share of the load might exceed the maximum output current rating or possibly trip the overcurrent protection. It is also necessary to minimize voltage shifts from a DCM's local PGND to others in the array as this would amount to a different local V_{EAO} from module to module.

As mentioned previously, the EAO terminal is the output of the DCM's error amplifier and the control node for the buck-boost regulation stage. The common EAO configuration then becomes a current "summing junction" where the outputs of all the error amplifiers source or sink their instantaneous error currents and produce a "net" voltage for the control loops of the DCMs in the array.

Figure 15 illustrates the typical behavior of V_{EAO} vs. I_{OUT} for various V_{IN} at nominal V_{OUT} set point for the 750W DCM.

Figure 15
Example of DCM output current
vs. EAO voltage for
various temperatures

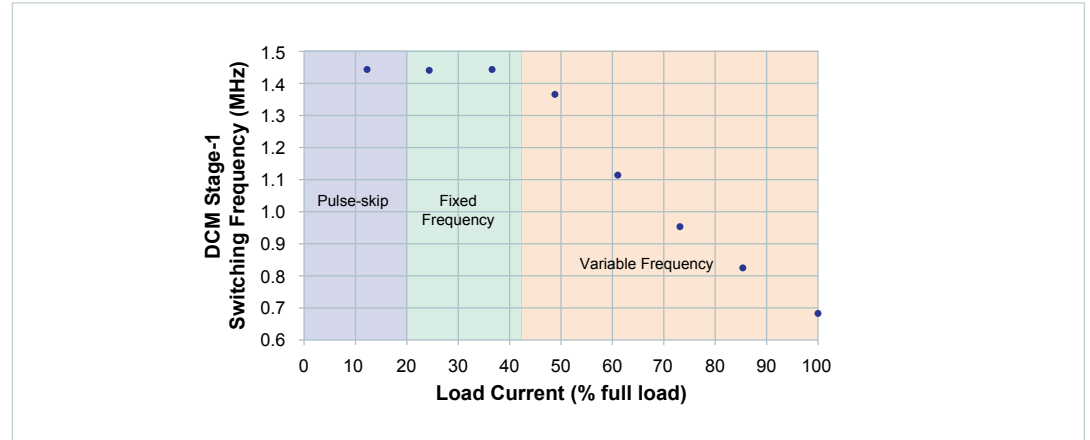


The family of curves in Figure 15 show a strong dependency on V_{IN} . It should be clear from this data that all modules must run at the same "effective" input voltage at +IN in order to obtain optimal sharing. Given that each module must have its own input filter, the voltages at the +IN terminal may not be identical so it is important to minimize this error and follow the layout suggestions regarding symmetry in the Layout Guidelines section.

Output Ripple

In a DCM, there are three time-domain modes of operation for the ZVS buck-boost stage, which depend on the load: fixed-frequency operation, variable-frequency operation, and pulse-skip mode (PSM). Figure 16 shows an example of the approximate region of each mode with respect to the load current at nominal line and output conditions. In fixed-frequency operation, the ZVS buck-boost switching frequency is running at its maximum. This maximum frequency is trimmed at the factory and results in comparable switching frequencies for each DCM™ in the array. However, as the load increases such that the DCMs enter variable-frequency operation, the differences between each DCM's switching frequency potentially increases and beats become more prevalent.

Figure 16
ZVS buck-boost stage
switching frequency vs. I_{LOAD}



Figures 17 and 18 show the formation of beats at 100% load for a 4-up array of DCM3717S60D13K0TN1 vs. the 50% load case.

Figure 17
 V_{OUT} ripple for 4-up array
 $V_{IN} = 40V$, $V_{OUT} = 12.2V$
 $I_{LOAD} = 50\%$

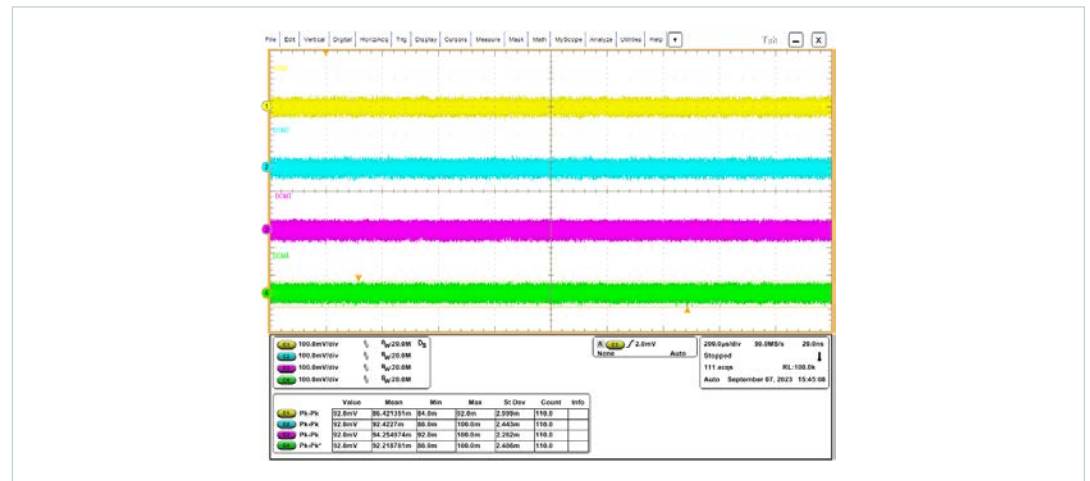
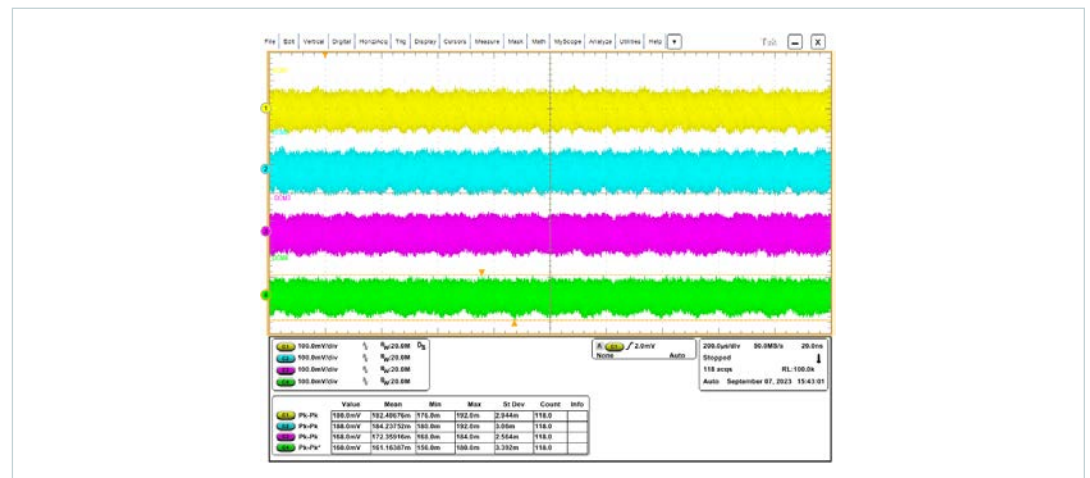


Figure 18
 V_{OUT} ripple for 4-up array
 $V_{IN} = 40V$, $V_{OUT} = 12.2V$
 $I_{LOAD} = 100\%$

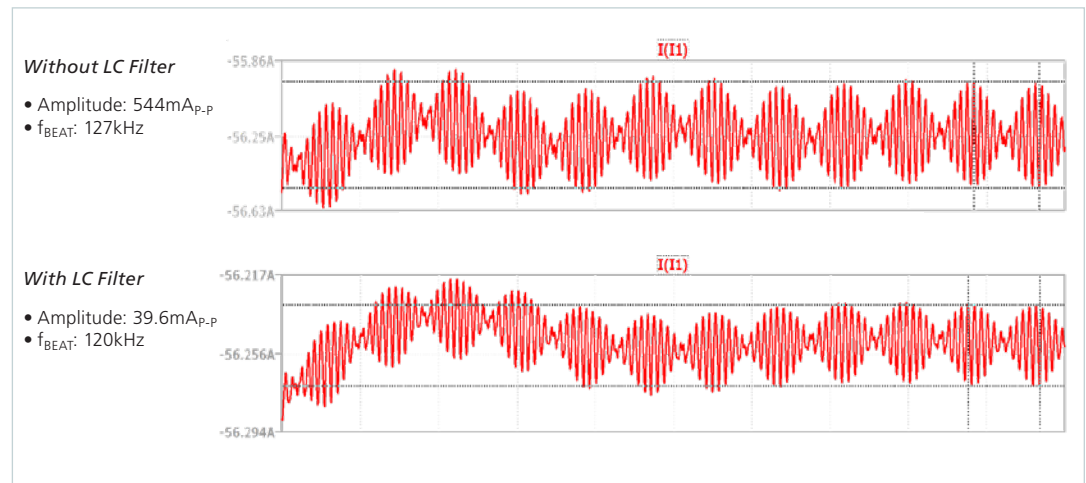


Input Ripple

On the input side of the array, each input LC filter serves to isolate the DCMs and minimize interaction of their input switching currents. The following example shows simulations to illustrate the effect of having an LC filter in an array with two DCMs verses no LC filter. The amplitude of the beats is 39.6mA_{p-p} with filters vs. 544mA_{p-p} with no filters.

Figure 19

Simulation showing reduction of beats when using an input LC filter

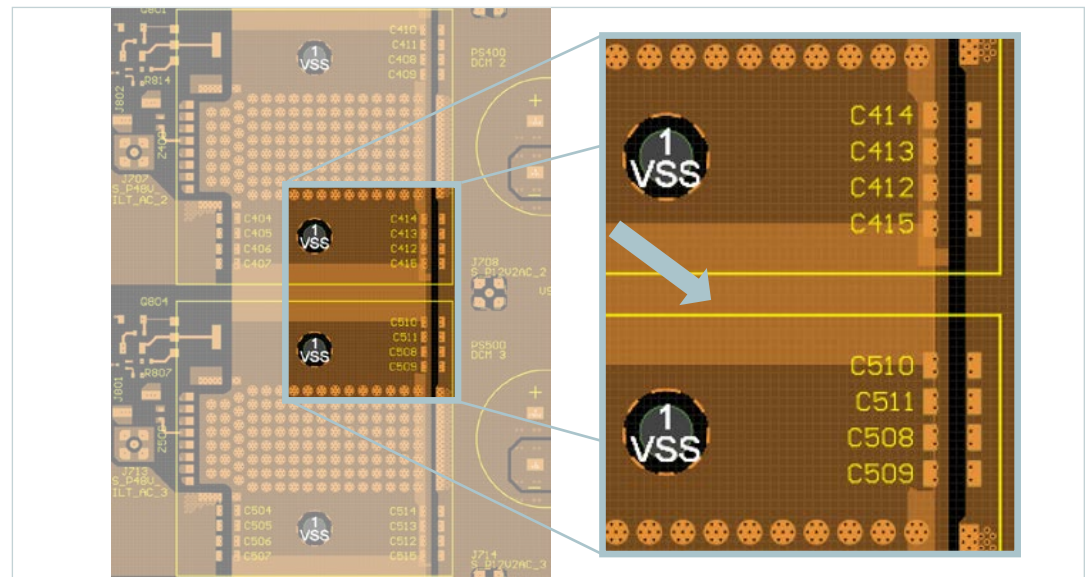


Thermal Considerations

In the "Layout Guidelines" section it was recommended that the DCMs should be placed in close proximity. While this is important for the electrical reasons previously discussed, the DCMs must still have sufficient separation to allow adequate cooling and prevent excessive internal temperatures. The physical separation of modules becomes even more important if the PCB is the dominant cooling path for heat to flow from the modules. Figure 20 shows an example of DCM™ spacing in an array.

Figure 20

Example of DCM spacing in an array



When using a heat sink as the cooling solution, it is recommended that an electrical insulator and gap compound be used. The insulator is necessary to prevent the grounded case top from bridging to the other terminals when the heat sink is installed. Figure 21 shows how the terminals on the SM-ChiP package are exposed on the top side of the package and without an insulator, could bridge to the case top.

Figure 21
SM-ChiP package

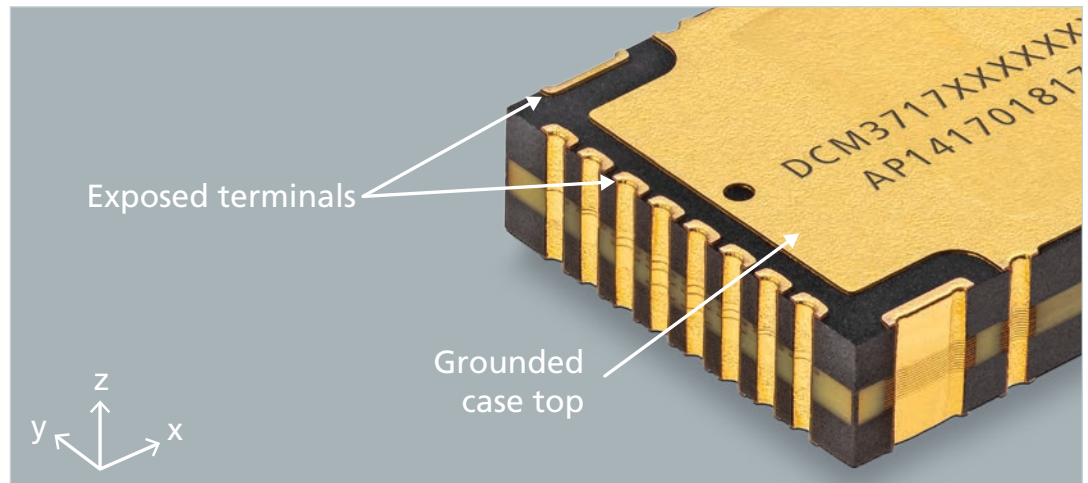
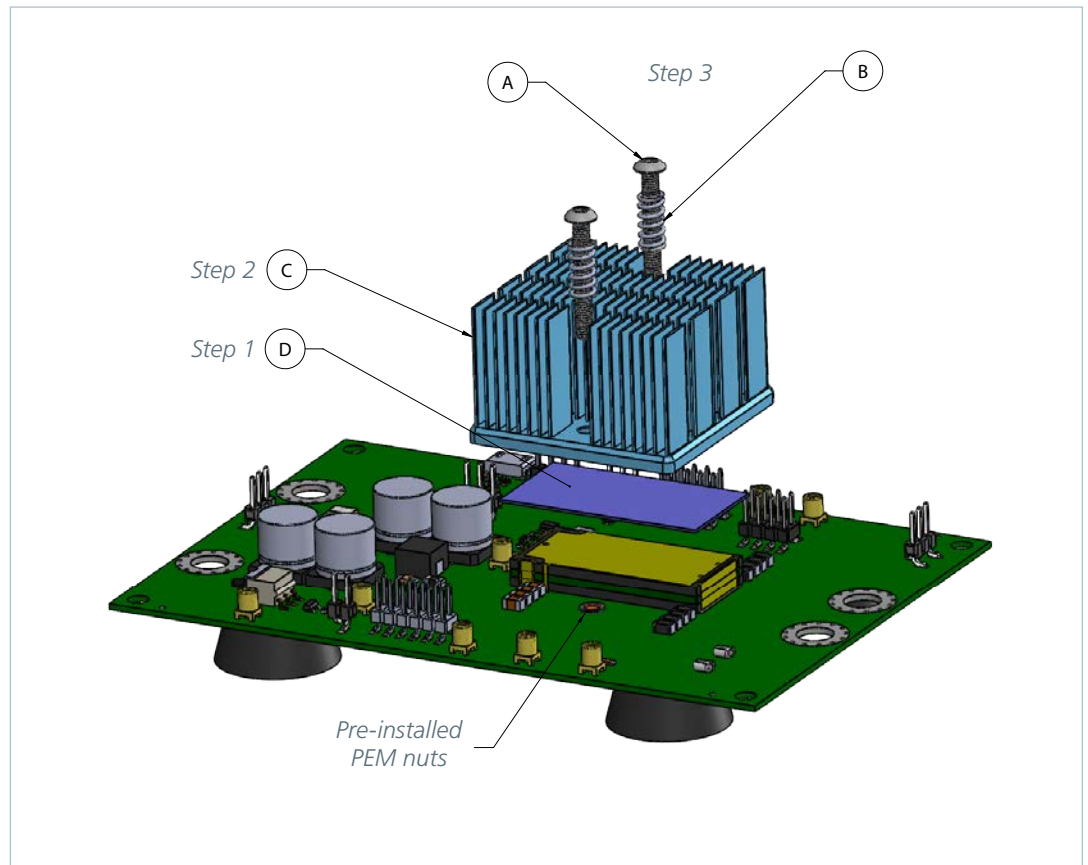


Figure 22
Example of heat sink
assembly with TIM on the
Singola evaluation PCB,
PIN DCM3717E60D13K0TN1



Input Filter Considerations

For a DC-DC converter, an input filter is recommended for EMI considerations. DCM input switching currents can generate ripple current noise which can propagate upstream to the power supply unit (PSU) and couple into sensitive circuitry running off the PSU. In addition, conducted EMI aggressors elsewhere in the system can pollute the input voltage and cause undesired behavior in the DCM.

In an array, there are good reasons for keeping the outputs in close proximity to each other. Since each DCM internally senses its output terminal voltage, it is important to minimize the impedance of the PDN, not only to the load but from one DCM to another. This, however, places a higher burden on the inputs of the DCMs since their proximity may increase the possibility of interaction between the DCMs. Such interactions may produce beat frequencies when DCMs run at slightly different frequencies. An example of this was presented in Figure 19. An input filter that uses both series and shunt attenuation is a good choice. An LC topology with some damping provides the shunt attenuation needed by way of the C to ground. The C with supplemental ceramic bypass caps helps keep AC currents circulating locally to the DCM's input. The series attenuation offered by the L helps to isolate the DCMs from each other. For these reasons, each DCM should have its dedicated input filter network.

Output Capacitance

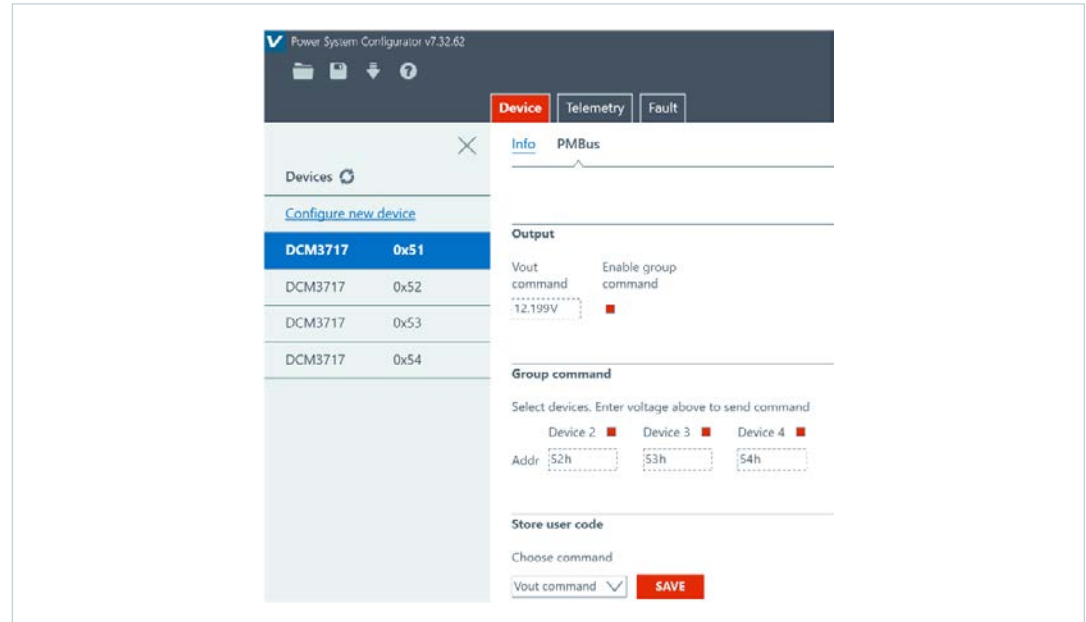
External ceramics placed locally to the +OUT terminal are recommended to help reduce output ripple due to internal switching of the module and allow the user more control to mitigate effects of the PDN. Additional output bulk capacitance as specified in the product datasheet can be added at the output as a means of energy storage for fast load transients.

PMBus® Interface

Vicor provides a user interface called Power System Configurator (PSC) for ease of PMBus® communication, for viewing telemetry and fault status of each DCM™ in the array. PSC provides a separate tab for each DCM in the array to:

1. Change the output voltage set-point V_{OUT_SET} for all DCMs in the array using the group command protocol.

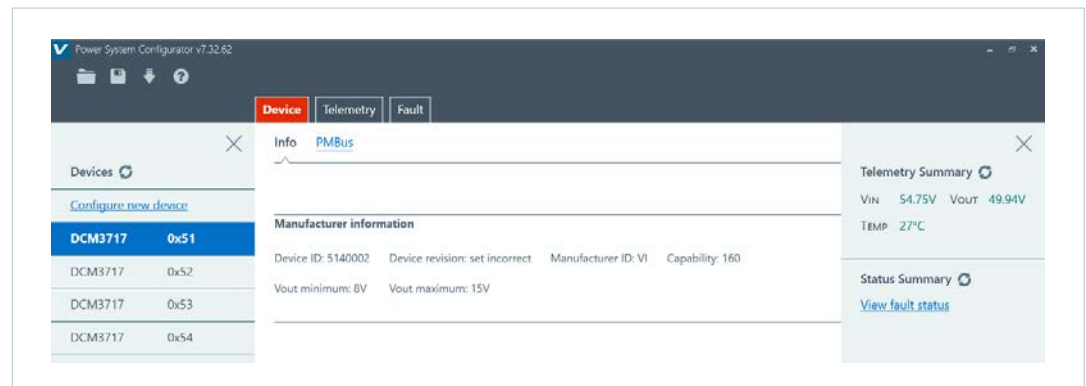
Figure 23
PSC V_{OUT_SET} programming



When programming the output voltage via PMBus using the VOUT_COMMAND (as described in the product specification), the PMBus group command protocol should be used. The group command protocol allows for a PMBus command to be sent to multiple units in succession but halts execution by each module until the last command has been sent. This will cause all of the DCMs in the array to wait until the last VOUT_COMMAND has been sent before collectively updating their output voltage setting. Not using the group command protocol can lead to nuisance detection of $\%_{EAIN_HI}$ faults for units that are programmed lower than the others in the array.

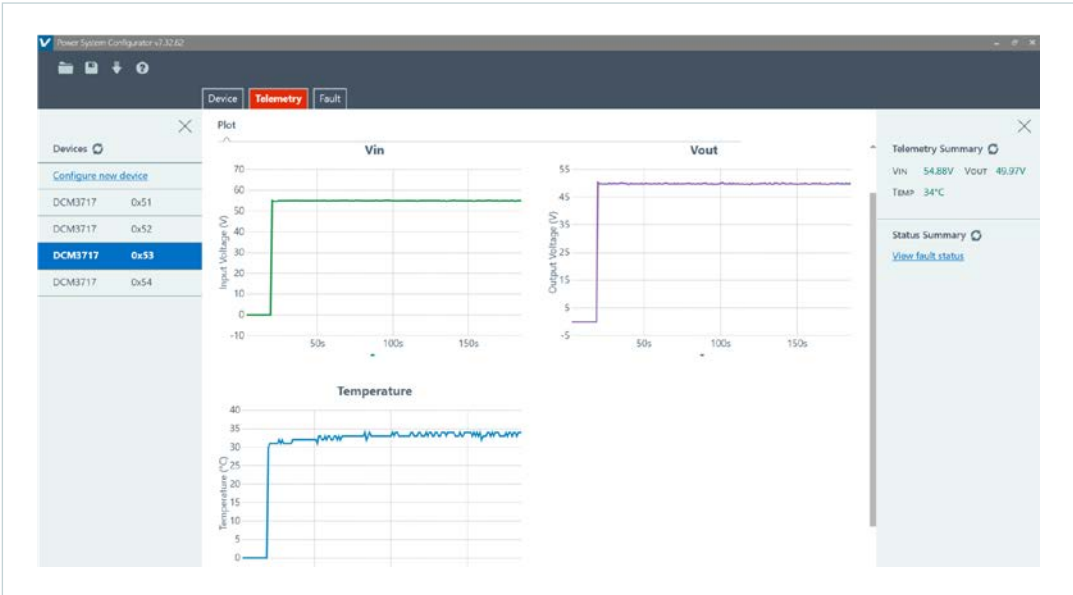
2. Display device information.

Figure 24
PSC device information tab



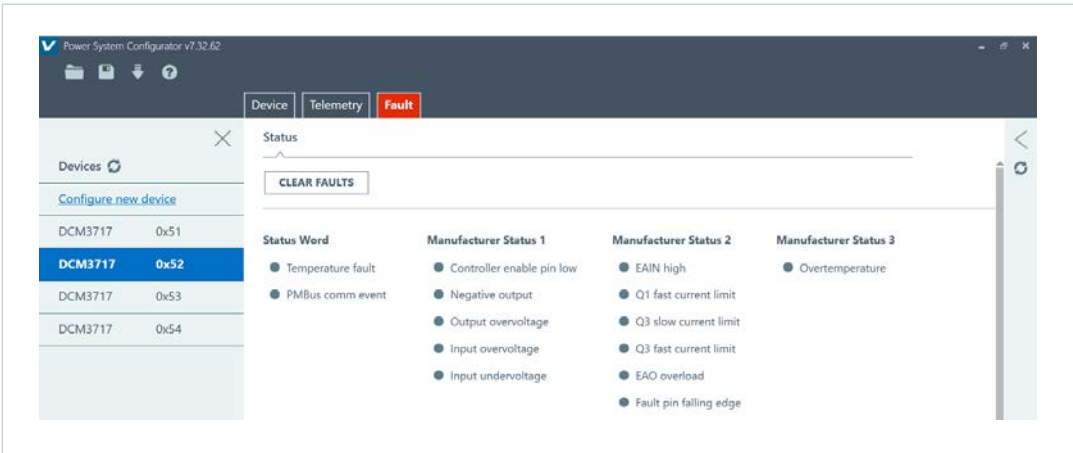
3. Display telemetry readout of V_{IN} , V_{+INV} (V_{OUT}), and buck-boost internal controller temperature.

Figure 25
PSC telemetry tab



4. Display the status of all faults.

Figure 26
PSC fault tab



Visit [Vicor Tools](#) for more information on the Vicor [Power System Configurator](#) and to download the installer.

Conclusion

In an array of DCMs, there is the benefit of increased power beyond that of a single module with no electrical de-rating. By following good layout practices, paying attention to the I/O signals that must be tied together, and implementing proper fusing and filtering the user can take full advantage of this benefit.

Appendix: DCM™ Product Information

Device	P _{OUT} Max (W)	Input Voltage (V _{DC})			Output Voltage (V _{DC})			K
		Min	Typ	Max	Min	Typ	Max	
DCM3717S60E13G5TN1	750	40	54	60	10	12.2	12.5	1/4
DCM3717S60D13K0TN1	1000							
DCM3735S60D13L0TN1	2000							

Revision History

Revision	Date	Description	Page Number(s)
1.0	07/10/25	Initial release	n/a

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