The Autoranging Rectifier Module (ARM) provides an effective solution for the AC front end of a power supply designed with Vicor DC-DC converters. This high-performance power system building block satisfies a broad spectrum of requirements and agency standards.

The ARM contains all of the power switching and control circuitry necessary for autoranging rectification, inrush current limiting, and overvoltage protection. This module also provides converter enable and status functions for orderly power up / down control or sequencing. To complete the AC front-end configuration, the user needs only to add hold-up capacitors and a suitable input filter with transient protection.

Functional Description (Figure 7.1)

Initial Conditions: The switch that bypasses the inrush limiting Positive Temperature Coefficient (PTC) thermistor is open when power is applied, as is the switch that engages the strap for voltage doubling. In addition, the downstream DC-DC modules are disabled via the Enable (EN) line, and Bus OK (BOK) is high.

Power-Up Sequence (Figure 7.2)

1.1 Upon application of input power, the output bus capacitors begin to charge. The thermistor limits the wcharge current, and the exponential time constant is determined by the hold-up capacitor value and the thermistor cold resistance. The slope (dV/dt) of the capacitor voltage approaches zero as the capacitors become charged to the peak of the AC line voltage.

2.1 If the bus voltage is less than 200V as the slope nears zero, the voltage doubler is activated, and the bus voltage climbs exponentially to twice the peak line voltage. If the bus voltage is greater than 200V, the doubler is not activated.

3.1 If the bus voltage is greater than 235V as the slope approaches zero, the inrush limiting thermistor is bypassed. Below 235V, the thermistor is not bypassed.

4.1 The converters are enabled ~150ms after the thermistor bypass switch is closed.

5.1 Bus OK is asserted after an additional ~150ms delay to allow the converter outputs to settle within specification.

Power-Down Sequence (Figure 7.2)

When input power is turned off or fails, the following sequence occurs as the bus voltage decays:

1.2 Bus OK is de-asserted when the bus voltage falls below $205V_{DC}$ (typical).

2.2 The converters are disabled when the bus voltage falls below $200V_{DC}$. If power is reapplied after the converters are disabled, the entire power-up sequence is repeated. If a momentary power interruption occurs and power is re-established before the bus reaches the disable threshold, the power-up sequence is not repeated.

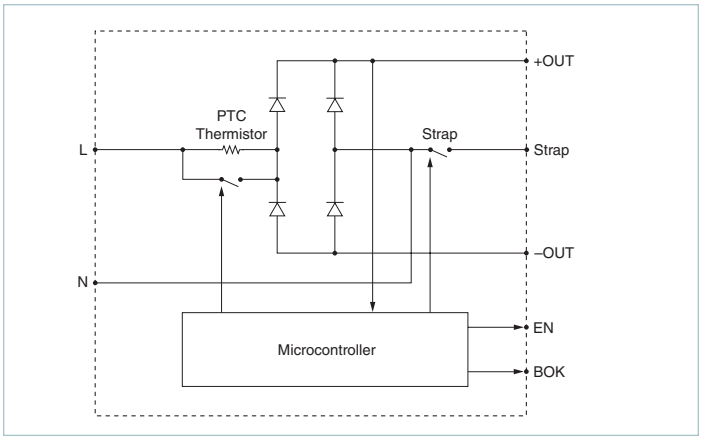


Figure 7.1 *— Functional block diagram*

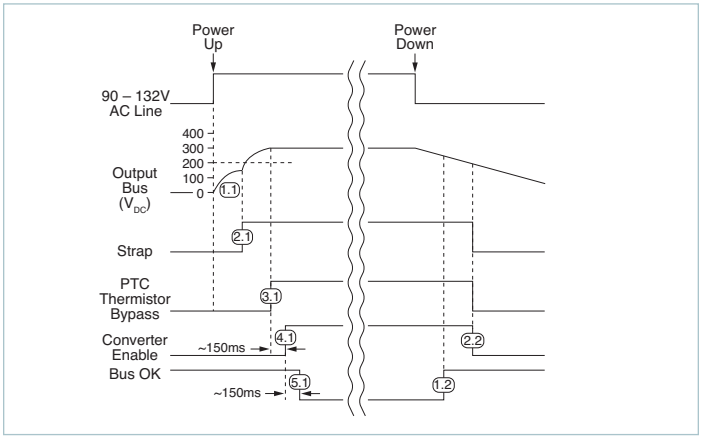


Figure 7.2 *— Timing diagram: power up / down sequence*

Off-Line Power Supply Configuration

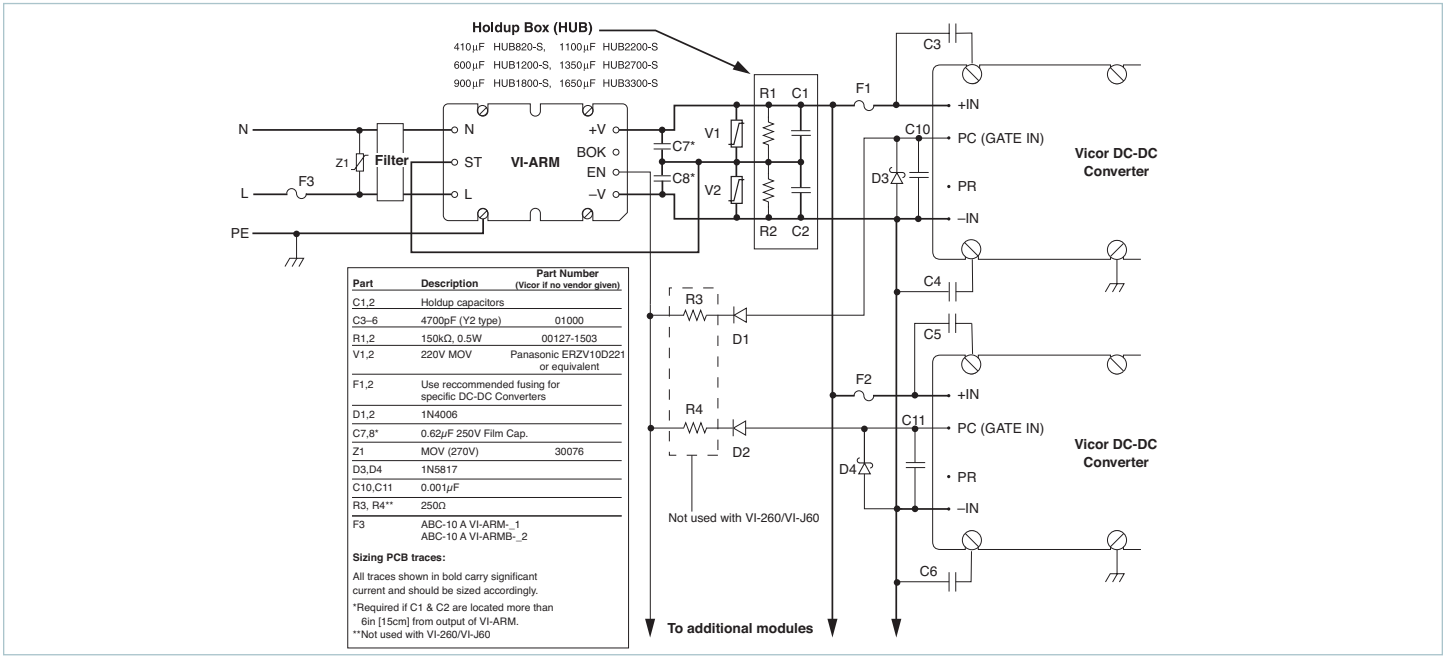
The ARM™ maintains the DC output bus voltage between 200 and 375V_{DC} over the entire universal input range, this being compatible with the Maxi, Mini, Micro 300V input converters as well as VI-260 family and VI-J60 family DC-DC converters. The ARM automatically switches to the proper rectification mode (doubled or undoubled) depending on the input voltage, eliminating the possibility of damage due to improper line connection. The VI-ARM-x1 is rated at 500W in the low range (90 –132V_{AC} input), and 750W in the high range (180 – 264V_{AC} input). The VI-ARMB–x2 is rated for 750 and 1,500W for the low and high input ranges respectively. Either of these modules can serve as the AC front end for any number and combination of compatible converters as long as the maximum power rating is not exceeded. See VI-ARMB derating curves (Figures 1 and 2) on VI-ARM data sheet.

Strap (ST) Pin: In addition to input and output power pin connections, it is necessary to connect the Strap pin to the junction of the series hold-up capacitors (C1, C2, Figure 7.3) for proper (autoranging) operation. Varistors across the capacitors provide input transient protection. The bleeder resistors (R1, R2, Figure 7.3) discharge the hold-up capacitors when power is switched off.

Enable (EN) Pin: (Figure 7.4) The Enable pin must be connected to the PC or GATE IN pin of all converter modules to disable the converters during power up. Otherwise, the converters would attempt to start while the hold-up capacitors were being charged through an un-bypassed thermistor, preventing the bus voltage from reaching the thermistor bypass threshold, thus disabling the power supply. The Enable output (the drain of a N-channel MOSFET) is internally pulled up to 15V through a 150kΩ resistor.

A signal diode should be placed close to and in series with the PC or GATE IN pin of each converter to eliminate the possibility of control interference between converters. The Enable pin switches to the high state (15V) with respect to the negative output power pin to turn on the converters after the power-up inrush is over. The Enable function also provides input overvoltage protection for the converters by turning off the converters if the DC bus voltage exceeds 400V_{DC}. The thermistor bypass switch opens if this condition occurs, placing the thermistor in series with the input voltage, which reduces the bus voltage to a safe level while limiting input current in case the varistors conduct. The thermistor bypass switch also opens if a fault or overload reduces the bus voltage to less than 180V_{DC}.

CAUTION: There is no input to output isolation in the ARM, hence the –OUT of the ARM and thus the –IN of the downstream DC-DC converter(s) are at a high potential. If it is necessary to provide an external enable / disable function by controlling the DC-DC converter's PC or GATE IN pin (referenced to the –IN) of the converter, an opto-isolator or isolated relay should be employed.



Part	Description	Part Number (Vicor if no vendor given)
C1,2	Holdup capacitors	
C3–6	4700pF (Y2 type)	01000
R1,2	150kΩ, 0.5W	00127-1503
V1,2	220V MOV	Panasonic ERZV10D221 or equivalent
F1,2	Use reccommended fusing for specific DC-DC Converters	
D1,2	1N4006	
C7,8*	0.62µF 250V Film Cap.	
Z1	MOV (270V)	30076
D3,D4	1N5817	
C10,C11	0.001µF	
R3, R4**	250Ω	
F3	ABC-10 A VI-ARM-_1 ABC-10 A VI-ARMB-_2	

Sizing PCB traces:

All traces shown in bold carry significant current and should be sized accordingly.

*Required if C1 & C2 are located more than 6in [15cm] from output of VI-ARM.

**Not used with VI-260/VI-J60

Figure 7.3 — *Typical ARM application*

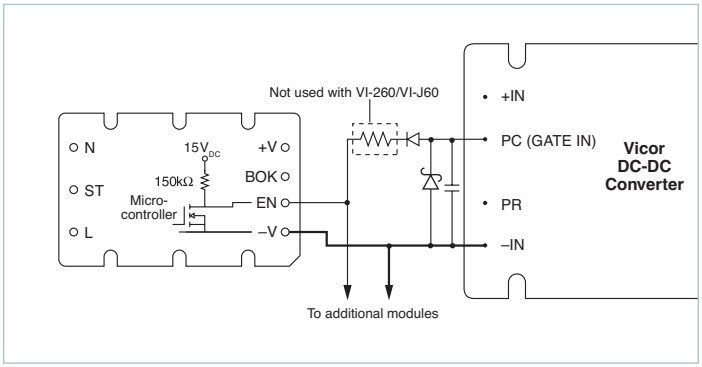


Figure 7.4 — *Enable (EN) function*

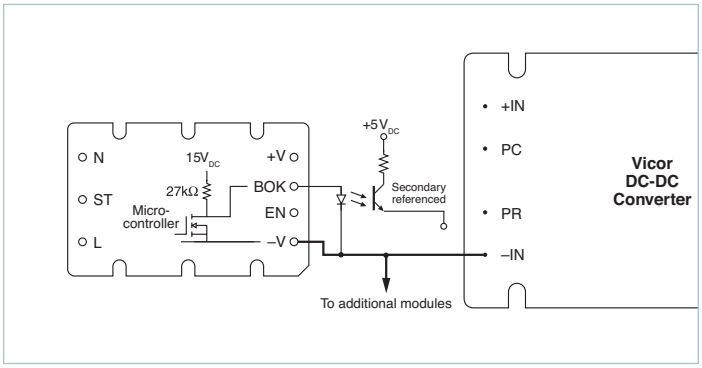
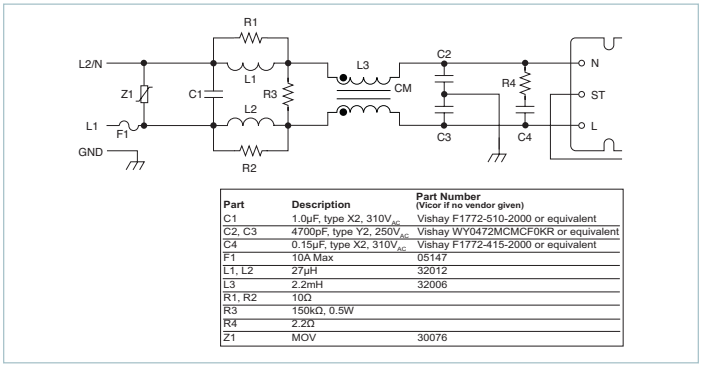
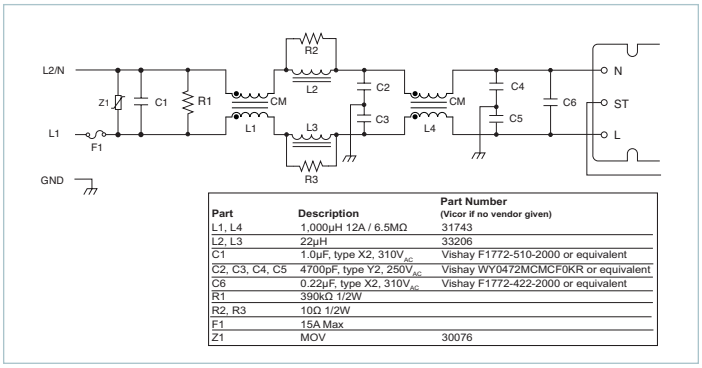


Figure 7.5 — *Bus OK (BOK) isolated power status indicator*



Part	Description	Part Number (Vicor if no vendor given)
C1	1.0µF, type X2, 310V$_{AC}$	Vishay F1772-510-2000 or equivalent
C2, C3	4700pF, type Y2, 250V$_{AC}$	Vishay WY0472MCMCF0KR or equivalent
C4	0.15µF, type X2, 310V$_{AC}$	Vishay F1772-415-2000 or equivalent
F1	10A Max	05147
L1, L2	27µH	32012
L3	2.2mH	32006
R1, R2	10Ω	
R3	150kΩ, 0.5W	
R4	2.2Ω	
Z1	MOV	30076

Figure 7.6a — *Recommended filter design; low-power filter connection for VI-ARM-x1*



Part	Description	Part Number (Vicor if no vendor given)
L1, L4	1,000µH 12A / 6.5MΩ	31743
L2, L3	22µH	33206
C1	1.0µF, type X2, 310V$_{AC}$	Vishay F1772-510-2000 or equivalent
C2, C3, C4, C5	4700pF, type Y2, 250V$_{AC}$	Vishay WY0472MCMCF0KR or equivalent
C6	0.22µF, type X2, 310V$_{AC}$	Vishay F1772-422-2000 or equivalent
R1	390kΩ 1/2W	
R2, R3	10Ω 1/2W	
F1	15A Max	
Z1	MOV	30076

Figure 7.6b — *Recommended filter design; high-power filter connection for VI-ARMB-x2*

Bus OK (BOK) Pin: (Figure 7.5) The Bus OK pin is intended to provide early-warning power fail information and is also referenced to the negative output pin.

CAUTION: There is no input-to-output isolation in the ARM. It is necessary to monitor Bus OK via an optocoupler if it is to be used on the secondary (output) side of the converters. A line-isolation transformer should be used when performing scope measurements. Scope probes should never be applied simultaneously to the input and output as this will damage the module.

Filter: Two input filter recommendations are shown for low-power VI-ARM-x1 and high-power VI-ARMB-x2. (Figures 7.6a and 7.6b)

Both filter configurations provide sufficient common-mode and differential-mode insertion loss in the frequency range between 100kHz and 30MHz to comply with the Class B conducted emissions limit.

Hold-up Capacitors: Hold-up capacitor values should be determined according to output bus voltage ripple, power-fail hold-up time, and ride-through time. (Figure 7.7) Many applications require the power supply to maintain output regulation during a momentary power failure of specified duration, i.e., the converters must hold up or ride through such an event while maintaining undisturbed output voltage regulation. Similarly, many of these same systems require notification of an impending power failure to allow time to perform an orderly shutdown.

The energy stored on a capacitor, which has been charged to voltage V, is:

$$\varepsilon = 1/2(CV^2) \qquad (1)$$

where: ε = stored energy
C = capacitance
V = voltage across the capacitor

Energy is given up by the capacitors as they are discharged by the converters. The energy expended (the power-time product) is:

$$\varepsilon = P\Delta t = C(V_1^2 - V_2^2)/2 \qquad (2)$$

where: P = operating power
Δt = discharge interval
V_1 = capacitor voltage at the beginning of Δt
V_2 = capacitor voltage at the end of Δt

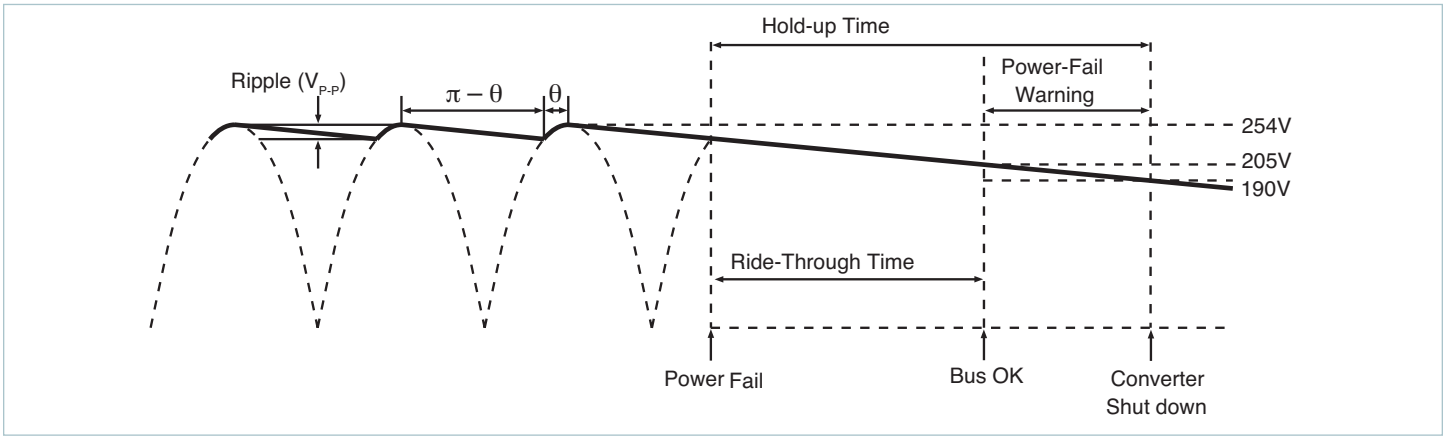


Figure 7.7 — *General timing diagram of bus voltage following interruption of the AC mains*

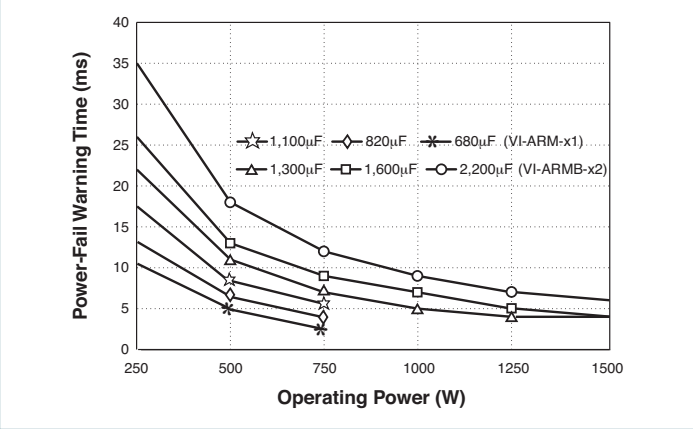


Figure 7.8 — *Power-fail warning time vs. operating power and total bus capacitance, series combination of C1, C2 (Figure 7.3)*

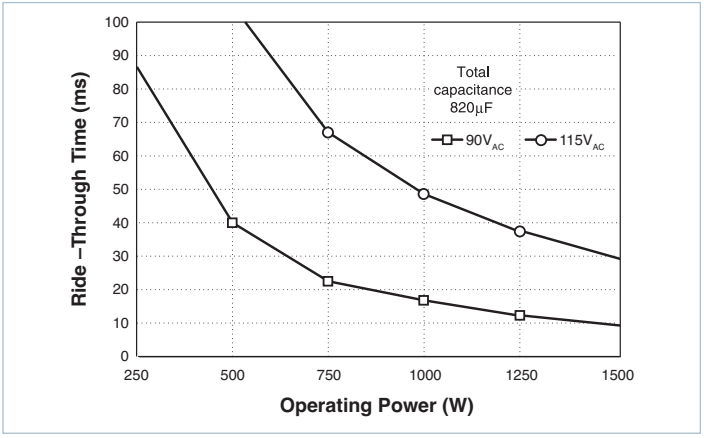


Figure 7.9 — *Ride-through time vs. operating power*

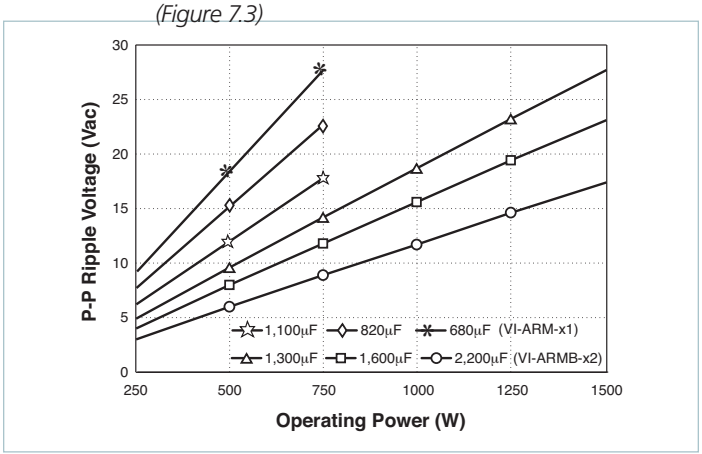


Figure 7.10 — *Ripple voltage vs. operating power and bus capacitance, series combination of C1, C2 (Figure 7.3)*

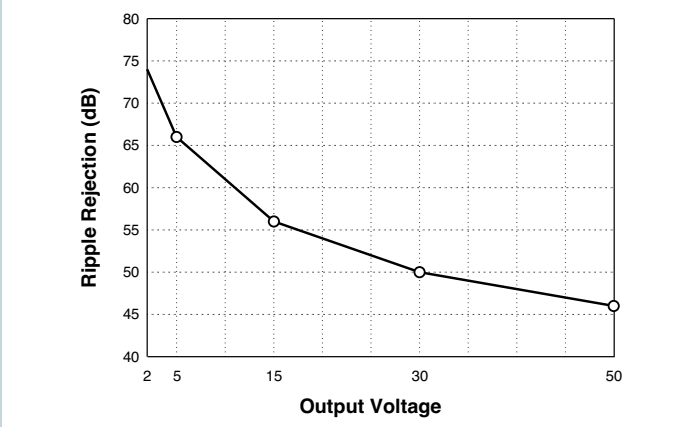


Figure 7.11 — *Converter ripple rejection vs. output voltage (typical)*

Rearranging equation 2 to solve for the required capacitance:

$$C = 2P\Delta t / (V_1^2 - V_2^2) \quad (3)$$

The power-fail warning time (Δt) is defined as the interval between (BOK) and converter shutdown (EN) as illustrated in Figure 7.7. The Bus OK and Enable thresholds are 205V and 190V, respectively. A simplified relationship between power fail warning time, operating power, and bus capacitance is obtained by inserting these constants:

$$C = 2P\Delta t / (205^2 - 190^2)$$

$$C = 2P\Delta t / (5{,}925)$$

It should be noted that the series combination (C1, C2, Figure 7.3) requires each capacitor to be twice the calculated value, but the required voltage rating is reduced to 200V.

Allowable ripple voltage on the bus (or ripple current in the capacitors) may define the capacitance requirement. Consideration should also be given to converter ripple rejection and resulting output ripple voltage.

For example, a converter whose output is 15V and nominal input is 300V will provide typically 56dB ripple rejection, i.e., $10V_{P-P}$ of input ripple will produce $15mV_{P-P}$ of output ripple. (Figure 7.11) Equation 3 is again used to determine the required capacitance. In this case, V_1 and V_2 are the instantaneous values of bus voltage at the peaks and valleys (Figure 7.7) of the ripple, respectively. The capacitors must hold up the bus voltage for the time interval (Δt) between peaks of the rectified line as given by:

$$\Delta t = (\pi - \theta) / 2\pi f \quad (4)$$

where: f = line frequency

θ = rectifier conduction angle

(Figure 7.7)

The approximate conduction angle is given by:

$$\theta = \cos^{-1} V_2 / V_1 \quad (5)$$

Another consideration in hold-up capacitor selection is their ripple current rating. The capacitors' rating must be higher than the maximum operating ripple current. The approximate operating ripple current (RMS) is given by:

$$I_{RMS} = 2P / V_{AC} \quad (6)$$

where: P = operating power level

V_{AC} = operating line voltage

Calculated values of bus capacitance for various hold-up time, ride-through time, and ripple voltage requirements are given as a function of operating power level in Figures 7.8, 7.9 and 7.10, respectively.

Example

In this example, the output required at the point of load is $12V_{DC}$ at 320W. Therefore, the output power from the ARM would be 375W (assuming a converter efficiency of 85%). The desired hold-up time is at least 9ms over an input range of 90 – $264V_{AC}$.

Determining Required Capacitance for Power-Fail Warning:. Figure 7.8 is used to determine capacitance for a given power fail warning time and power level, and shows that the total bus capacitance must be at least 820µF. Since two capacitors are configured in series, each capacitor must be at least 1,640µF.

Note: The warning time is not dependent on line voltage. A hold-up capacitor calculator is available on the Vicor website, at: https://asp.vicorpower.com/calculators/calculators.asp?calc=4

Determining Ride-through Time: Figure 7.9 illustrates ride-through time as a function of line voltage and output power and shows that at a nominal line of $115V_{AC}$, ride-through would be 68ms. Ride-through time is a function of line voltage.

Determining Ripple Voltage on the Hold-up Capacitors: Figure 7.10 is used to determine ripple voltage as a function of operating power and bus capacitance, and shows that the ripple voltage across the hold-up capacitors will be $12V_{AC}$.

Determining the Ripple on the Output of the DC-DC Converter: Figure 7.11 is used to determine the ripple rejection of the DC-DC converter and indicates a ripple rejection of approximately 60dB for a 12V output. If the ripple on the bus voltage is $12V_{AC}$ and the ripple rejection of the converter is 60dB, the output ripple of the converter due to ripple on its input (primarily 120Hz) will be $12mV_{P-P}$.