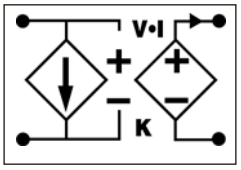
V·I CHIP
FACTORIZED POWER

V048F015T100
V048F015M100

RoHS

VTM™ Transformer

- 48 V to 1.5 V V•I Chip™ Converter
- 100.0 A (150.0 A for 1 ms)
- High density – 339 A/in³
- Small footprint – 80 A/in²
- Low weight – 0.5 oz (15 g)
- Pick & Place / SMD or Through hole
- 125°C operation (T_J)
- 1 µs transient response
- 3.5 million hours MTBF
- Typical efficiency 89%
- No output filtering required



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Vf = 26.0 - 55 V
V_{OUT} = 0.820 - 1.71 V
I_{OUT} = 100.0 A
K = 1/32
R_{OUT} = 1.1 mΩ max

Product Description

The V048F015T100 V•I Chip transformer excels at speed, density and efficiency to meet the demands of advanced power applications while providing isolation from input to output. It achieves a response time of less than 1 µs and delivers up to 100.0 A in a volume of less than 0.295 in³ with unprecedented efficiency. It may be paralleled to deliver higher power levels at an output voltage settable from 0.820 to 1.71 Vdc.

The VTM V048F015T100's nominal output voltage is 1.5 Vdc from a 48 Vdc input Factorized Bus, Vf, and is controllable from 0.820 to 1.71 Vdc at no load, and from 0.710 to 1.61 Vdc at full load, over a Vf input range of 26.0 to 55 Vdc. It can be operated either open- or closed-loop depending on the output regulation needs of the application. Operating open-loop, the output voltage tracks its Vf input voltage with a transformation ratio, K = 1/32, for applications requiring an isolated output voltage with high efficiency. Closing the loop back to an input PRM™ regulator or DC-DC converter enables tight load regulation.

The 1.5 V VTM achieves a current density of 339 A/in³ in a V•I Chip package compatible with standard pick-and-place and surface mount assembly processes. The VTM's fast dynamic response and low noise eliminate the need for bulk capacitance at the load, substantially increasing system density while improving reliability and decreasing cost.

Absolute Maximum Ratings

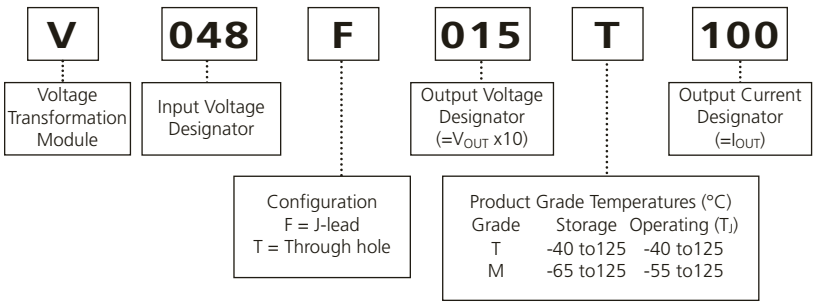
Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60	Vdc	
	100	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
VC to -In	-0.3 to 19.0	Vdc	
+Out to -Out	-0.5 to 4.0	Vdc	
Isolation voltage	2,250	Vdc	Input to output
Output current	100.0	A	Continuous
Peak output current	150.0	A	For 1 ms
Output power	161	W	Continuous
Peak output power	242	W	For 1 ms
Case temperature during reflow[a]	225	°C	MSL 5
	245	°C	MSL 6, TOB = 4 hrs
Operating junction temperature[b]	-40 to 125	°C	T-Grade
	-55 to 125	°C	M-Grade
Storage temperature	-40 to 125	°C	T-Grade
	-65 to 125	°C	M-Grade

Notes:

[a] 245°C reflow capability applies to product with manufacturing date code 1001 and greater.

[b] The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by a shutdown comparator.

Part Numbering



Electrical Specifications

Input Specs (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	26.0	48	55	Vdc	Max Vin = 53 V, operating from -55°C to -40°C
Input dV/dt			1	V/µs	
Input overvoltage turn-on	55.1			Vdc	
Input overvoltage turn-off			59.5	Vdc	
Input current			3.6	Adc	
Input reflected ripple current		124		mA p-p	Using test circuit in Figure 15; See Figure 1
No load power dissipation		5.6	7.8	W	
Internal input capacitance		4.0		µF	
Internal input inductance			5	nH	

Output Specs (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Output voltage	0.820		1.71	Vdc	No load
	0.710		1.61	Vdc	Full load
Rated DC current	0		100.0	Adc	26.0 - 55 V_{IN}
Peak repetitive current			150.0	A	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
Short circuit protection set point	125			Adc	Module will shut down
Current share accuracy		5	10	%	See Parallel Operation on Page 9
Efficiency					
Half load	88.8	89.3		%	See Figure 3
Full load	88.6	89.2		%	See Figure 3
Internal output inductance		1.6		nH	
Internal output capacitance		306		µF	Effective value
Output overvoltage setpoint	1.7			Vdc	Module will shut down
Output ripple voltage					
No external bypass		100	200	mVp-p	See Figures 2 and 5
94 µF bypass capacitor		14		mVp-p	See Figure 6
Effective switching frequency	2.8	2.9	3.0	MHz	Fixed, 1.4 MHz per phase
Line regulation					
K	0.0309	1/32	0.0316		$V_{OUT} = K \bullet V_{IN}$ at no load
Load regulation					
R_{OUT}		0.9	1.1	mΩ	See Figure 16
Transient response					
Voltage overshoot		60		mV	100.0 A load step with 100 µF C_{IN}; See Figures 7 and 8
Response time		200		ns	See Figures 7 and 8
Recovery time		1		µs	See Figures 7 and 8

Waveforms

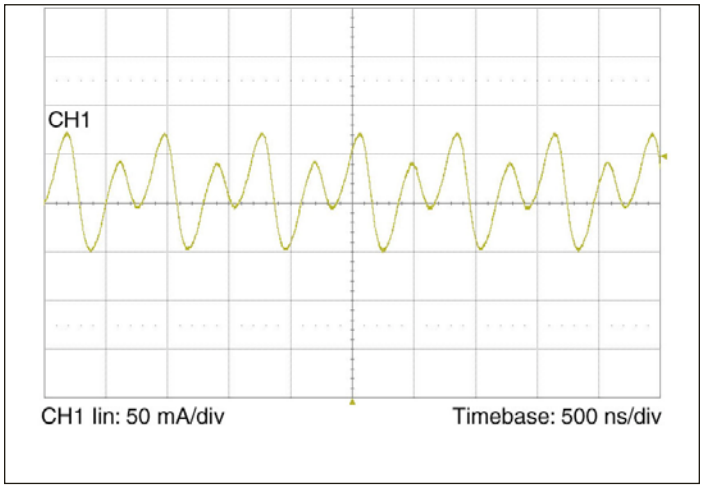


Figure 1 *— Input reflected ripple current at full load and 48 Vf.*

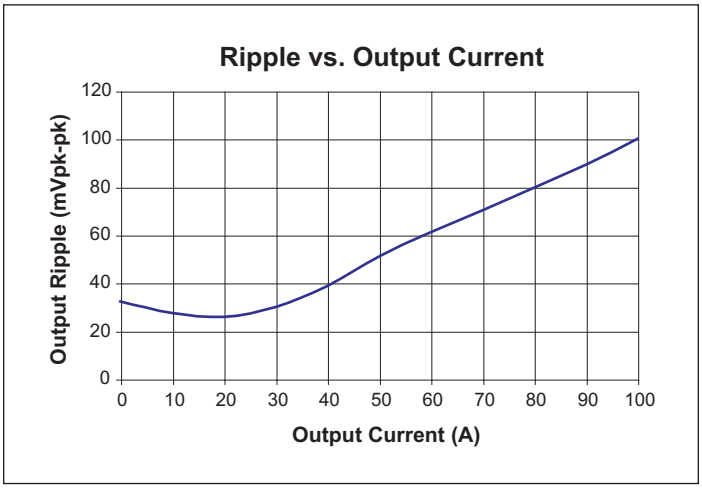


Figure 2 *— Output voltage ripple vs. output current at 48 Vf with no POL bypass capacitance.*

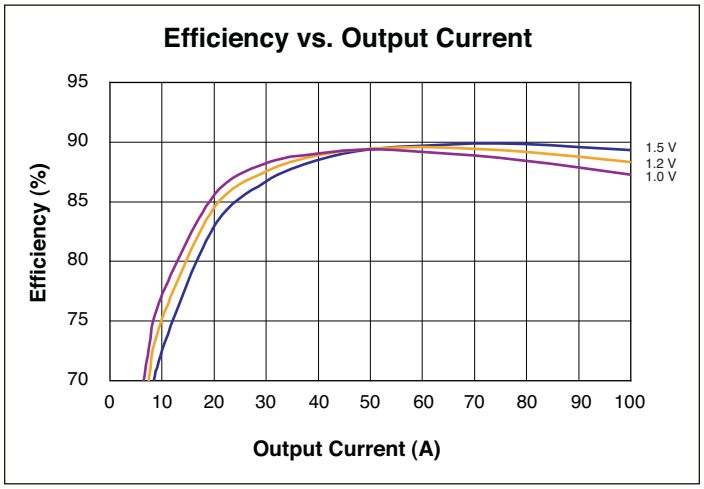


Figure 3 *— Efficiency vs. output current.*

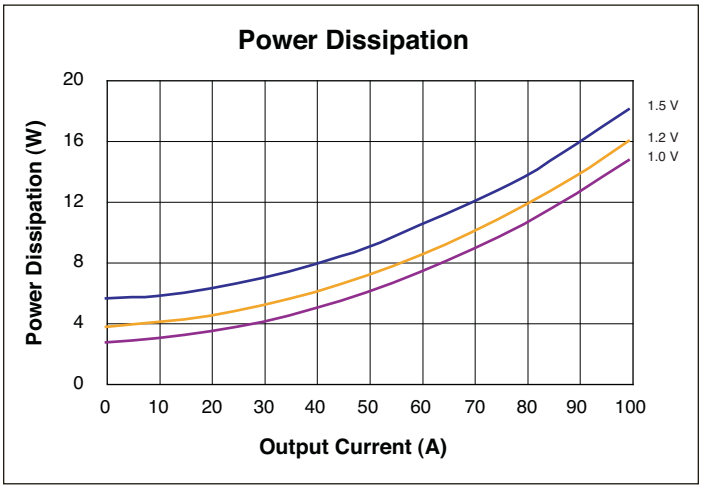


Figure 4 *— Power dissipation vs. output current.*

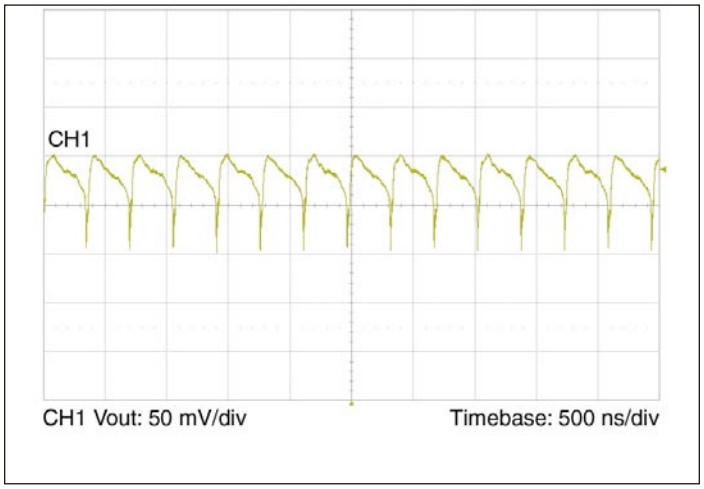


Figure 5 *— Output voltage ripple at full load and 48 Vf with no POL bypass capacitance.*

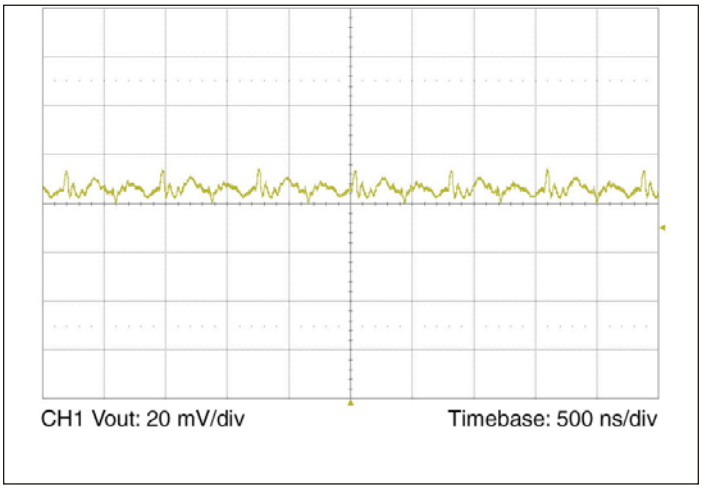


Figure 6 *— Output voltage ripple at full load and 48 Vf with 94 µF ceramic POL bypass capacitance and 20 nH distribution inductance.*

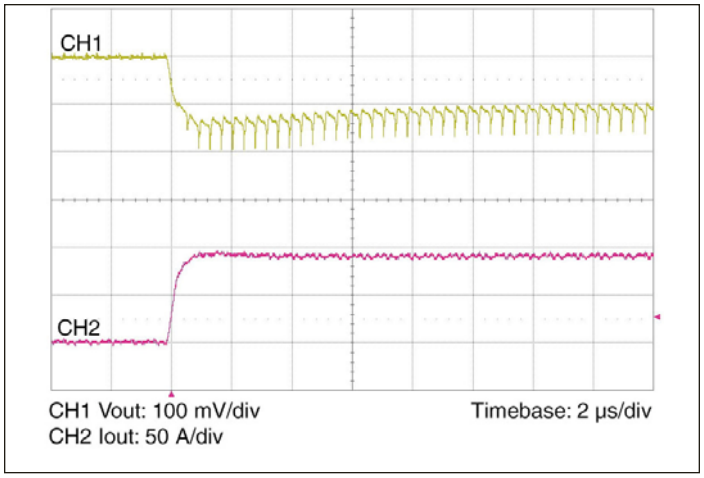


Figure 7 *— 0-100.0 A load step with 100 µF input capacitance and no output capacitance.*

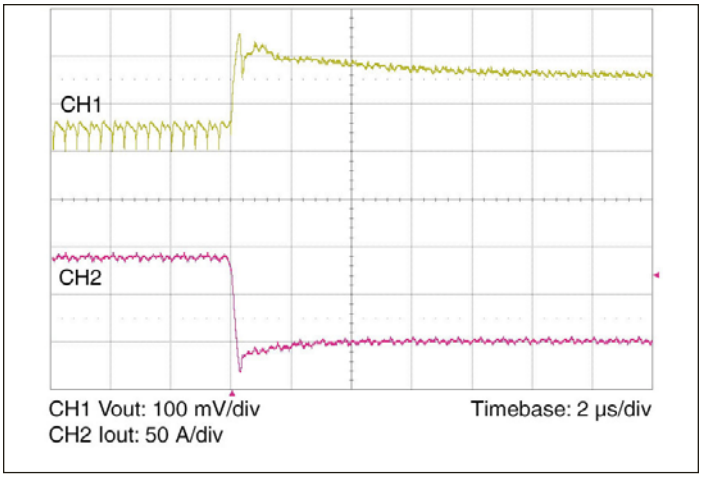


Figure 8 *— 100.0-0 A load step with 100 µF input capacitance and no output capacitance.*

General

Parameter	Min	Typ	Max	Unit	Note
MTBF					
MIL-HDBK-217F		3.5		Mhrs	25°C, GB
Isolation specifications					
Voltage	2,250			Vdc	Input to output
Capacitance		3,000		pF	Input to output
Resistance	10			MΩ	Input to output
Agency approvals		cTÜVus			UL/CSA 60950-1, EN 60950-1
		CE Mark			Low voltage directive
		RoHS			
Mechanical					See Mechanical Drawings, Figures 10 – 13
Weight		0.53/15		oz/g	
Dimensions					
Length		1.28/32,5		in/mm	
Width		0.87/22		in/mm	
Height		0.265/6,73		in/mm	
Peak compressive force applied to case (Z axis)		5	6	lbs.	Supported by J-leads only
Thermal					
Over temperature shutdown	125	130	135	°C	Junction temperature
Thermal capacity		9.3		Ws/°C	
Junction-to-case thermal impedance ($R_{\theta JC}$)		1.1		°C/W	See Thermal Considerations on Page 9
Junction-to-board thermal impedance ($R_{\theta JB}$)		2.1		°C/W	

Auxiliary Pins (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Primary Control (PC)					
DC voltage	4.8	5.0	5.2	Vdc	
Module disable voltage	2.4	2.5		Vdc	
Module enable voltage		2.5	2.6	Vdc	VC voltage must be applied when module is enabled using PC
Current limit	2.4	2.5	2.9	mA	Source only
Disable delay time		6		µs	PC low to Vout low
VTM Control (VC)					
External boost voltage	12	14	19	Vdc	Required for VTM start up without PRM
External boost duration		10		ms	Maximum duration of VC pulse = 20 ms

Pin / Control Functions

+In / -In DC Voltage Ports

The VTM input should be connected to the PRM output terminals. Given that both the PRM and VTM have high switching frequencies, it is often good practice to use a series inductor to limit high frequency currents between the PRM output and VTM input capacitors. The input voltage should not exceed the maximum specified. If the input voltage exceeds the overvoltage turn-off, the VTM will shutdown. The VTM does not have internal input reverse polarity protection. Adding a properly sized diode in series with the positive input or a fused reverse-shunt diode will provide reverse polarity protection.

TM – For Factory Use Only

VC – VTM Control

The VC port is multiplexed. It receives the initial V_{CC} voltage from an upstream PRM, synchronizing the output rise of the VTM with the output rise of the PRM. Additionally, the VC port provides feedback to the PRM to compensate for the VTM output resistance. In typical applications using VTMs powered from PRMs, the PRM's VC port should be connected to the VTM VC port.

The VC port is not intended to be used to supply V_{CC} voltage to the VTM for extended periods of time. If VC is being supplied from a source other than the PRM, the voltage should be removed after 20 ms.

PC – Primary Control

The Primary Control (PC) port is a multifunction port for controlling the VTM as follows:

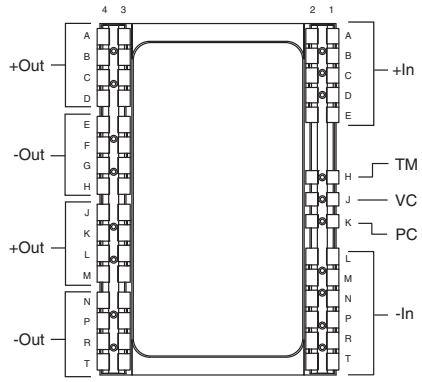
Disable – If PC is left floating, the VTM output is enabled. To disable the output, the PC port must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC port. Once disabled, 14 V must be re-applied to the VC port to restart the VTM.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5 Vdc.

+Out / -Out DC Voltage Output Ports

The output and output return are through two sets of contact locations. The respective +Out and –Out groups must be connected in parallel with as low an interconnect resistance as possible. Within the specified input voltage range, the Level 1 DC behavioral model shown in Figure 16 defines the output voltage of the VTM. The current source capability of the VTM is shown in the specification table.

To take full advantage of the VTM, the user should note the low output impedance of the device. The low output impedance provides fast transient response without the need for bulk POL capacitance. Limited-life electrolytic capacitors required with conventional converters can be reduced or even eliminated, saving cost and valuable board real estate.



Bottom View

Signal Name	Pin Designation
+In	A1-E1, A2-E2
–In	L1-T1, L2-T2
TM	H1, H2
VC	J1, J2
PC	K1, K2
+Out	A3-D3, A4-D4, J3-M3, J4-M4
–Out	E3-H3, E4-H4, N3-T3, N4-T4

Figure 9 *— VTM pin configuration*

Mechanical Drawings

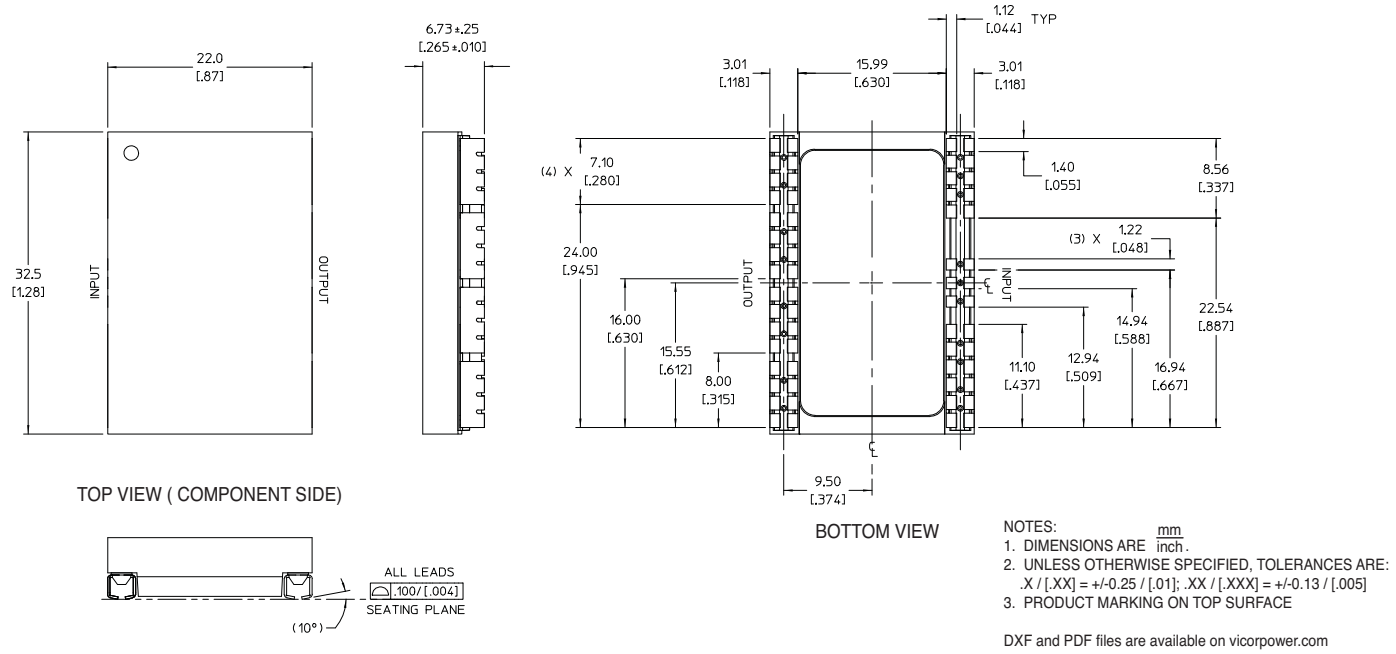


Figure 10 *— VTM J-Lead mechanical outline; Onboard mounting*

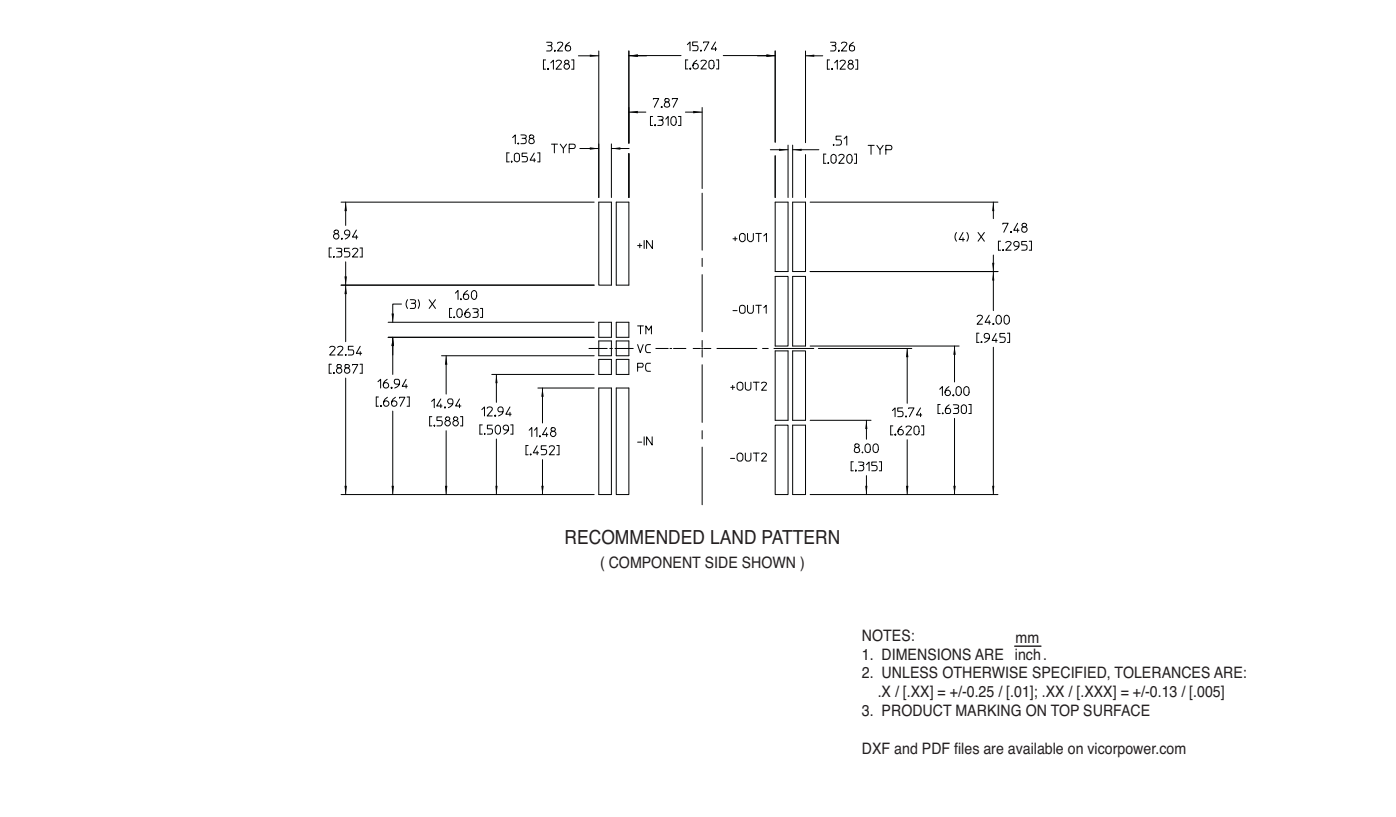


Figure 11 *— VTM J-Lead PCB land layout information; Onboard mounting*

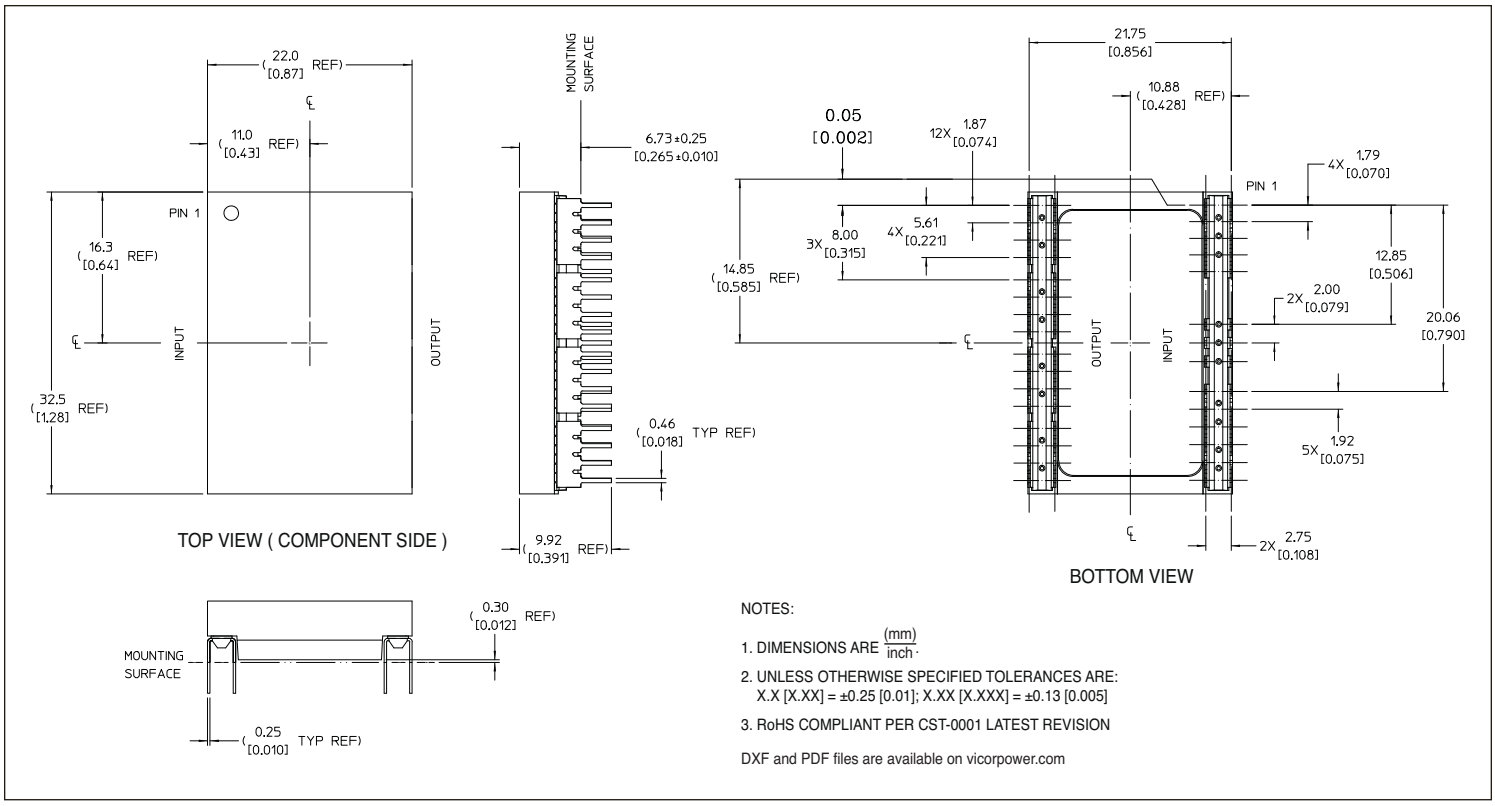


Figure 12 *— VTM Through-hole mechanical outline*

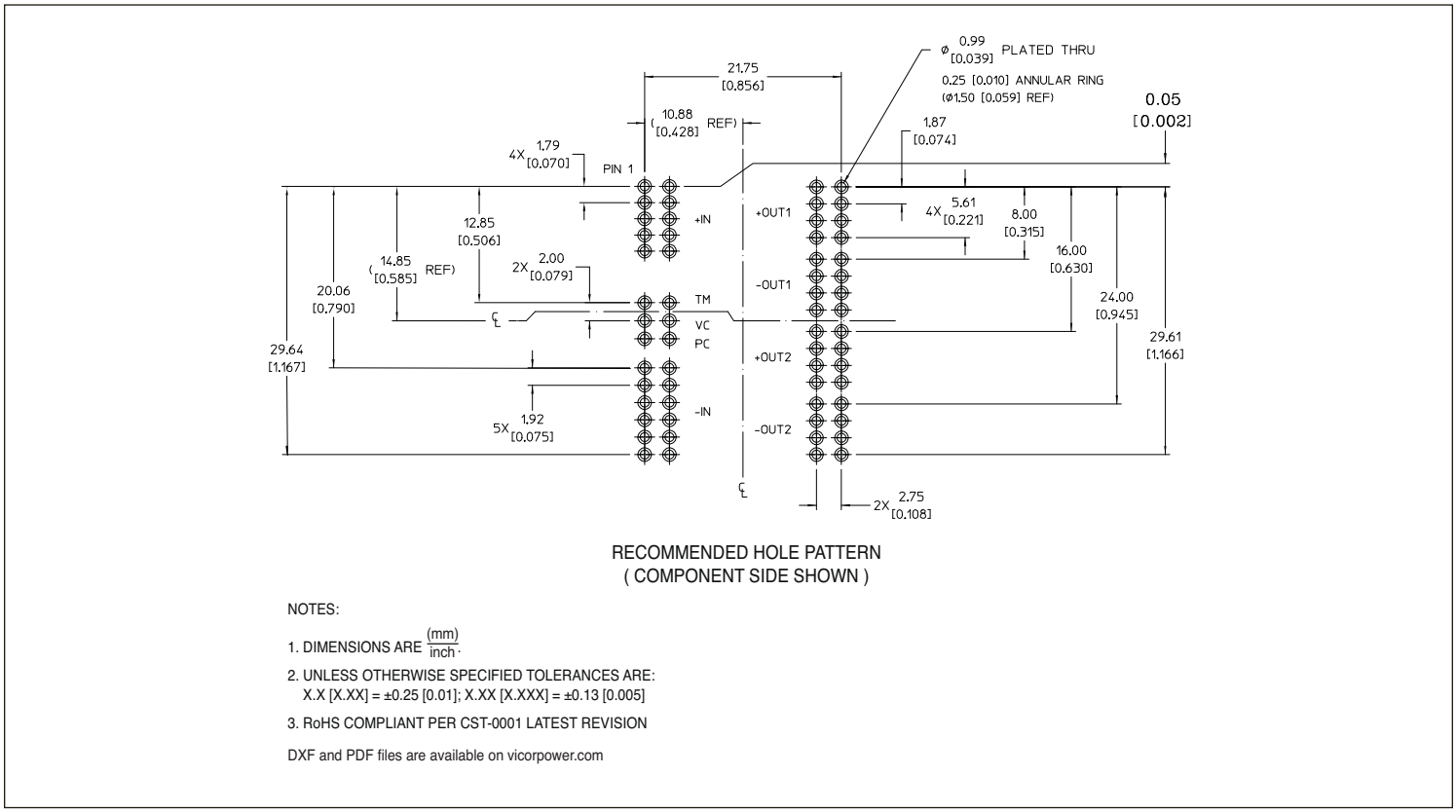
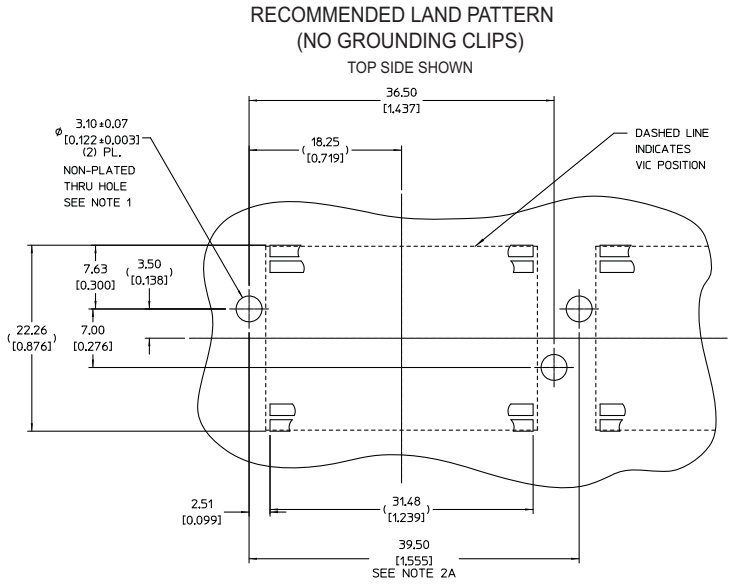
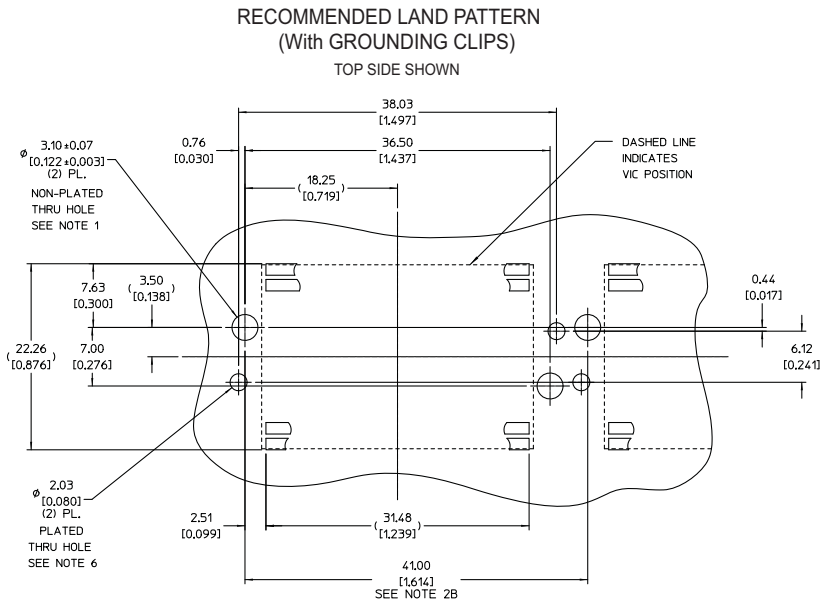


Figure 13 *— VTM Through-hole PCB layout information*





NOTES:

1. MAINTAIN 3.50 [0.138] DIA. KEEP-OUT ZONE FREE OF COPPER, ALL PCB LAYERS.
2. (A) MINIMUM RECOMMENDED PITCH IS 39.50 [1.555], THIS PROVIDES 7.00 [0.275] COMPONENT EDGE-TO-EDGE SPACING, AND 0.50 [0.020] CLEARANCE BETWEEN VICOR HEAT SINKS.

   (B) MINIMUM RECOMMENDED PITCH IS 41.00 [1.614], THIS PROVIDES 8.50 [0.334] COMPONENT EDGE-TO-EDGE SPACING, AND 2.00 [0.079] CLEARANCE BETWEEN VICOR HEAT SINKS.
3. V•I CHIP LAND PATTERN SHOWN FOR REFERENCE ONLY; ACTUAL LAND PATTERN MAY DIFFER. DIMENSIONS FROM EDGES OF LAND PATTERN TO PUSH-PIN HOLES WILL BE THE SAME FOR ALL FULL SIZE V•ICHIP PRODUCTS.
4. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
5. UNLESS OTHERWISE SPECIFIED:
   DIMENSIONS ARE MM [INCH].
   TOLERANCES ARE:
   X.X [X.XX] = ±0.3 [0.01]
   X.XX [X.XXX] = ±0.13 [0.005]
6. PLATED THROUGH HOLES FOR GROUNDING CLIPS (33855) SHOWN FOR REFERENCE. HEATSINK ORIENTATION AND DEVICE PITCH WILL DICTATE FINAL GROUNDING SOLUTION.

Figure 14 *— Hole location for push pin heat sink relative to V•I Chip*

Parallel Operation

In applications requiring higher current or redundancy, VTMs can be operated in parallel without adding control circuitry or signal lines. To maximize current sharing accuracy, it is imperative that the source and load impedance on each VTM in a parallel array be equal. If VTMs are being fed by an upstream PRM, the VC nodes of all VTMs must be connected to the PRM VC.

To achieve matched impedances, dedicated power planes within the PC board should be used for the output and output return paths to the array of paralleled VTMs. This technique is preferable to using traces of varying size and length.

The VTM power train and control architecture allow bi-directional power transfer when the VTM is operating within its specified ranges. Bi-directional power processing improves transient response in the event of an output load dump. The VTM may operate in reverse, returning output power back to the input source. It does so efficiently.

Thermal Considerations

V•I Chip products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input/output conditions, thermal management and environmental conditions. Maintaining the top of the V048F015T100 case to less than 100°C will keep all junctions within the V•I Chip below 125°C for most applications. The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.
It is not recommended to use a V•I Chip for an extended period of time at full load without proper heatsinking.

Input Impedance Recommendations

To take full advantage of the VTM's capabilities, the impedance of the source (input source plus the PC board impedance) must be low over a range from DC to 5 MHz. Input bypass capacitance may be added to improve transient performance or compensate for high source impedance. The VTM has extremely wide bandwidth so the source response to transients is usually the limiting factor in overall output response of the VTM.

Anomalies in the response of the source will appear at the output of the VTM, multiplied by its K factor of 1/32. The DC resistance of the source should be kept as low as possible to minimize voltage deviations on the input to the VTM. If the VTM is going to be operating close to the high limit of its input range, make sure input voltage deviations will not trigger the input overvoltage turn-off threshold.

Input Fuse Recommendations

V•I Chips are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of V•I Chips must always be incorporated within the power system. A fast acting fuse is required to meet safety agency Conditions of Acceptability. The input line fuse should be placed in series with the +In port.

Application Notes

For VTM and V•I Chip application notes on soldering, thermal management, board layout, and system design click on the link below:

http://www.vicorpower.com/technical_library/application_information/chips/

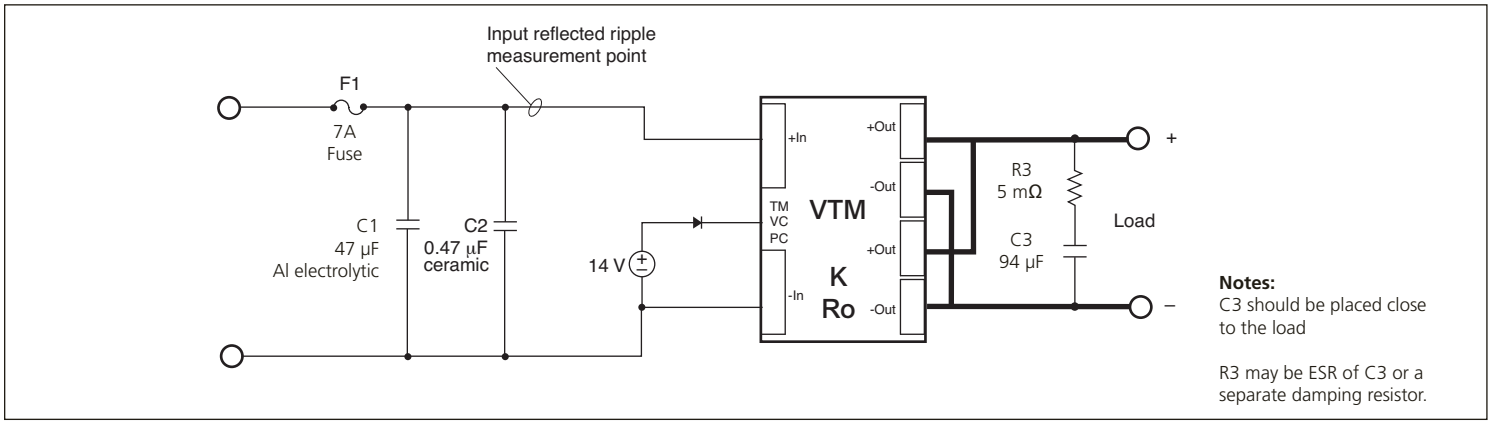


Figure 15 — *VTM test circuit*

V•I Chip VTM Level 1 DC Behavioral Model for 48 V to 1.5 V, 100.0 A

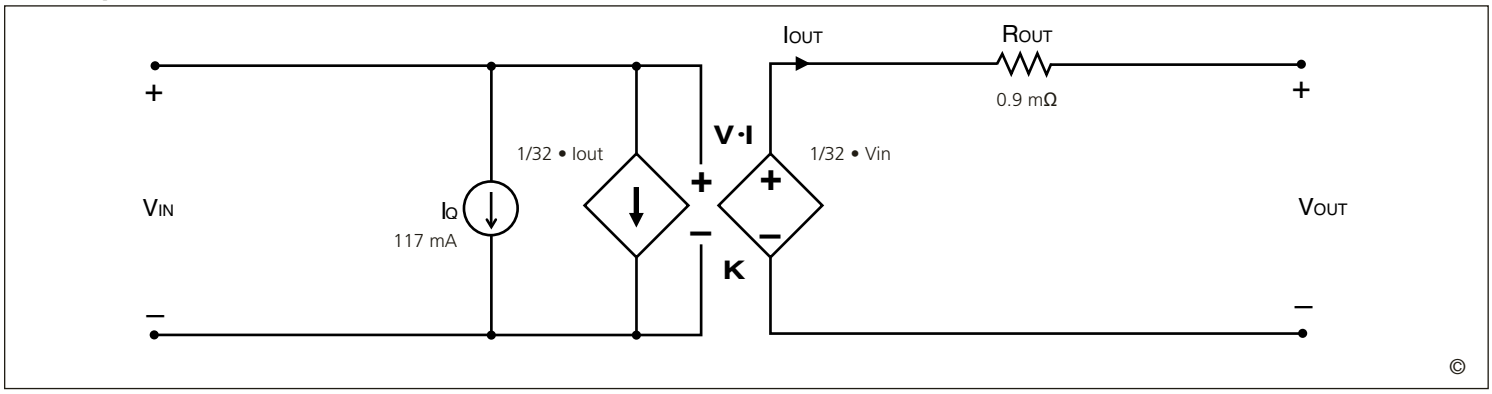


Figure 16 *— This model characterizes the DC operation of the V•I Chip VTM, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.*

V•I Chip VTM Level 2 Transient Behavioral Model for 48 V to 1.5 V, 100.0 A

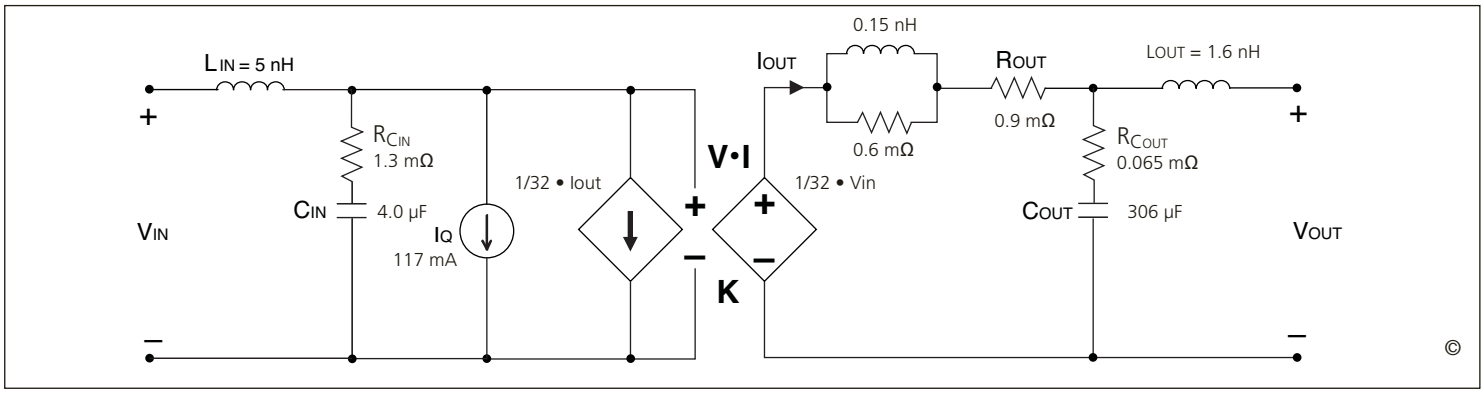


Figure 17 *— This model characterizes the AC operation of the V•I Chip VTM including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.*

In figures below;

K = VTM transformation ratio

R_O = VTM output resistance

V_f = PRM output (Factorized Bus Voltage)

V_O = VTM output

V_L = Desired load voltage

FPA Adaptive Loop

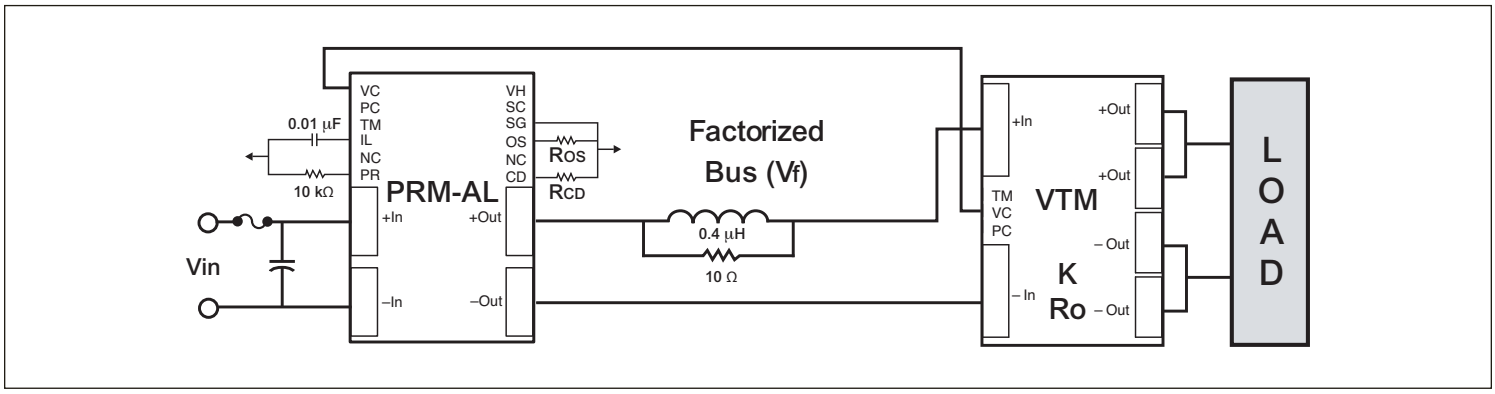


Figure 18 *— The PRM controls the factorized bus voltage, V_f, in proportion to output current to compensate for the output resistance, Ro, of the VTM. The VTM output voltage is typically within 1% of the desired load voltage (V_L) over all line and load conditions.*

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Technical Support: apps@vicorpower.com

Electrical Specifications

Input Specs (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	26.0	48	55	Vdc	Max Vin = 50 V, operating from -55°C to -20°C
Input dV/dt			1	V/µs	
Input overvoltage turn-on	55.1			Vdc	
Input overvoltage turn-off			59.5	Vdc	
Input current			3.6	Adc	
Input reflected ripple current		124		mA p-p	Using test circuit in Figure 15; See Figure 1
No load power dissipation		5.6	7.8	W	
Internal input capacitance		4.0		µF	
Internal input inductance			5	nH	

Output Specs (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Output voltage	0.820		1.71	Vdc	No load
	0.710		1.61	Vdc	Full load
Rated DC current	0		100.0	Adc	26 - 50 V_{IN}
Peak repetitive current			150.0	A	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
Short circuit protection set point	125			Adc	Module will shut down
Current share accuracy		5	10	%	See Parallel Operation on Page 9
Efficiency					
Half load	88.8	89.3		%	See Figure 3
Full load	88.6	89.2		%	See Figure 3
Internal output inductance		1.6		nH	
Internal output capacitance		306		µF	Effective value
Output overvoltage setpoint	1.7			Vdc	Module will shut down
Output ripple voltage					
No external bypass		100	200	mVp-p	See Figures 2 and 5
94 µF bypass capacitor		14		mVp-p	See Figure 6
Effective switching frequency	2.8	2.9	3.0	MHz	Fixed, 1.4 MHz per phase
Line regulation					
K	0.0309	1/32	0.0316		$V_{OUT} = K \bullet V_{IN}$ at no load
Load regulation					
R_{OUT}		0.9	1.1	mΩ	See Figure 16
Transient response					
Voltage overshoot		60		mV	100.0 A load step with 100 µF C_{IN}; See Figures 7 and 8
Response time		200		ns	See Figures 7 and 8
Recovery time		1		µs	See Figures 7 and 8

Waveforms

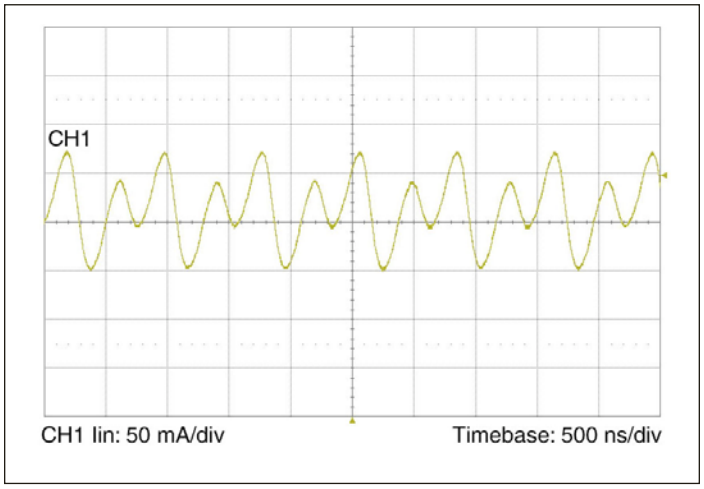


Figure 1 — *Input reflected ripple current at full load and 48 Vf.*

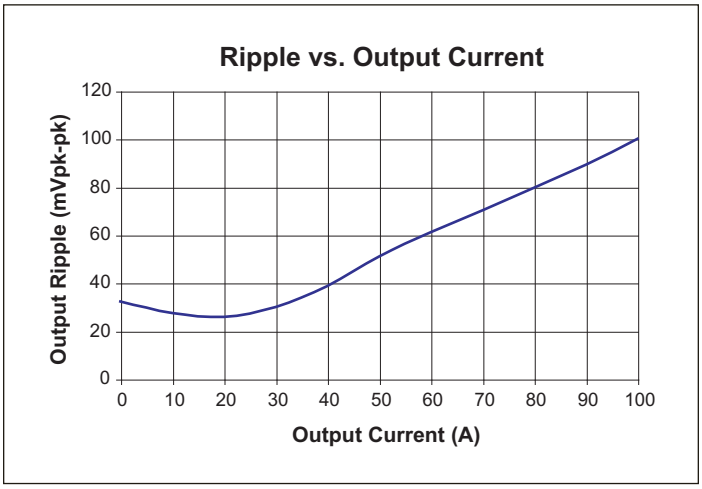


Figure 2 — *Output voltage ripple vs. output current at 48 Vf with no POL bypass capacitance.*

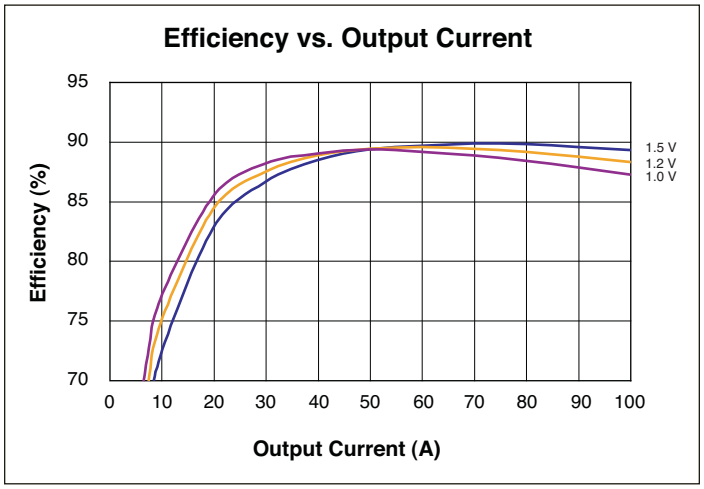


Figure 3 — *Efficiency vs. output current.*

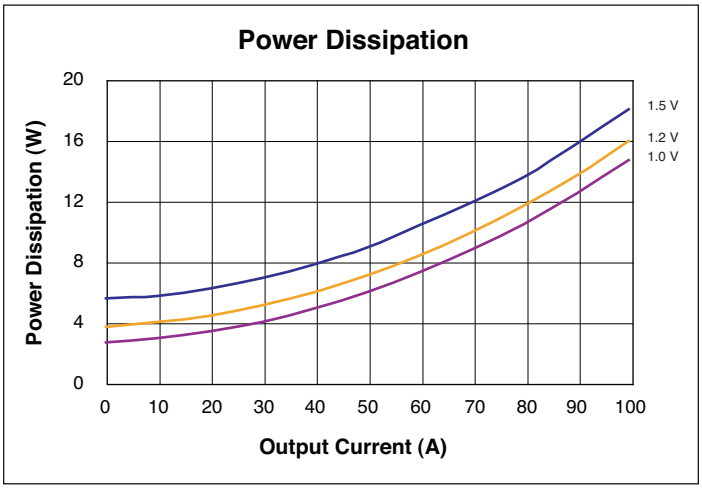


Figure 4 — *Power dissipation vs. output current.*

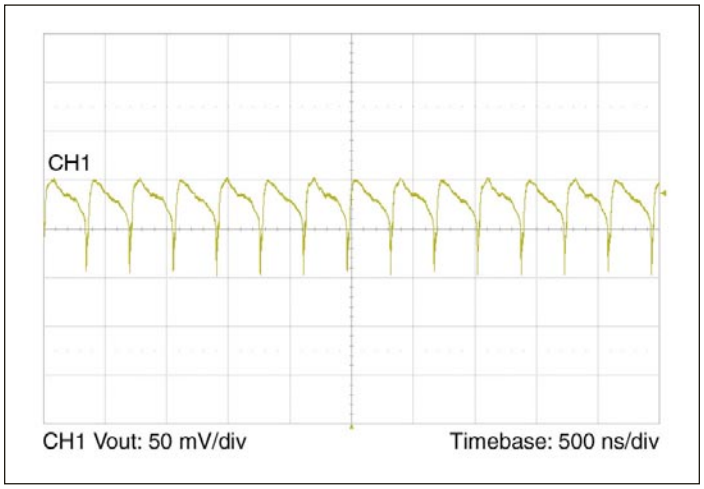


Figure 5 — *Output voltage ripple at full load and 48 Vf with no POL bypass capacitance.*

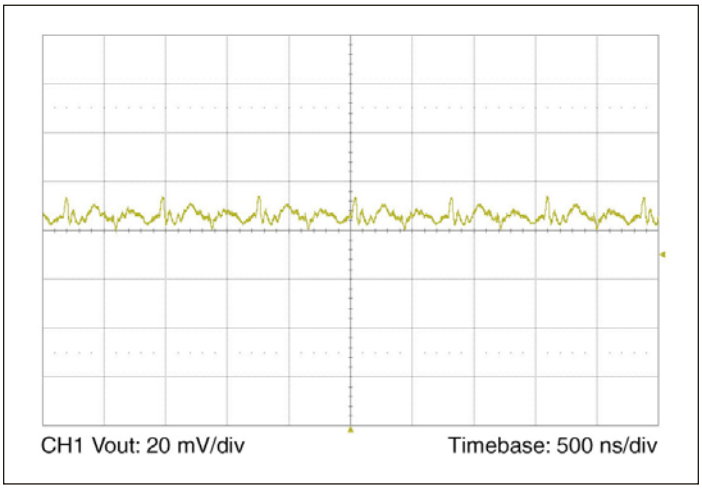


Figure 6 — *Output voltage ripple at full load and 48 Vf with 94 µF ceramic POL bypass capacitance and 20 nH distribution inductance.*

Electrical Specifications (continued)

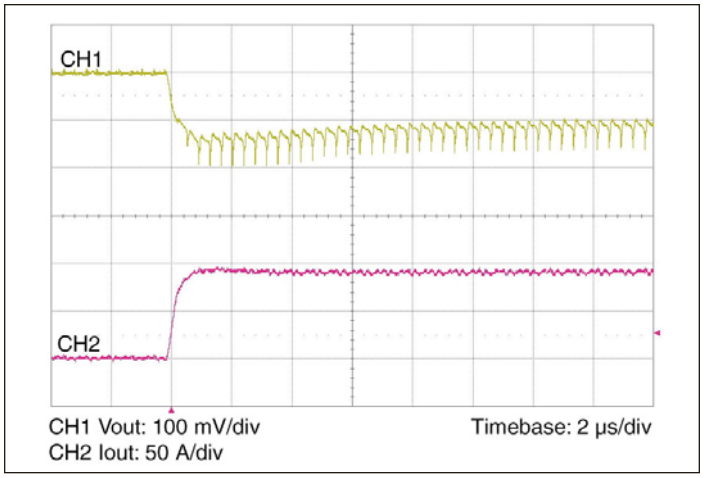


Figure 7 *— 0-100.0 A load step with 100 µF input capacitance and no output capacitance.*

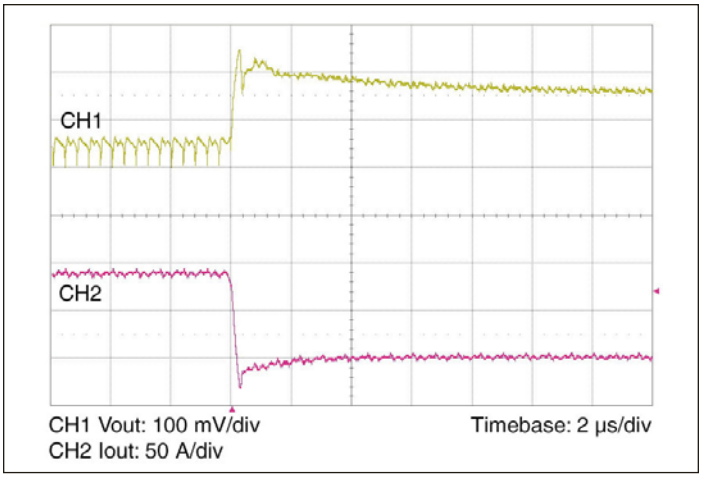


Figure 8 *— 100.0-0 A load step with 100 µF input capacitance and no output capacitance.*

General

Parameter	Min	Typ	Max	Unit	Note
MTBF					
MIL-HDBK-217F		3.5		Mhrs	25°C, GB
Isolation specifications					
Voltage	2,250			Vdc	Input to output
Capacitance		3,000		pF	Input to output
Resistance	10			MΩ	Input to output
Agency approvals		cTÜVus			UL/CSA 60950-1, EN 60950-1
		CE Mark			Low voltage directive
		RoHS			
Mechanical					See Mechanical Drawings, Figures 10 – 13
Weight		0.53/15		oz/g	
Dimensions					
Length		1.28/32,5		in/mm	
Width		0.87/22		in/mm	
Height		0.265/6,73		in/mm	
Peak compressive force applied to case (Z axis)		5	6	lbs.	Supported by J-leads only
Thermal					
Over temperature shutdown	125	130	135	°C	Junction temperature
Thermal capacity		9.3		Ws/°C	
Junction-to-case thermal impedance ($R_{\theta JC}$)		1.1		°C/W	See Thermal Considerations on Page 9
Junction-to-board thermal impedance ($R_{\theta JB}$)		2.1		°C/W	

Auxiliary Pins (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Primary Control (PC)					
DC voltage	4.8	5.0	5.2	Vdc	
Module disable voltage	2.4	2.5		Vdc	
Module enable voltage		2.5	2.6	Vdc	VC voltage must be applied when module is enabled using PC
Current limit	2.4	2.5	2.9	mA	Source only
Disable delay time		6		µs	PC low to Vout low
VTM Control (VC)					
External boost voltage	12	14	19	Vdc	Required for VTM start up without PRM
External boost duration		10		ms	Maximum duration of VC pulse = 20 ms

Pin / Control Functions

+In / -In DC Voltage Ports

The VTM input should be connected to the PRM output terminals. Given that both the PRM and VTM have high switching frequencies, it is often good practice to use a series inductor to limit high frequency currents between the PRM output and VTM input capacitors. The input voltage should not exceed the maximum specified. If the input voltage exceeds the overvoltage turn-off, the VTM will shutdown. The VTM does not have internal input reverse polarity protection. Adding a properly sized diode in series with the positive input or a fused reverse-shunt diode will provide reverse polarity protection.

TM – For Factory Use Only

VC – VTM Control

The VC port is multiplexed. It receives the initial V_{CC} voltage from an upstream PRM, synchronizing the output rise of the VTM with the output rise of the PRM. Additionally, the VC port provides feedback to the PRM to compensate for the VTM output resistance. In typical applications using VTMs powered from PRMs, the PRM's VC port should be connected to the VTM VC port.

The VC port is not intended to be used to supply V_{CC} voltage to the VTM for extended periods of time. If VC is being supplied from a source other than the PRM, the voltage should be removed after 20 ms.

PC – Primary Control

The Primary Control (PC) port is a multifunction port for controlling the VTM as follows:

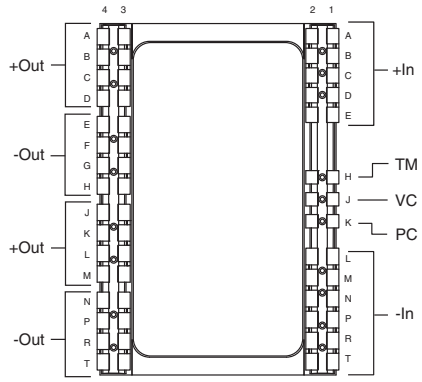
Disable – If PC is left floating, the VTM output is enabled. To disable the output, the PC port must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC port. Once disabled, 14 V must be re-applied to the VC port to restart the VTM.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5 Vdc.

+Out / -Out DC Voltage Output Ports

The output and output return are through two sets of contact locations. The respective +Out and –Out groups must be connected in parallel with as low an interconnect resistance as possible. Within the specified input voltage range, the Level 1 DC behavioral model shown in Figure 16 defines the output voltage of the VTM. The current source capability of the VTM is shown in the specification table.

To take full advantage of the VTM, the user should note the low output impedance of the device. The low output impedance provides fast transient response without the need for bulk POL capacitance. Limited-life electrolytic capacitors required with conventional converters can be reduced or even eliminated, saving cost and valuable board real estate.



Bottom View

Signal Name	Pin Designation
+In	A1-E1, A2-E2
–In	L1-T1, L2-T2
TM	H1, H2
VC	J1, J2
PC	K1, K2
+Out	A3-D3, A4-D4, J3-M3, J4-M4
–Out	E3-H3, E4-H4, N3-T3, N4-T4

Figure 9 *— VTM pin configuration*

Mechanical Drawings

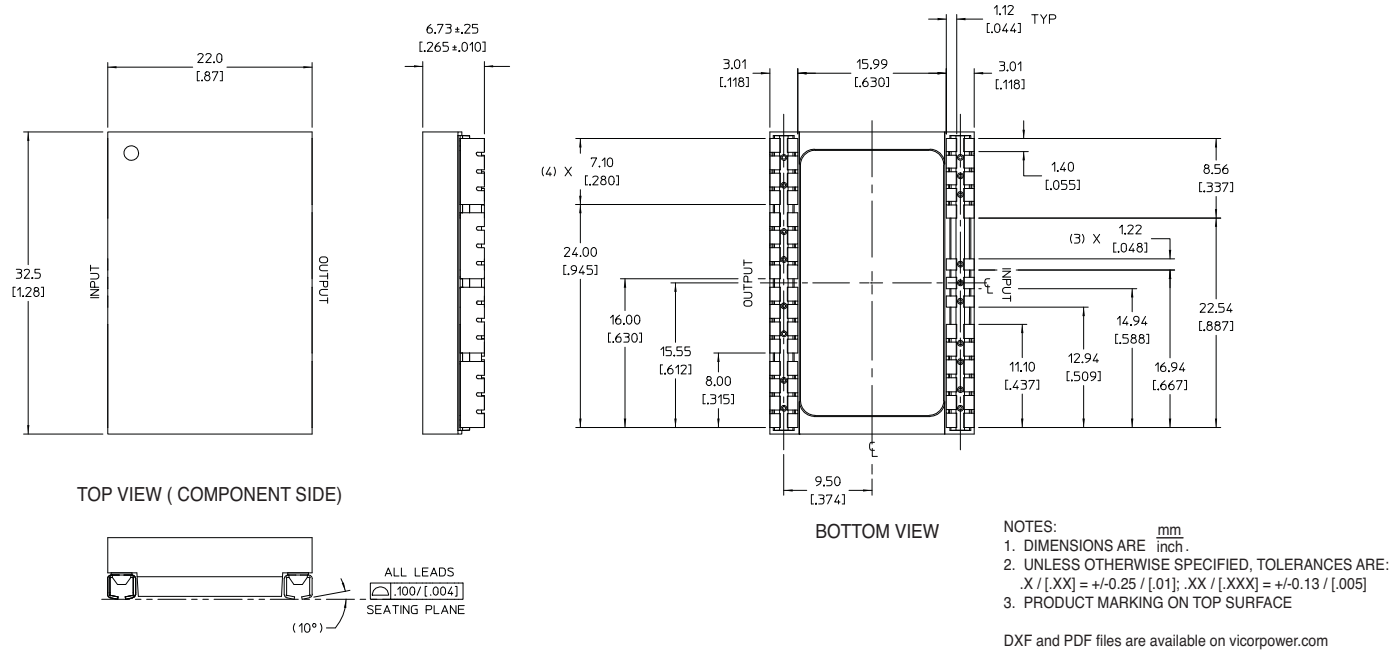


Figure 10 *— VTM J-Lead mechanical outline; Onboard mounting*

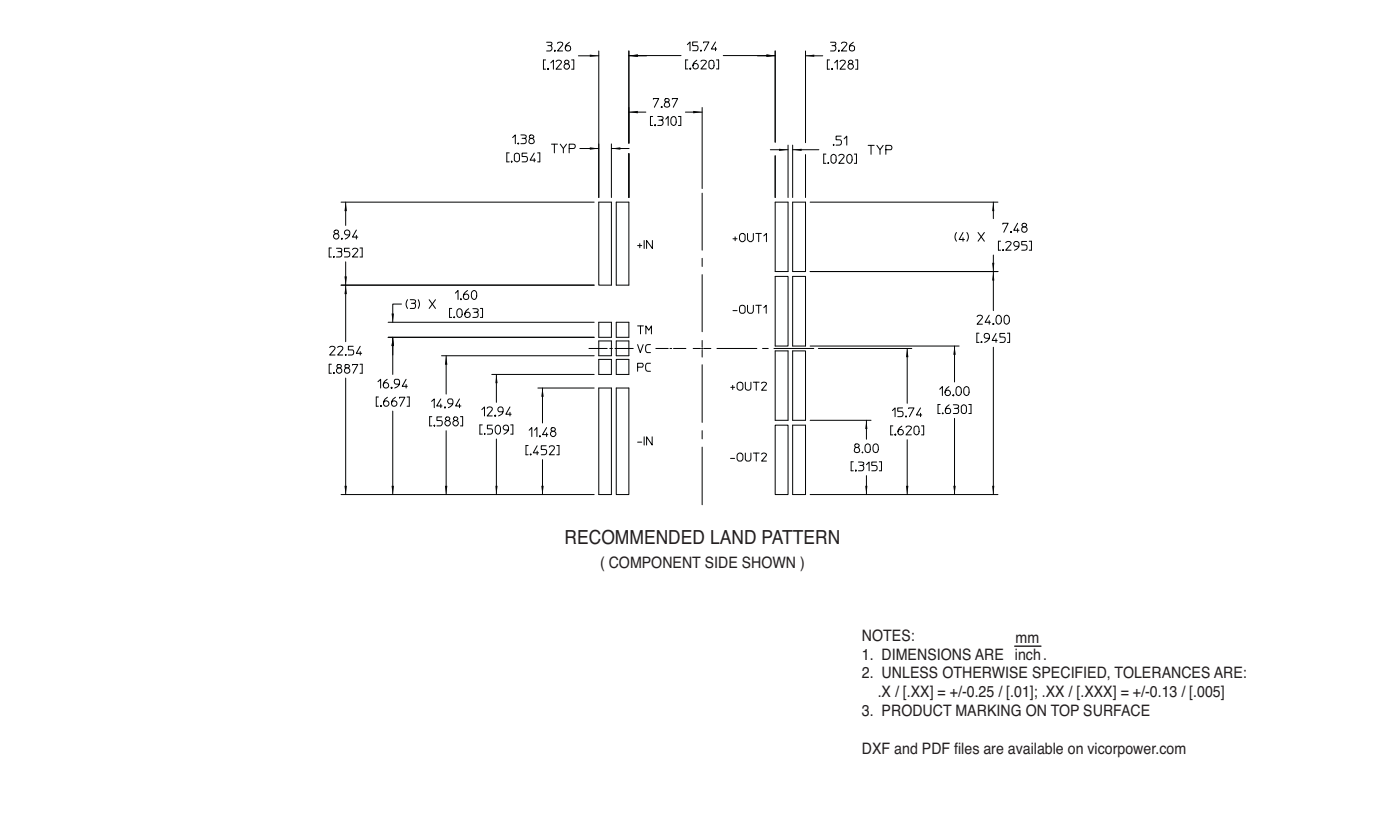


Figure 11 *— VTM J-Lead PCB land layout information; Onboard mounting*

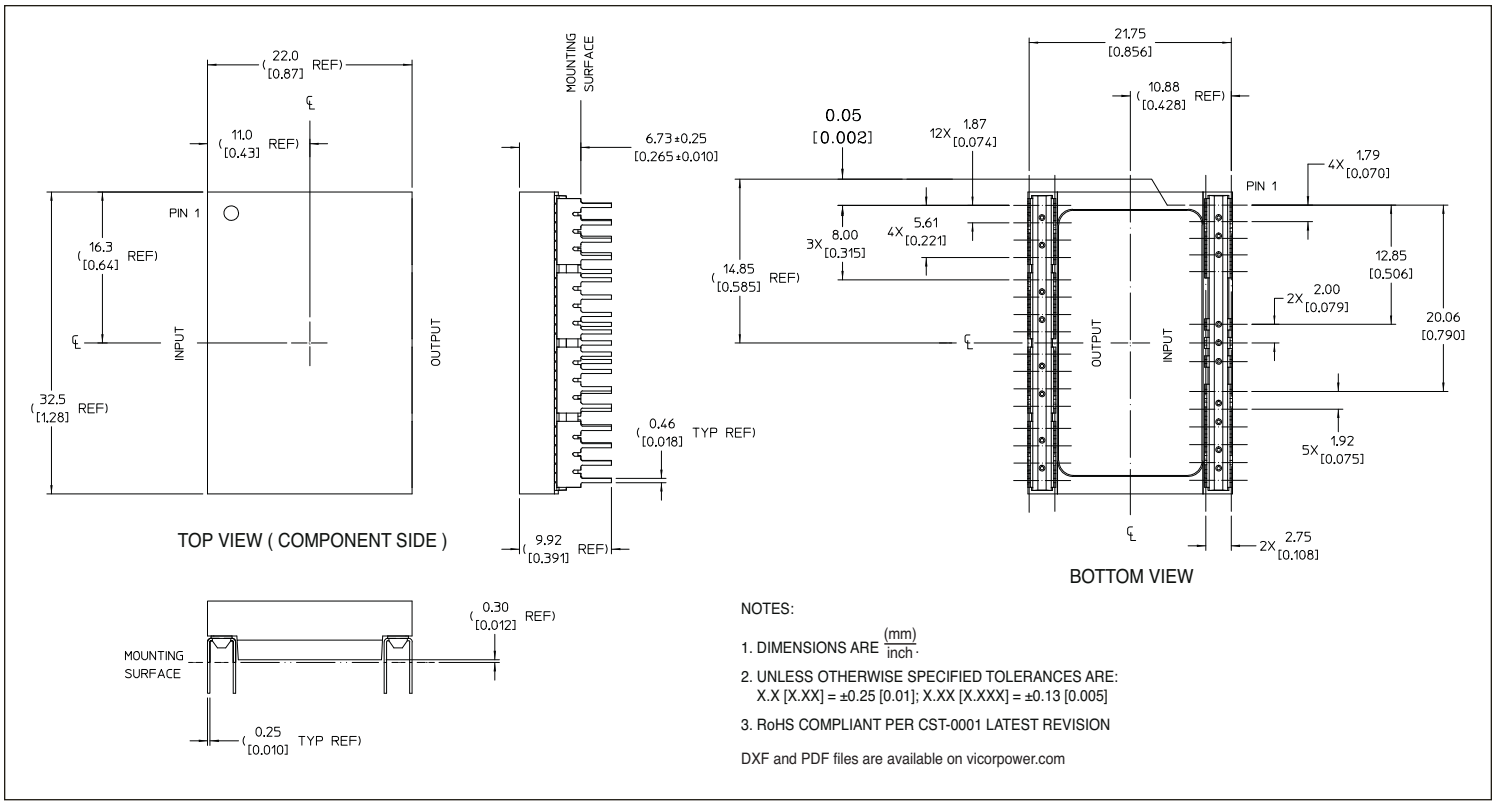


Figure 12 *— VTM Through-hole mechanical outline*

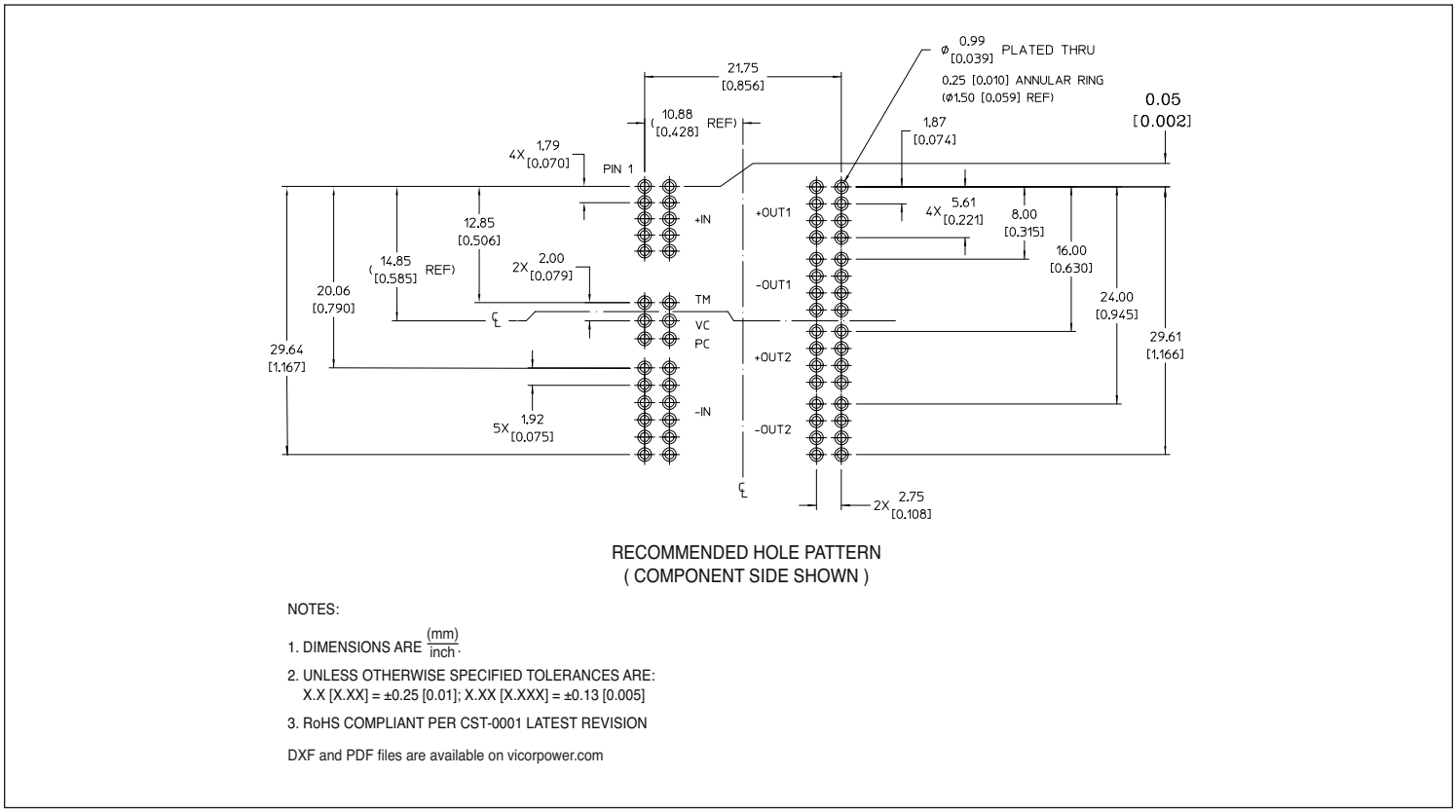
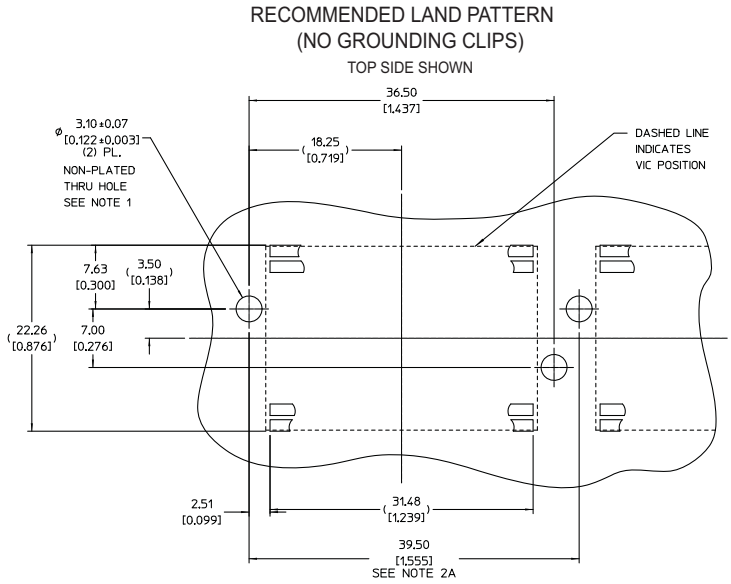
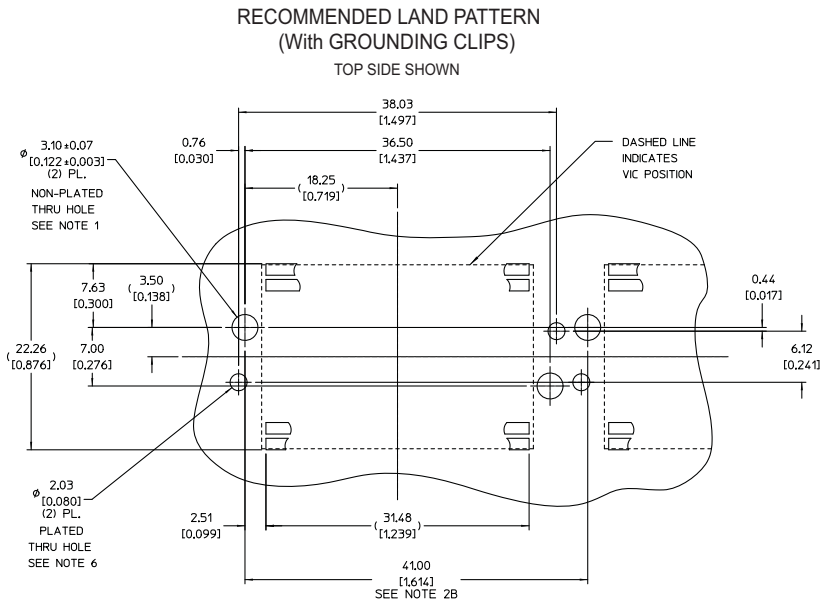


Figure 13 *— VTM Through-hole PCB layout information*





NOTES:

1. MAINTAIN 3.50 [0.138] DIA. KEEP-OUT ZONE FREE OF COPPER, ALL PCB LAYERS.
2. (A) MINIMUM RECOMMENDED PITCH IS 39.50 [1.555], THIS PROVIDES 7.00 [0.275] COMPONENT EDGE-TO-EDGE SPACING, AND 0.50 [0.020] CLEARANCE BETWEEN VICOR HEAT SINKS.

   (B) MINIMUM RECOMMENDED PITCH IS 41.00 [1.614], THIS PROVIDES 8.50 [0.334] COMPONENT EDGE-TO-EDGE SPACING, AND 2.00 [0.079] CLEARANCE BETWEEN VICOR HEAT SINKS.
3. V•I CHIP LAND PATTERN SHOWN FOR REFERENCE ONLY; ACTUAL LAND PATTERN MAY DIFFER. DIMENSIONS FROM EDGES OF LAND PATTERN TO PUSH-PIN HOLES WILL BE THE SAME FOR ALL FULL SIZE V•ICHIP PRODUCTS.
4. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
5. UNLESS OTHERWISE SPECIFIED:
   DIMENSIONS ARE MM [INCH].
   TOLERANCES ARE:
   X.X [X.XX] = ±0.3 [0.01]
   X.XX [X.XXX] = ±0.13 [0.005]
6. PLATED THROUGH HOLES FOR GROUNDING CLIPS (33855) SHOWN FOR REFERENCE. HEATSINK ORIENTATION AND DEVICE PITCH WILL DICTATE FINAL GROUNDING SOLUTION.

Figure 14 *— Hole location for push pin heat sink relative to V•I Chip*

Parallel Operation

In applications requiring higher current or redundancy, VTMs can be operated in parallel without adding control circuitry or signal lines. To maximize current sharing accuracy, it is imperative that the source and load impedance on each VTM in a parallel array be equal. If VTMs are being fed by an upstream PRM, the VC nodes of all VTMs must be connected to the PRM VC.

To achieve matched impedances, dedicated power planes within the PC board should be used for the output and output return paths to the array of paralleled VTMs. This technique is preferable to using traces of varying size and length.

The VTM power train and control architecture allow bi-directional power transfer when the VTM is operating within its specified ranges. Bi-directional power processing improves transient response in the event of an output load dump. The VTM may operate in reverse, returning output power back to the input source. It does so efficiently.

Thermal Considerations

V•I Chip products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input/output conditions, thermal management and environmental conditions. Maintaining the top of the V048F015T100 case to less than 100°C will keep all junctions within the V•I Chip below 125°C for most applications. The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.
It is not recommended to use a V•I Chip for an extended period of time at full load without proper heatsinking.

Input Impedance Recommendations

To take full advantage of the VTM's capabilities, the impedance of the source (input source plus the PC board impedance) must be low over a range from DC to 5 MHz. Input bypass capacitance may be added to improve transient performance or compensate for high source impedance. The VTM has extremely wide bandwidth so the source response to transients is usually the limiting factor in overall output response of the VTM.

Anomalies in the response of the source will appear at the output of the VTM, multiplied by its K factor of 1/32. The DC resistance of the source should be kept as low as possible to minimize voltage deviations on the input to the VTM. If the VTM is going to be operating close to the high limit of its input range, make sure input voltage deviations will not trigger the input overvoltage turn-off threshold.

Input Fuse Recommendations

V•I Chips are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of V•I Chips must always be incorporated within the power system. A fast acting fuse is required to meet safety agency Conditions of Acceptability. The input line fuse should be placed in series with the +In port.

Application Notes

For VTM and V•I Chip application notes on soldering, thermal management, board layout, and system design click on the link below:

http://www.vicorpower.com/technical_library/application_information/chips/

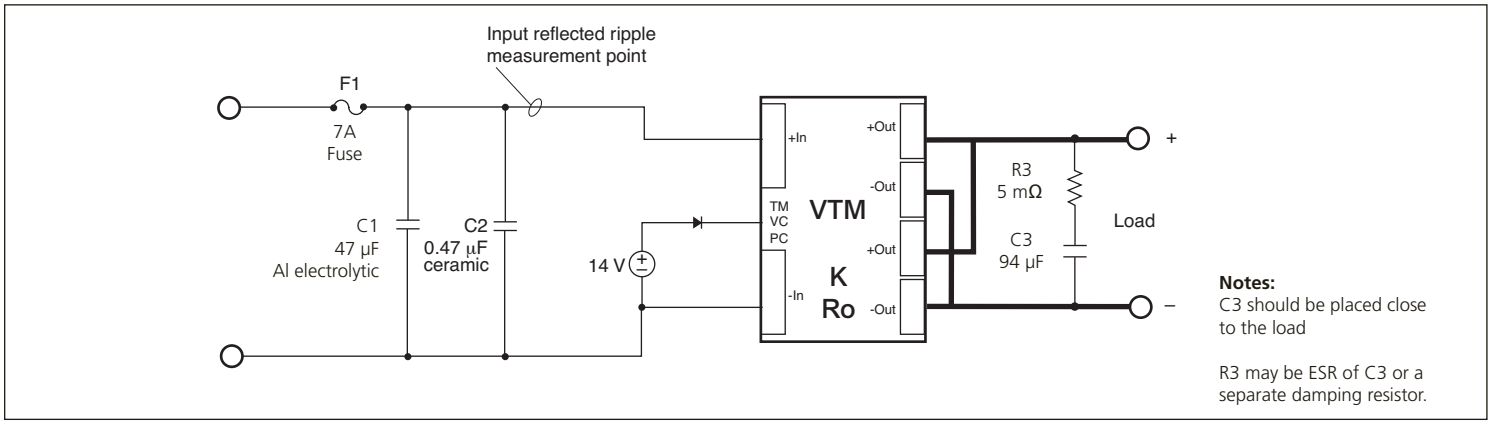


Figure 15 — *VTM test circuit*

V•I Chip VTM Level 1 DC Behavioral Model for 48 V to 1.5 V, 100.0 A

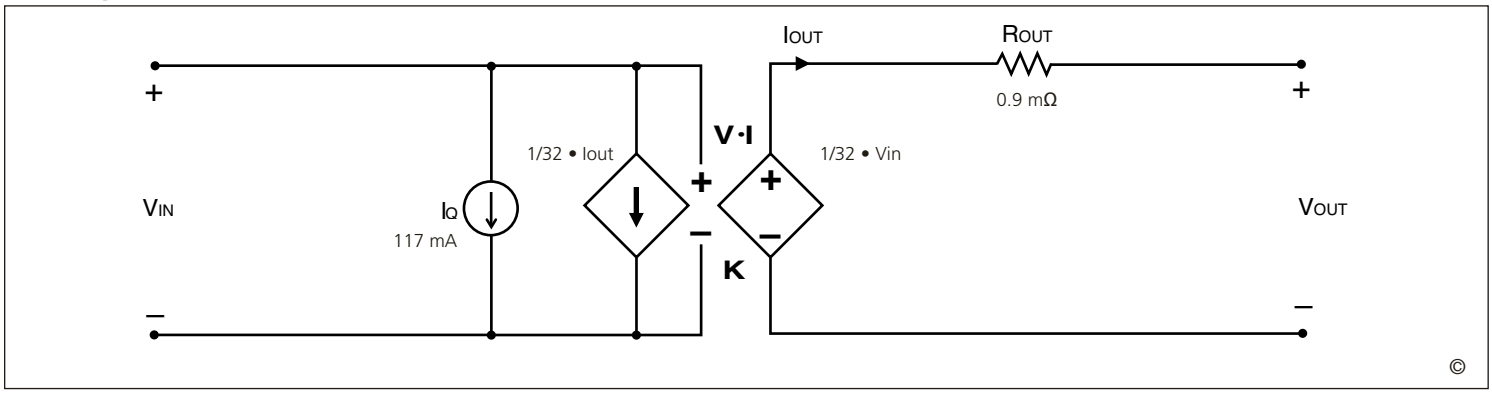


Figure 16 *— This model characterizes the DC operation of the V•I Chip VTM, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.*

V•I Chip VTM Level 2 Transient Behavioral Model for 48 V to 1.5 V, 100.0 A

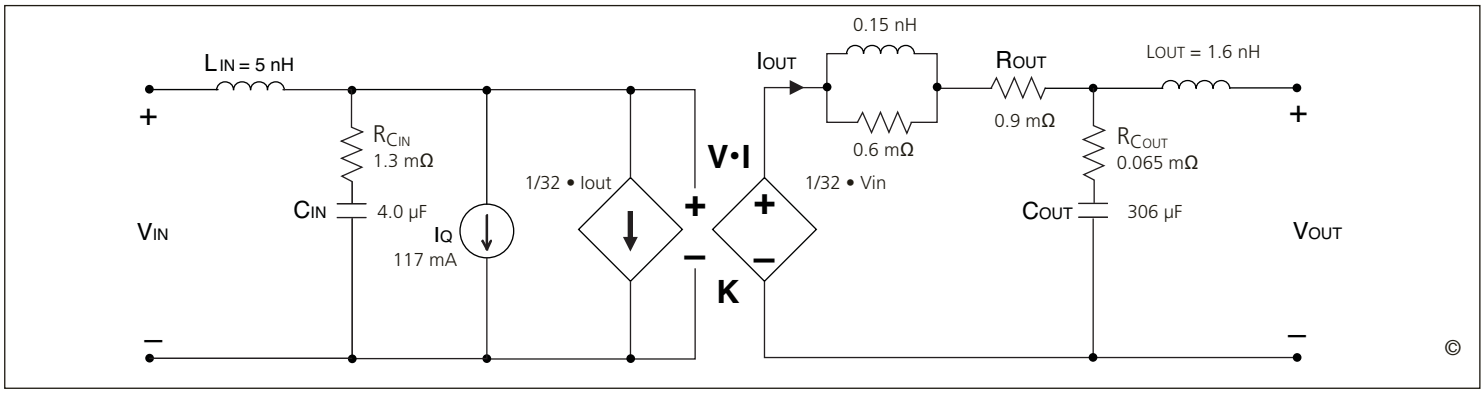


Figure 17 *— This model characterizes the AC operation of the V•I Chip VTM including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.*

In figures below;

K = VTM transformation ratio

R_O = VTM output resistance

V_f = PRM output (Factorized Bus Voltage)

V_O = VTM output

V_L = Desired load voltage

FPA Adaptive Loop

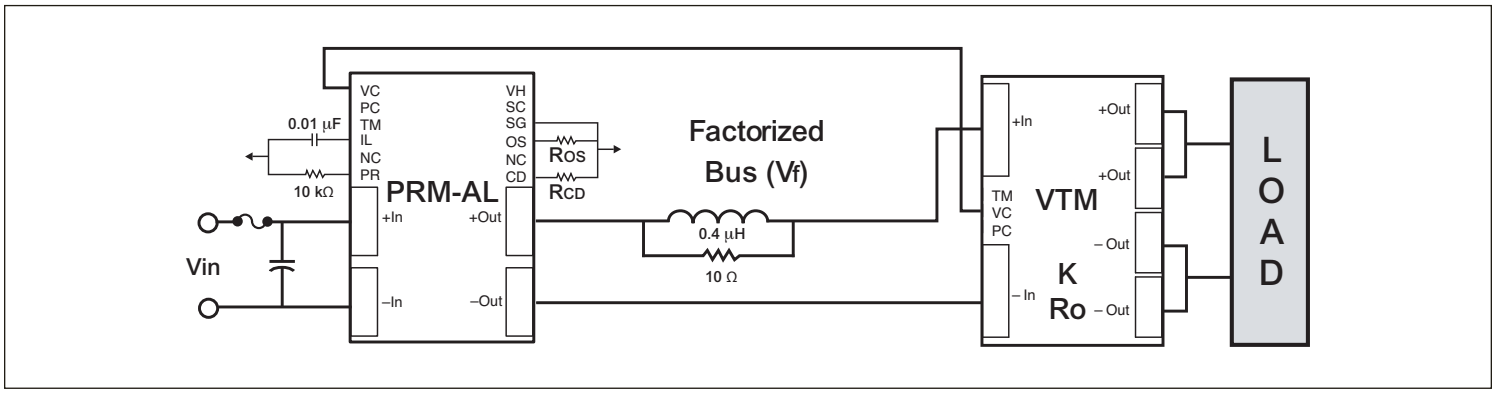


Figure 18 *— The PRM controls the factorized bus voltage, V_f, in proportion to output current to compensate for the output resistance, Ro, of the VTM. The VTM output voltage is typically within 1% of the desired load voltage (V_L) over all line and load conditions.*

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