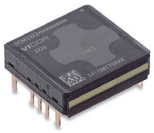
# DCM™ DC-DC Converter

## DCM2322xA5N0660y6z



## Isolated, Regulated DC Converter

### Features & Benefits

- Isolated, regulated DC-DC converter
- Up to 60W, 12.00A continuous
- 86.2% peak efficiency
- 241W/in$^3$ power density
- Wide input range 43 – 154$V_{DC}$
- Safety Extra Low Voltage (SELV) 5.0V nominal output
- 3000$V_{DC}$ isolation
- ZVS high-frequency switching
  - Enables low-profile, high-density filtering
- Dual modes of operation:
  - Array mode
    - Up to 8 units – 480W
    - No power de-rating needed
    - Sharing strategy permits dissimilar line voltages across an array
  - Enhanced $V_{OUT}$ regulation mode
    - Standalone 60W
- Fully operational current limit
- OV, OC, UV, short circuit and thermal shut down

### Typical Applications

- Rail Transportation
- Defense / Aerospace
- Industrial
- Process Control

| Product Ratings | |
|---|---|
| $V_{IN}$ = 43 – 154V | $P_{OUT}$ = 60W |
| $V_{OUT}$ = 5.0V (3.5 – 5.5V Trim) | $I_{OUT}$ = 12.00A |

### Product Description

The DCM2322 is a lower-power, isolated and regulated DC-DC converter that operates from an unregulated, wide-range input to generate an isolated 5.0$V_{DC}$ output. With its high-frequency zero-voltage switching (ZVS) topology, the DCM2322 converter consistently delivers high efficiency across the input line range. Modular DCM converters and downstream DC-DC products support efficient power distribution, providing superior power system performance and connectivity from a variety of unregulated power sources to the point-of-load.

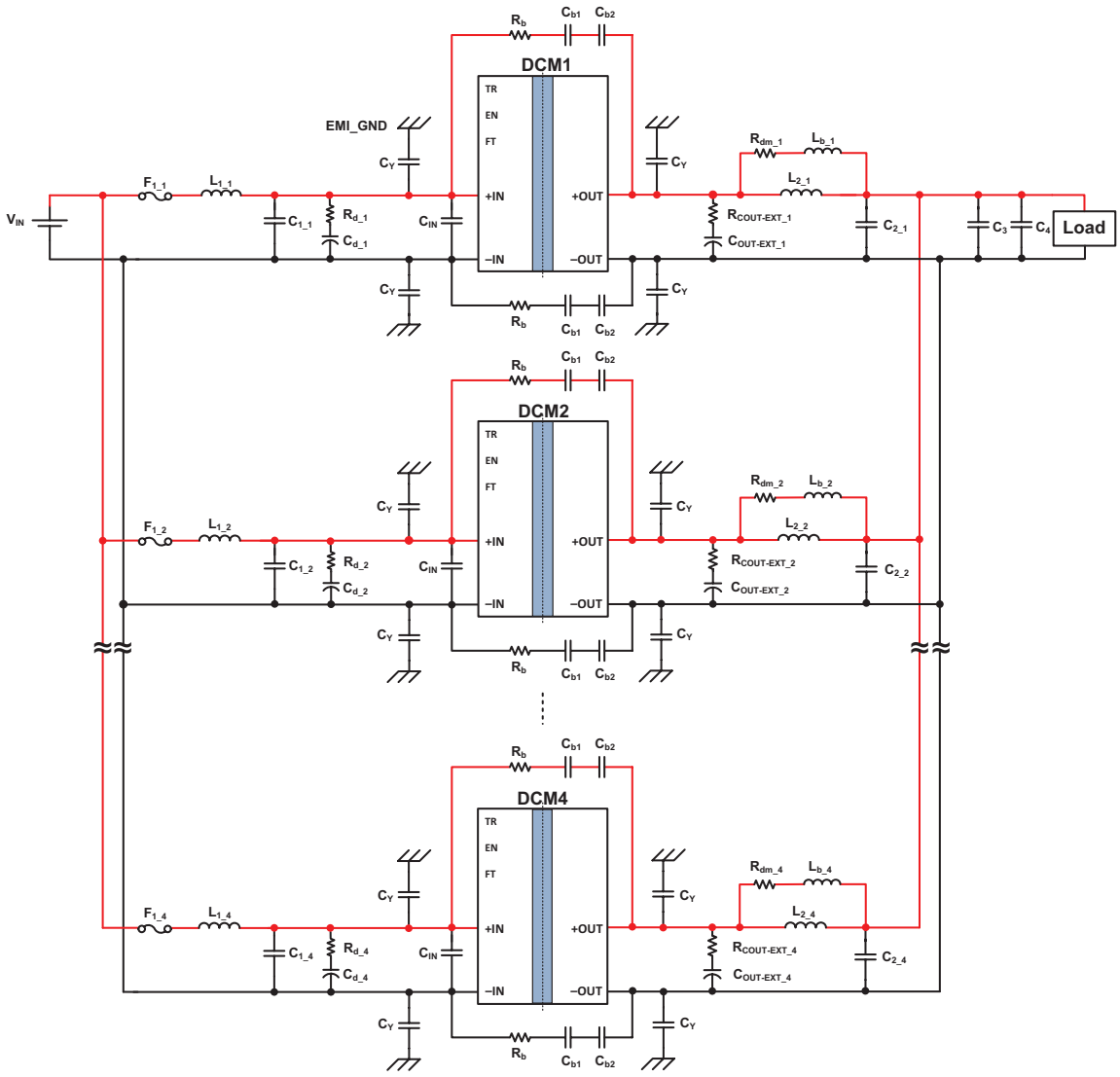
Leveraging the thermal and density benefits of Vicor ChiP packaging technology, the DCM2322 offers flexible thermal management options with very low top- and bottom-side thermal impedances. Thermally-adept ChiP-based power components enable customers to quickly and predictably achieve cost-effective power-system solutions.

### Package Information

- Through-hole ChiP™ package
  - 0.978 x 0.898 x 0.284in [24.84 x 22.80 x 7.21mm]
  - Weight: 14.4g [0.51oz]

**Note:** Product images may not highlight current product markings and cosmetic features.

## Typical Applications

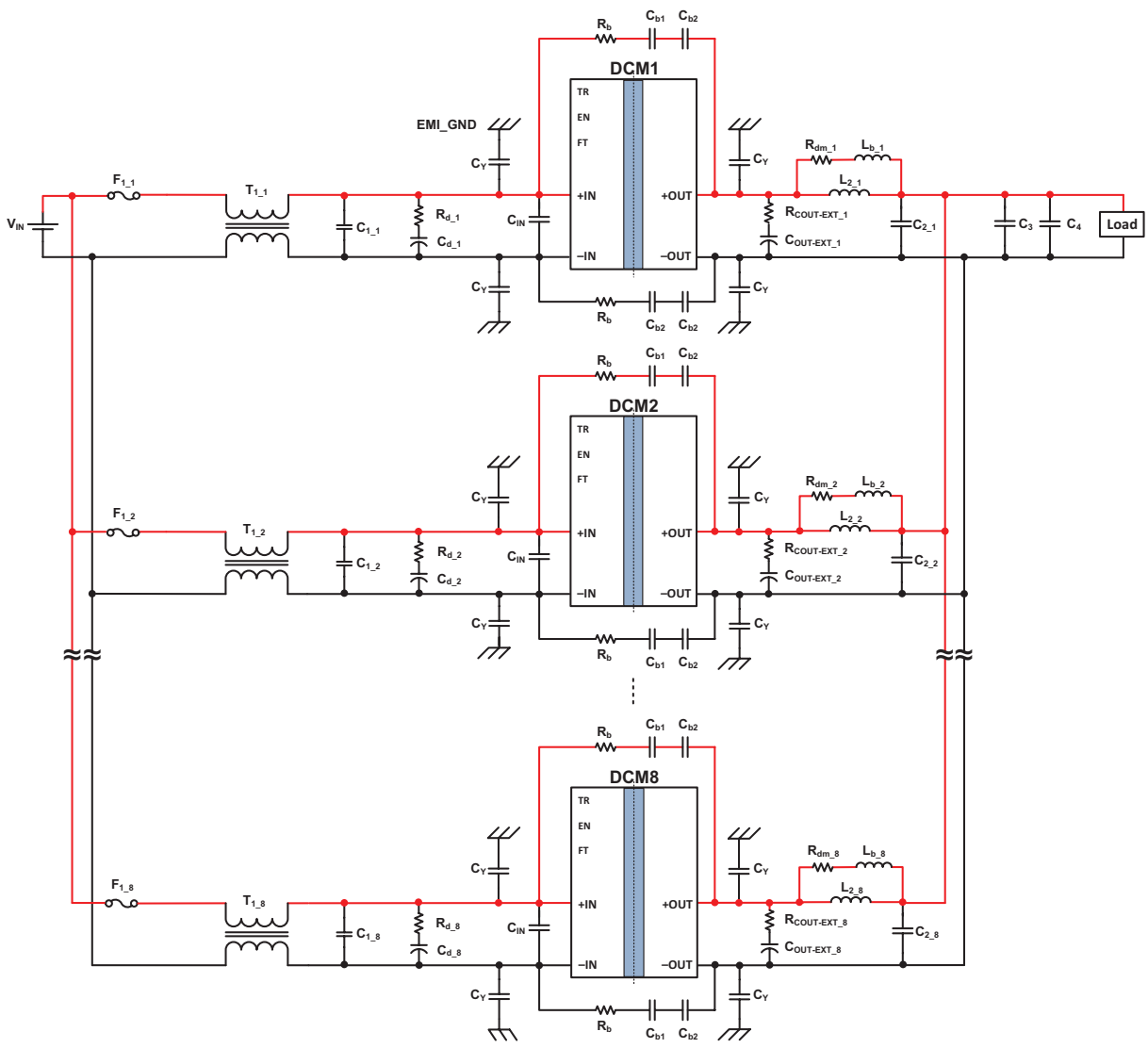



**Note:** $C_{IN}$, $R_b$, $C_{b1}$ and $C_{b2}$ are required components for proper operation of the DCM. See required components table below.

*DCM2322xA5N0660y6z in an array of four units; applicable when DCM is operating in Array Mode*

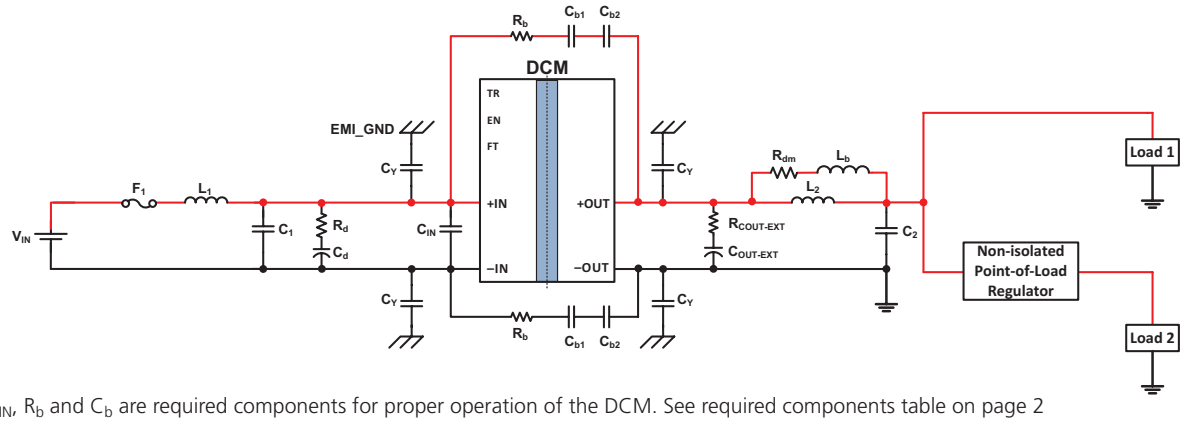
| Required Components | |
|---|---|
| $C_{IN}$ | **TDK** C5750X7T2E225M250KA, 2.2µF, 250V |
| $R_b$ | **Generic** 1Ω, 1/4W |
| $C_{b1}$ , $C_{b2}$ | **KEMET** C1812C103KGRACTU, 10,000pF, 2000V |

## Typical Applications (Cont.)




**Note:** $C_{IN}$, $R_b$, $C_{b1}$ and $C_{b2}$ are required components for proper operation of the DCM. See required components table on page 2.

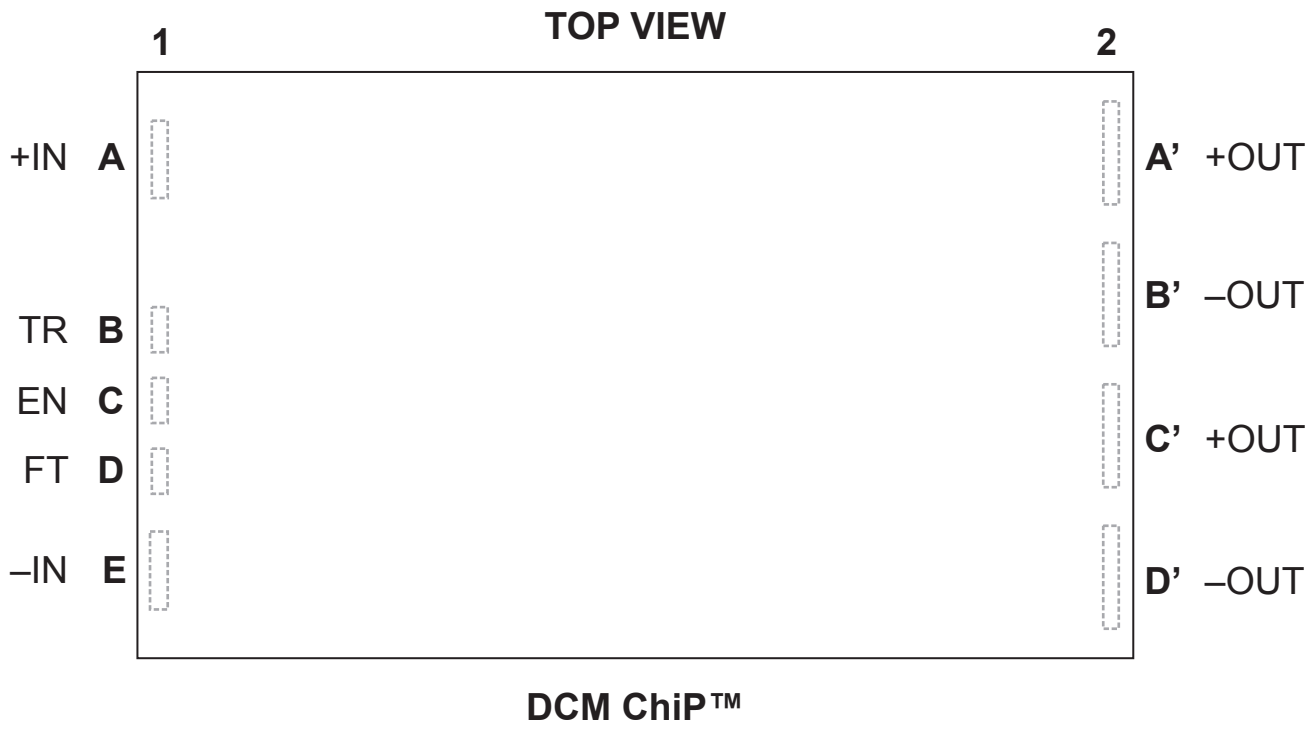
*Parallel operation of DCMs with common-mode chokes installed on the input side to suppress common-mode noise; applicable when DCM is operating in Array Mode*




**Note:** $C_{IN}$, $R_b$ and $C_b$ are required components for proper operation of the DCM. See required components table on page 2

*Single DCM2322xA5N0660y6z to a non-isolated regulator and direct-to-load*

## Pin Configuration




## Pin Descriptions

| Pin Number | Signal Name | Type | Function |
|---|---|---|---|
| A1 | +IN | INPUT POWER | Positive input power terminal |
| B1 | TR | INPUT | Enables and disables trim functionality; adjusts output voltage when trim active |
| C1 | EN | INPUT | Dual function:<br>1. Enables either Array or Enhanced $V_{OUT}$ Regulation Mode<br>2. Enables and disables power supply |
| D1 | FT | OUTPUT | Fault monitoring |
| E1 | –IN | INPUT POWER RETURN | Negative input power terminal |
| A'2, C'2 | +OUT | OUTPUT POWER | Positive output power terminal |
| B'2, D'2 | –OUT | OUTPUT POWER RETURN | Negative output power terminal |

## Part Ordering Information

| Part Number | Temperature Grade | Option | Tray Size |
|---|---|---|---|
| DCM2322TA5N0660**T60** | **T** = –40 to 125°C | **60** = Array and Enhanced $V_{OUT}$ Regulation Modes / Analog control Interface Version | 323 x 136 x 16mm 24 parts per tray |
| DCM2322TA5N0660**M60** | **M** = –55 to 125°C | | |

## Storage and Handling Information

Note: For compressive loading refer to Application Note AN:036, "Recommendations for Maximum Compressive Force of Heat Sinks."
For handling and assembly processing refer to Application Note AN:031, "Through-Hole ChiP™ Package Soldering Guidelines."

| Parameter | Comments | Specification |
|---|---|---|
| Storage Temperature Range | T-Grade | –40 to 125°C |
| | M-Grade | –65 to 125°C |
| Operating Internal Temperature Range ($T_{INT}$) | T-Grade | –40 to 125°C |
| | M-Grade | –55 to 125°C |
| Peak Temperature Top Case (Soldering) [a] | For further information, please contact factory applications | 135°C |
| Lead Finish | Nickel | 0.51 – 2.03µm |
| | Palladium | 0.02 – 0.15µm |
| | Gold | 0.003 – 0.051µm |
| Weight | | 14.4g [0.51oz] |
| MSL Rating | Not applicable to through-hole ChiP products | N/A |
| ESD Rating | Method per Human Body Model (HBM) Test ESDA / JEDEC JDS-001-2012 | Class 1C |
| | Charged Device Model (CDM) JESD22-C101E | Class 2 |

[a] Product is not intended for reflow solder attach.

## Safety, Reliability and Agency Approvals

| Parameter | Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Dielectric Withstand Test | IN to OUT | **3000** | | | $V_{DC}$ |
| | IN to CASE | **1500** | | | $V_{DC}$ |
| | OUT to CASE | **1500** | | | $V_{DC}$ |
| Insulation Resistance | IN to OUT, IN to CASE, OUT to CASE at 500$V_{DC}$, 1 minute | 50 | | | MΩ |
| MTBF | MIL-HDBK-217 FN2 Parts Count 25°C Ground Benign, Stationary, Indoors / Computer | | 3.84 | | MHrs |
| | Telcordia Issue 2, Method I Case 3, 25°C, 100% D.C., GB, GC | | 8.95 | | |
| Agency Approvals/Standards | | | | | |
| | cCSAus, UL 62368-1, CAN/CSA-C22.2 No. 62368-1 | | | | |
| | cTÜVus, EN IEC 62368-1, UL 62368-1, CSA-C22.2 No. 62368-1 | | | | |
| | UKCA, electrical equipment (safety) regulations | | | | |
| | CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable | | | | |

## Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device. Electrical specifications do not apply when operating beyond rated operating conditions.

| Parameter | Comments | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage (+IN to –IN) | | -0.5 | 175.0 | V |
| Input Voltage Slew Rate | | -1 | 1 | V/µs |
| TR to –IN | | -0.3 | 3.5 | V |
| EN to –IN | | -0.3 | 3.5 | V |
| FT to –IN | | -0.3 | 3.5 | V |
| | | | 5 | mA |
| Output Voltage (+OUT to –OUT) | | -0.5 | 6.6 | V |
| Dielectric Withstand (Input to Output) | Supplementary insulation | 3000 | | $V_{DC}$ |
| Average Output Current | | | 17.0 | A |

## Common Electrical Specifications for Array and Enhanced $V_{OUT}$ Regulation Operation

Specifications apply over all line, trim and load conditions, internal temperature $T_{INT}$ = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C < $T_{INT}$ < 125°C for T-Grade and –55°C < $T_{INT}$ < 125°C for M-Grade.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Power Input Specifications** | | | | | | |
| Input Voltage Range | $V_{IN}$ | Continuous operation | **43** | **100** | **154** | V |
| Inrush Current (Peak) | $I_{INRP}$ | With maximum $C_{OUT-EXT}$, full resistive load | | | **6.0** | A |
| Input Capacitance (Internal) | $C_{IN-INT}$ | Effective value at nominal input voltage | | 1.3 | | µF |
| Input Capacitance (Internal) ESR | $R_{CIN-INT}$ | At 1MHz | | 2.68 | | mΩ |
| Input Inductance (External) | $L_{IN}$ | Differential mode, with no further line bypassing | | | **1** | µH |
| | | | | | | |
| **No-Load Specifications** | | | | | | |
| Input Power – Disabled | $P_Q$ | Nominal line, see Figure 4 | | 0.6 | 0.8 | W |
| | | Worst case line, see Figure 4 | | | **1.0** | |
| Input Power – Enabled with No Load | $P_{NL}$ | Nominal line, see Figure 5 | | 2.0 | 3.0 | W |
| | | Worst case line, see Figure 5 | | | **3.5** | |
| | | | | | | |
| **Power Output Specifications** | | | | | | |
| Output Voltage Set Point | $V_{OUT-NOM}$ | $V_{IN}$ = 100V, nominal trim, at 100% load, $T_{INT}$ = 25°C | 4.97 | 5.0 | 5.03 | V |
| Rated Output Voltage Trim Range | $V_{OUT-TRIMMING}$ | Specifies the low, nominal and high trim conditions<br>• Array Mode: trim range over temp at full load<br>• Enhanced $V_{OUT}$ Regulation Mode: trim range over temp, with >10% rated load | **3.5** | **5.0** | **5.5** | V |
| Rated Output Power | $P_{OUT}$ | Continuous, $V_{OUT}$ ≥ 5.0V | **60** | | | W |
| Rated Output Current | $I_{OUT}$ | Continuous, $V_{OUT}$ ≤ 5.0V | **12.00** | | | A |
| Output Current Limit | $I_{OUT-LIM}$ | Of rated $I_{OUT}$ max; fully operational current limit, for nominal trim and below | 100 | 120 | 140 | % |
| Current Limit Delay | $t_{IOUT-LIM}$ | The module will power limit in a fast transient event | | 1 | | ms |
| Efficiency | η | Full load, nominal line, nominal trim | 84.8 | 86.2 | | % |
| | | Full load, over line and temperature, nominal trim | **80.0** | | | |
| | | 50% load, over rated line, temperature and trim | **75.0** | | | |
| Output Voltage Ripple | $V_{OUT-PP}$ | 20MHz bandwidth. At nominal trim, minimum $C_{OUT-EXT}$ and at least 10% rated load | | 296 | | mV |
| Output Capacitance (Internal) | $C_{OUT-INT}$ | Effective value at nominal output voltage | | 160 | | µF |
| Output Capacitance (Internal) ESR | $R_{COUT-INT}$ | At 1MHz | | 0.183 | | mΩ |
| Output Capacitance (External) | $C_{OUT-EXT}$ | Excludes component temperature coefficient for load transients that remain >10% rated load | **470** | | **10000** | µF |
| | $C_{OUT-EXT-TRANS}$ | Excludes component temperature coefficient for load transients down to $I_{TRAN\_MIN}$ rated load, with static trim | **2200** | | **10000** | |
| | $C_{OUT-EXT-TRANS-TRIM}$ | Excludes component temperature coefficient for load transients down to $I_{TRAN\_MIN}$ rated load, with dynamic trimming | **4700** | | **10000** | |
| Minimum Transient Load | $I_{TRAN\_MIN}$ | Minimum required load for proper operation of DCM during load transient conditions | 0 | | | % |
| Output Capacitance ESR (External) | $R_{COUT-EXT}$ | At 10kHz, excludes component tolerances | **10** | | | mΩ |

## Common Electrical Specifications for Array and Enhanced $V_{OUT}$ Regulation Operation (Cont.)

Specifications apply over all line, trim and load conditions, internal temperature $T_{INT}$ = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C < $T_{INT}$ < 125°C for T-Grade and –55°C < $T_{INT}$ < 125°C for M-Grade.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Power Output Specifications (Cont.)** | | | | | | |
| Initialization Delay | $t_{INIT}$ | See state diagram | | 25 | **40** | ms |
| Output Turn-On Delay | $t_{ON}$ | From rising edge EN, with $V_{IN}$ pre-applied; see timing diagram | | 200 | | µs |
| Output Turn-Off Delay | $t_{OFF}$ | From falling edge EN; see timing diagram | | | **600** | µs |
| Soft Start Ramp Time | $t_{SS}$ | At full rated resistive load; Typical spec is 1-up with minimum $C_{OUT-EXT}$; Max spec is for arrays with max $C_{OUT-EXT}$ | | 30 | **60** | ms |
| Output Voltage Threshold for Max Rated Load Current | $V_{OUT-FL-THRESH}$ | During start up, $V_{OUT}$ must achieve this threshold before output can support full rated current | | | **2.5** | V |
| Output Current at Start Up | $I_{OUT-START}$ | Max load current at start up while $V_{OUT}$ is below $V_{OUT-FL\_THRESH}$ | **1.20** | | | A |
| Monotonic Soft-Start Threshold Voltage | $V_{OUT-MONOTONIC}$ | Output voltage rise becomes monotonic with 10% of preload once it crosses $V_{OUT-MONOTONIC}$ | | | **2.5** | V |
| Minimum Required Disabled Duration | $t_{OFF-MIN}$ | This refers to the minimum time a module needs to be in the disabled state before it will attempt to start via EN | | | **2** | ms |
| Minimum Required Disabled Duration for Predictable Restart | $t_{OFF-MONOTONIC}$ | This refers to the minimum time a module needs to be in the disabled state before it is guaranteed to exhibit monotonic soft-start and have predictable start-up timing | | | **100** | ms |
| Voltage Deviation (Transient) | $\%V_{OUT-TRANS}$ | Minimum $C_{OUT\_EXT}$ (10 ↔ 90% load step), excluding load line | | <10 | | % |
| Settling Time | $t_{SETTLE}$ | | | 8.0 | | ms |
| | | | | | | |
| **Powertrain Protections** | | | | | | |
| Input Voltage Initialization Threshold | $V_{IN-INIT}$ | Threshold to start $t_{INIT}$ delay | | | **9** | V |
| Input Voltage Reset Threshold | $V_{IN-RESET}$ | Latching faults will clear once $V_{IN}$ falls below $V_{IN-RESET}$ | **3** | | | V |
| Input Undervoltage Lockout Threshold | $V_{IN-UVLO–}$ | | **25.80** | | **40.85** | V |
| Input Undervoltage Recovery Threshold | $V_{IN-UVLO+}$ | See timing diagram | | | **43.00** | V |
| Input Overvoltage Lockout Threshold | $V_{IN-OVLO+}$ | | | | **171** | V |
| Input Overvoltage Recovery Threshold | $V_{IN-OVLO–}$ | See timing diagram | **154** | | | V |
| Output Overvoltage Threshold | $V_{OUT-OVP}$ | From 25 to 100% load; latched shut down | **6.33** | | | V |
| | $V_{OUT-OVP-LL}$ | From 0 to 25% load; latched shut down | **6.60** | | | V |
| Minimum Current-Limited Output Voltage | $V_{OUT-UVP}$ | Over all operating steady-state line and trim conditions | | | **2.25** | V |
| Overtemperature Threshold (Internal) | $T_{INT-OTP}$ | | **125** | | | °C |
| Power Limit | $P_{LIM}$ | | | | **110** | W |
| Input Voltage Overvoltage to Cessation of Powertrain Switching | $t_{OVLO-SW}$ | Independent of fault logic | | 3.2 | | µs |
| Input Voltage Overvoltage Response Time | $t_{OVLO}$ | For fault logic only | | | **200** | µs |
| Input Voltage Undervoltage Response Time | $t_{UVLO}$ | | | | **100** | ms |
| Short Circuit Response Time | $t_{SC}$ | Powertrain on, operational state | | | **200** | µs |
| Short Circuit, or Temperature Fault Recovery Time | $t_{FAULT}$ | See timing diagram | | 1 | | s |

## Common Electrical Specifications for Array and Enhanced $V_{OUT}$ Regulation Operation (Cont.)

Specifications apply over all line, trim and load conditions, internal temperature $T_{INT}$ = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C < $T_{INT}$ < 125°C for T-Grade and –55°C < $T_{INT}$ < 125°C for M-Grade.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Trim: TR** | | | | | | |
| TR Trim Disable Threshold | $V_{TRIM-DIS-TH}$ | Trim disabled when TR above this threshold at power up | | | **3.20** | V |
| TR Trim Enable Threshold | $V_{TRIM-EN-TH}$ | Trim enabled when TR below this threshold at power up | **3.15** | | | V |
| Internally Generated $V_{CC}$ | $V_{CC}$ | | **3.21** | 3.30 | **3.39** | V |
| TR Pin Functional Range | $V_{TRIM-EN}$ | | 0.00 | 2.33 | 3.16 | V |
| $V_{OUT}$ Referred TR Pin Resolution | $V_{OUT-RES}$ | With $V_{CC}$ = 3.3V | | 6 | | mV |
| TR Internal Pull-Up Resistance to $V_{CC}$ | $R_{TRIM-INT}$ | | **9.9** | 10.0 | **10.1** | kΩ |
| | | | | | | |
| **Enable: EN** | | | | | | |
| EN Enable Threshold | $V_{ENABLE-EN-TH}$ | | | | **2.31** | V |
| EN Disable Threshold | $V_{ENABLE-DIS-TH}$ | | **0.99** | | | V |
| Internally Generated $V_{CC}$ | $V_{CC}$ | | **3.21** | 3.30 | **3.39** | V |
| EN internal Pull-Up Resistance to $V_{CC}$ | $R_{ENABLE-INT}$ | | **9.9** | 10.0 | **10.1** | kΩ |
| Array Mode Enable Threshold | $V_{ARRAY-EN-TH}$ | | **2.97** | | | V |
| Enhanced $V_{OUT}$ Regulation Mode Enable Threshold | $V_{REG-EN-TH}$ | | | | **2.63** | V |
| | | | | | | |
| **Fault: FT** | | | | | | |
| FT Internal Pull-Up Resistance to $V_{CC}$ | $R_{FAULT-INT}$ | | **494** | 499 | **504** | kΩ |
| FT Voltage | $V_{FAULT-ACTIVE}$ | At rated current drive capability | **3.0** | | | V |
| FT Current Drive Capability | $I_{FAULT-ACTIVE}$ | Overload beyond the ABSOLUTE MAXIMUM ratings may cause module damage | **4** | | | mA |
| FT Response Time | $t_{FT-ACTIVE}$ | Delay from cessation of switching to FT Pin Active | | | **200** | µs |

## Electrical Specifications: Array Operation Only

Specifications apply over all line, trim and load conditions, internal temperature $T_{INT}$ = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C < $T_{INT}$ < 125°C for T-Grade and –55°C < $T_{INT}$ < 125°C for M-Grade.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Power Output Specifications** | | | | | | |
| Output Voltage Load Regulation | $\Delta V_{OUT-LOAD}$ | Linear load line. Output voltage increase from full rated load current to no load (does not include light-load regulation). See Figure 6 and Design Guidelines section | 0.2356 | 0.2632 | 0.2910 | V |
| Output Voltage Light-Load Regulation | $\Delta V_{OUT-LL}$ | 0 – 10% load, additional $V_{OUT}$, relative to calculated load-line point; see Design Guidelines section | **-0.08** | | **0.53** | V |
| Output Voltage Temperature Coefficient | $\Delta V_{OUT-TEMP}$ | Nominal, linear temperature coefficient, relative to $T_{INT}$ = 25°C; see Figure 20 and Design Guidelines Section | | **-0.67** | | mV / °C |
| Output Voltage Accuracy | $\%V_{OUT-ACCURACY}$ | The total output voltage set-point accuracy from the calculated ideal $V_{OUT}$ based on load, temp and trim. Excludes $\Delta V_{OUT-LL}$ | **-3.0** | | **3.0** | % |

## Electrical Specifications: Enhanced $V_{OUT}$ Operation Only

Specifications apply over all line, trim and load conditions, internal temperature $T_{INT}$ = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C < $T_{INT}$ < 125°C for T-Grade and –55°C < $T_{INT}$ < 125°C for M-Grade.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Power Output Specifications** | | | | | | |
| Output Voltage Load Regulation | $\Delta V_{OUT-REGULATION}$ | Nominal line, nominal trim, full load and ambient temperature | -0.8 | | 0.8 | % |
| | | Nominal line, nominal trim and:<br>• Load >20% of full load and ambient temperature<br>• Full load and over temperature | -1.5 | | 1.5 | |
| | | All other conditions (does not include light-load regulation) | -2.5 | | 2.5 | |
| Output Voltage Accuracy | $\%V_{OUT-ACCURACY}$ | The total output voltage set-point accuracy from the calculated $V_{OUT}$ based on load, temperature and trim; Excludes:<br>• $\Delta V_{OUT-LL}$<br>• $\%V_{OUT-REGULATION}$ | **-3.0** | | **3.0** | % |
| Output Voltage Light-Load Regulation | $\Delta V_{OUT-LL}$ | 0 – 10% load, additional $V_{OUT}$, relative to $V_{OUT}$ accuracy; see Design Guidelines section | **-0.08** | | **0.53** | V |

## Specified Operating Area

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device. Electrical specifications do not apply when operating beyond rated operating conditions.

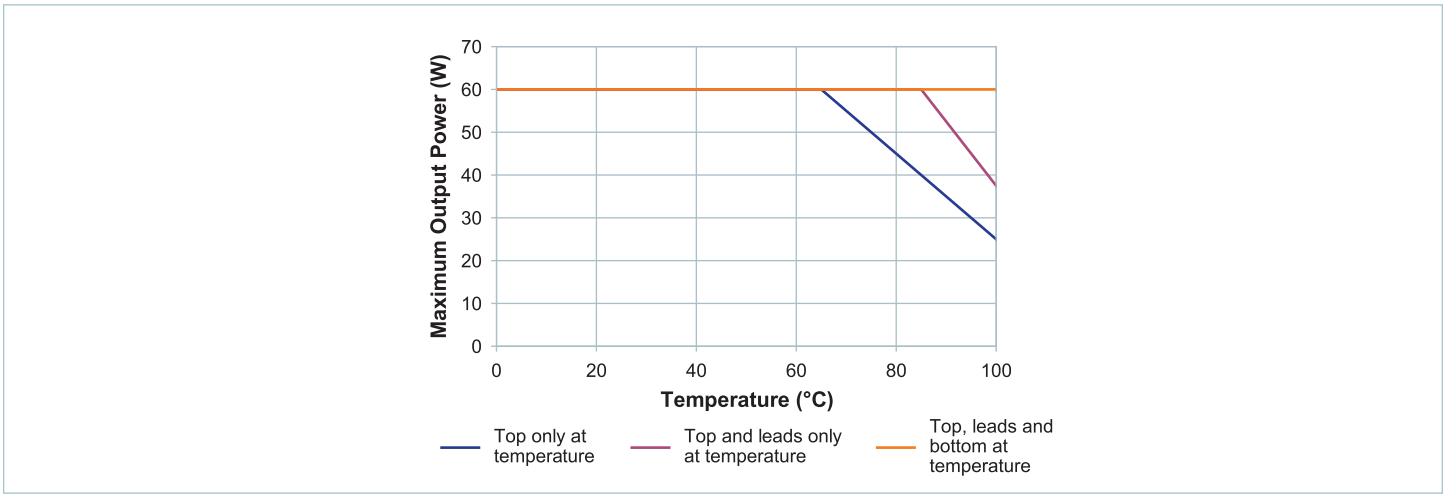



***Figure 1 —*** *Thermal specified operating area: max output power vs. case temperature, single unit at minimum full-load efficiency*

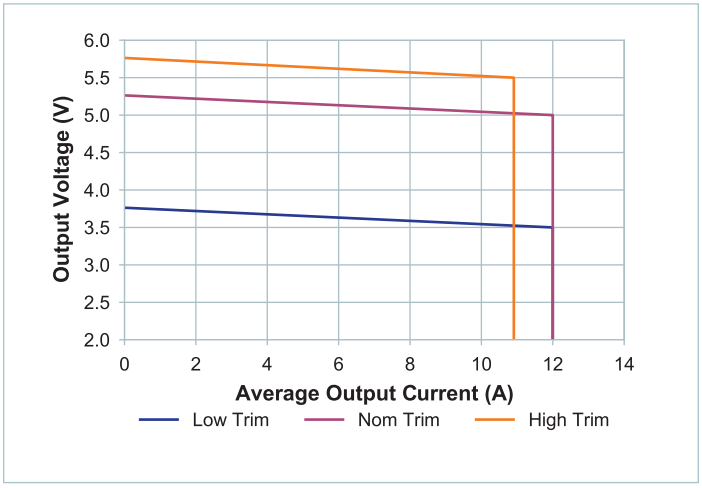



***Figure 2 —*** *Electrical specified operating area: Array Mode*

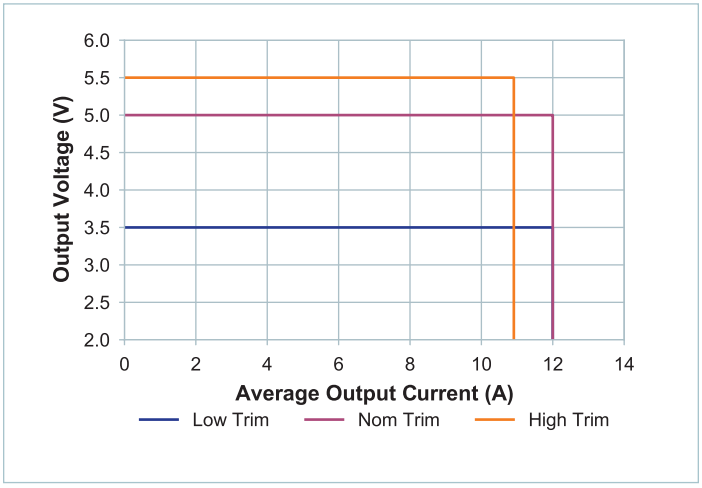
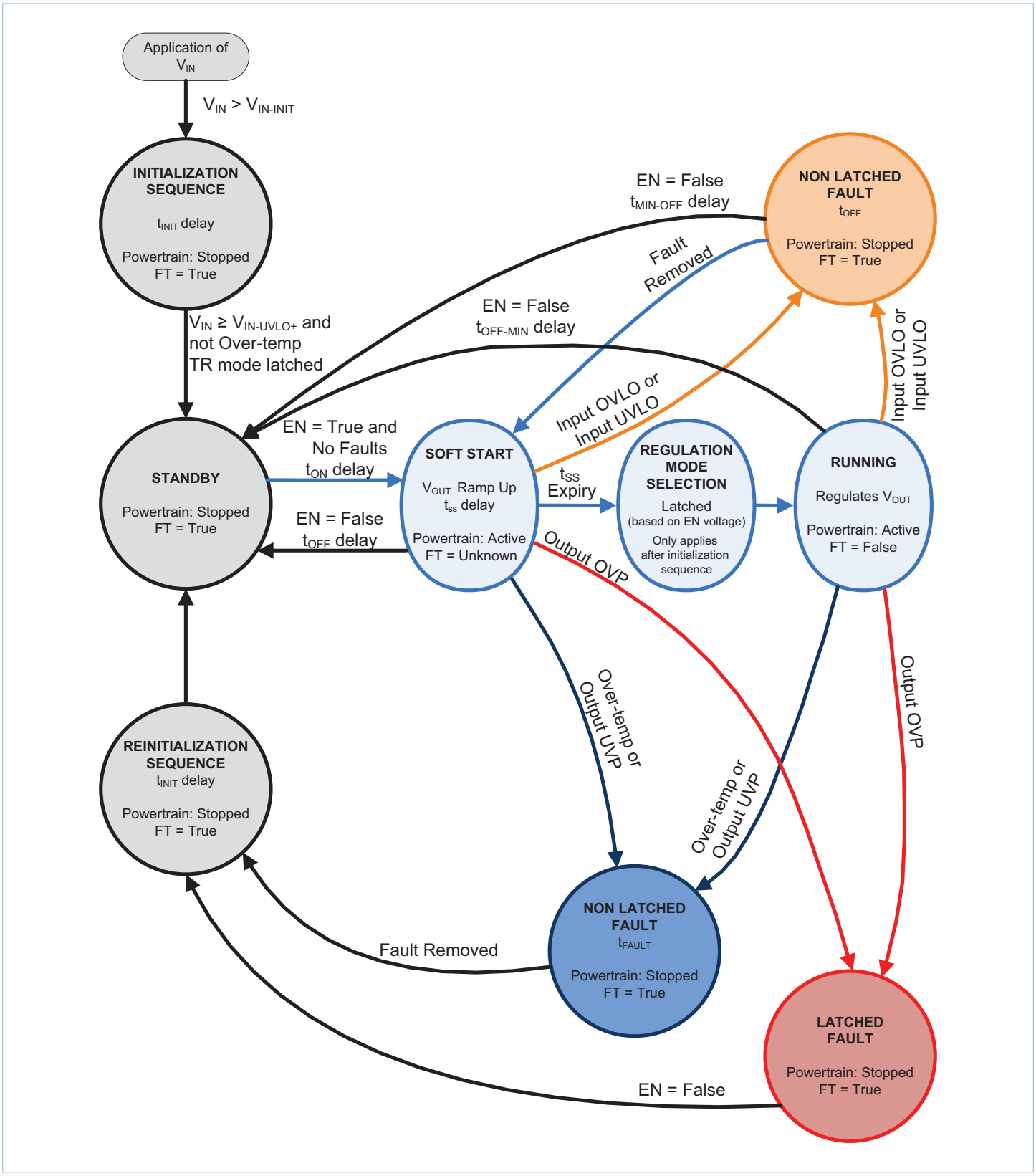



***Figure 3 —*** *Electrical specified operating area; Enhanced $V_{OUT}$ Regulation Mode*

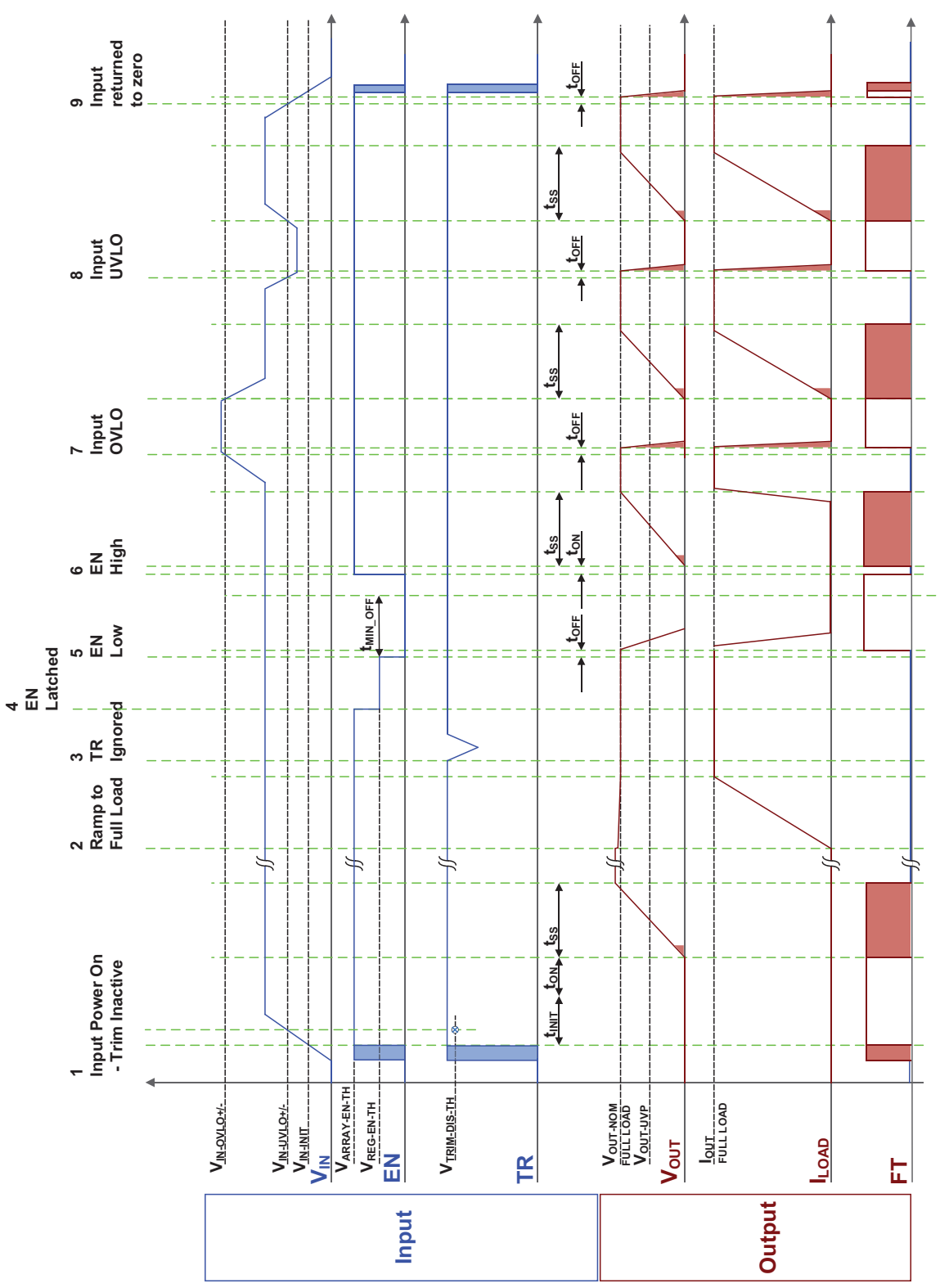
## High-Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



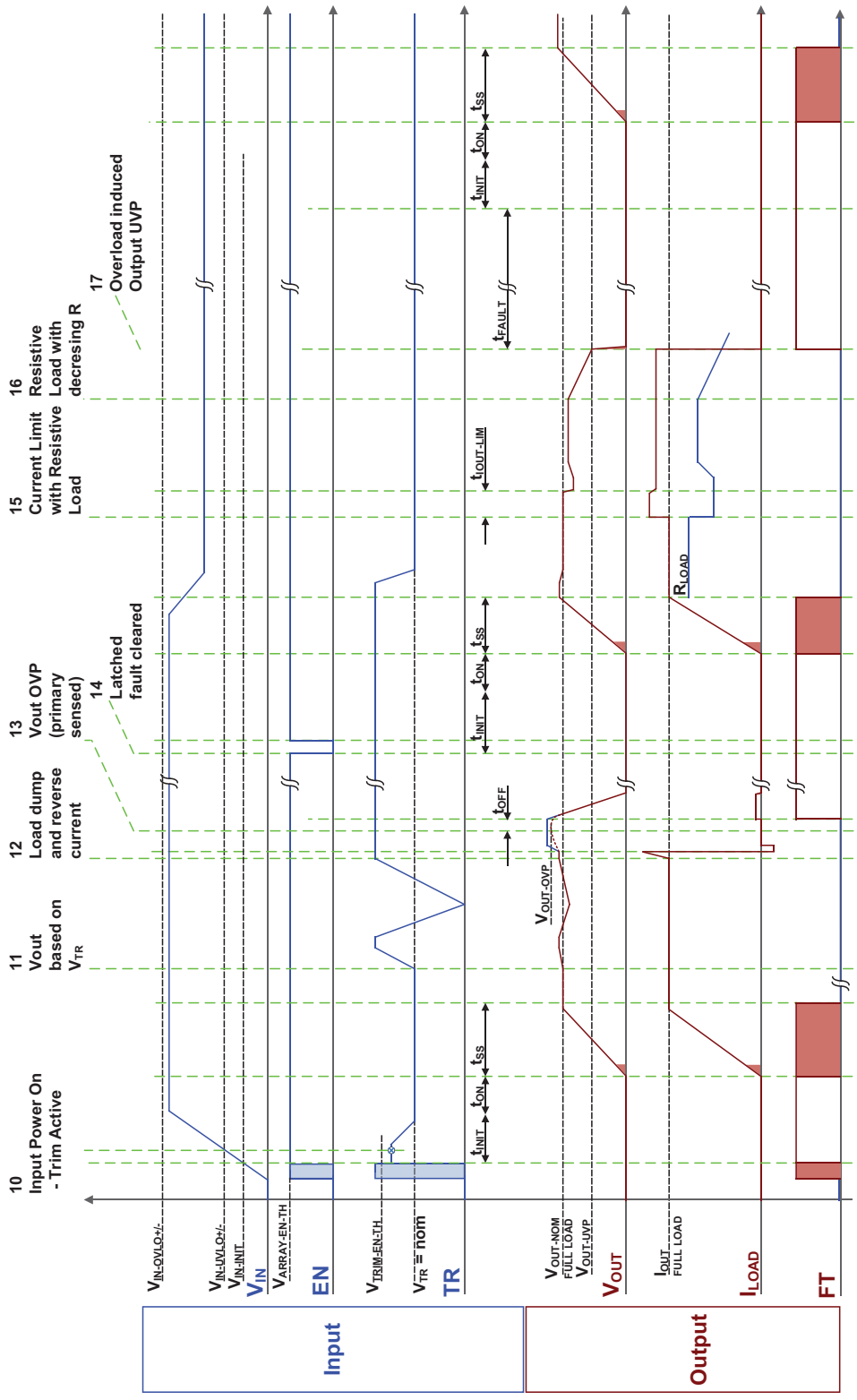
## Timing Diagrams – Array Mode

Module inputs are shown in blue; module outputs are shown in brown.



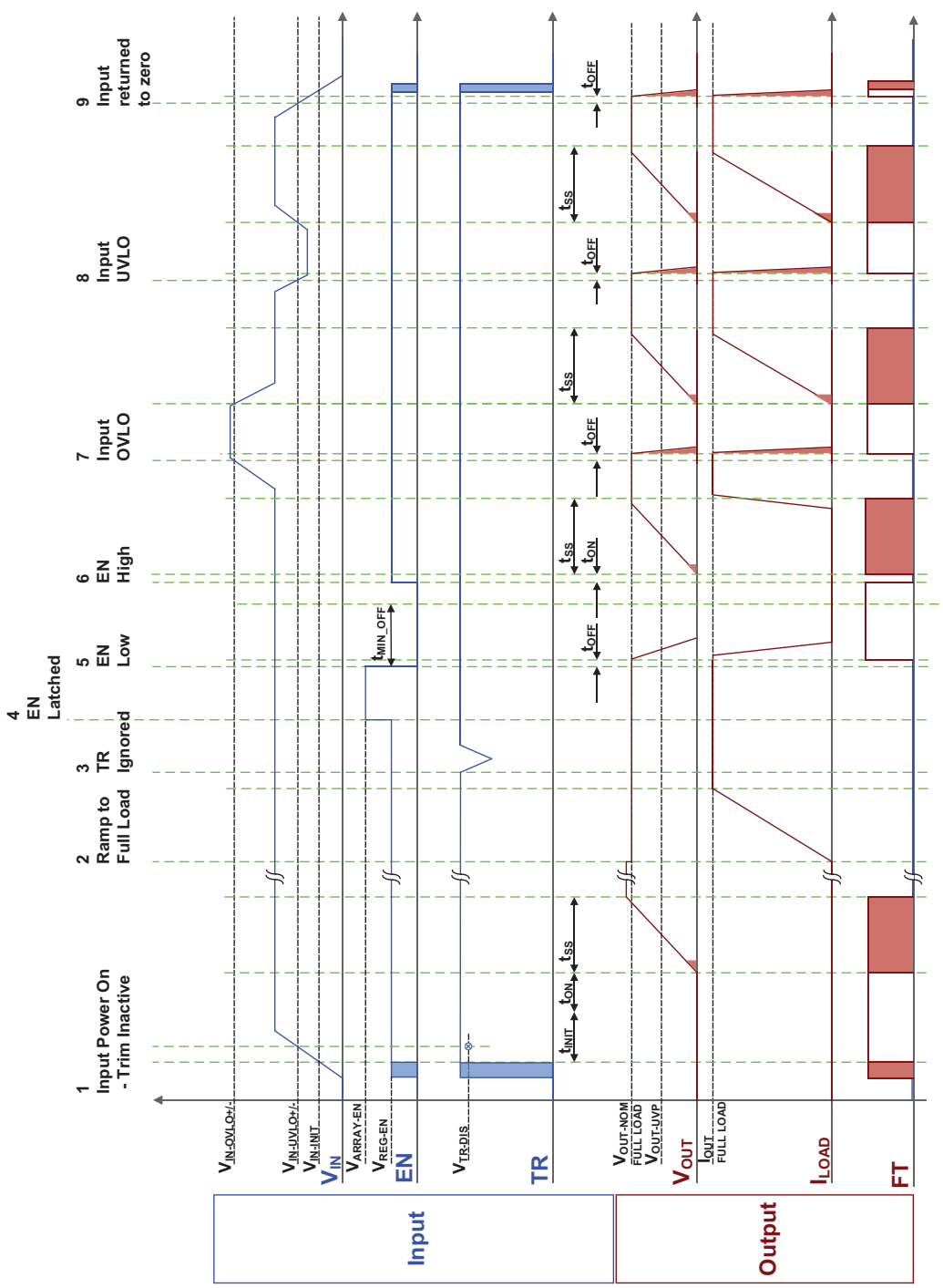
## Timing Diagrams – Array Mode (Cont.)

Module inputs are shown in blue; module outputs are shown in brown.



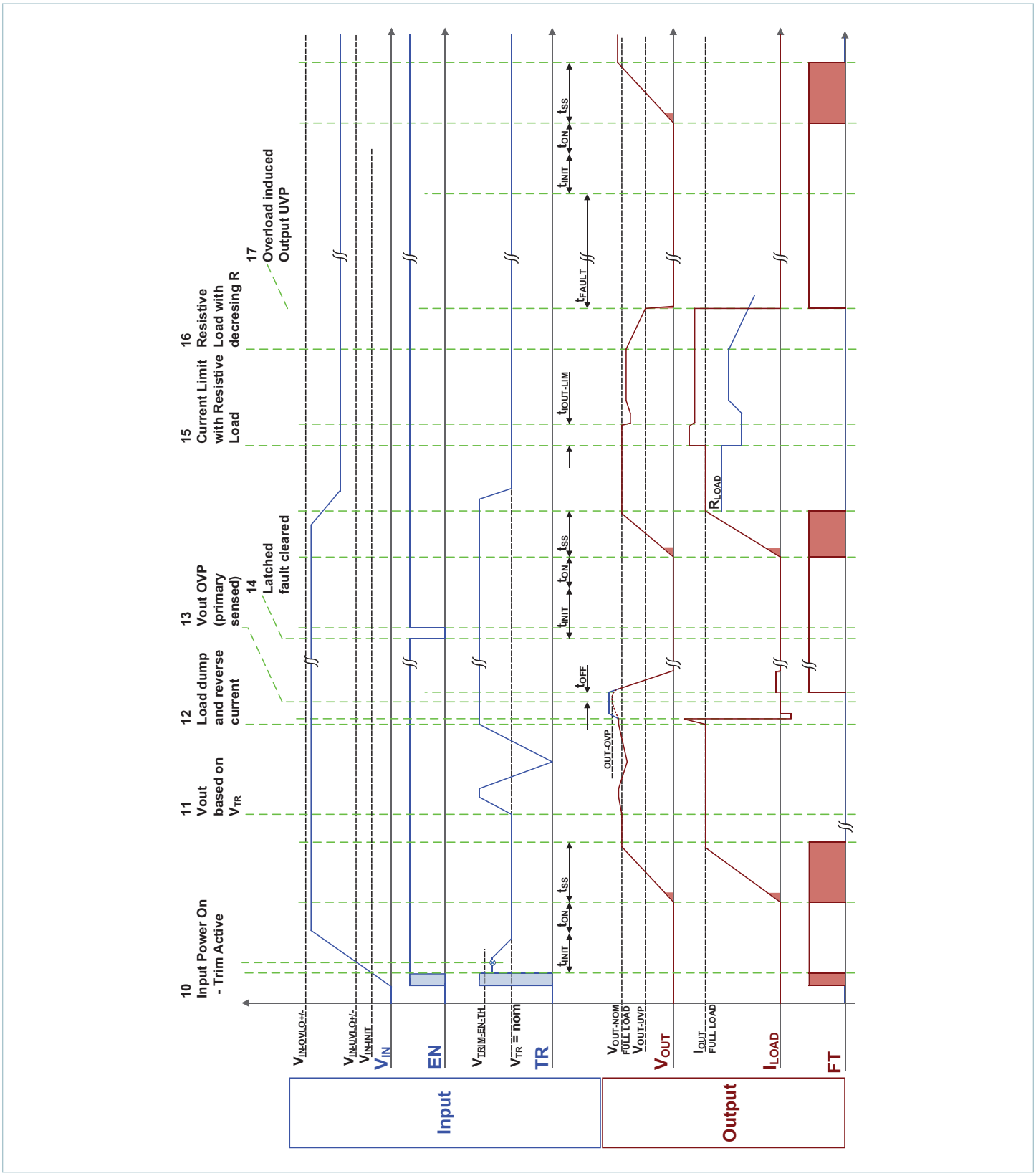
## Timing Diagrams – Enhanced $V_{OUT}$ Regulation Mode

Module inputs are shown in blue; module outputs are shown in brown.



## Timing Diagrams – Enhanced $V_{OUT}$ Regulation Mode (Cont.)

Module inputs are shown in blue; module outputs are shown in brown.



## Common Typical Performance Characteristics for Array and Enhanced $V_{OUT}$ Regulation Operation

The following figures present typical performance at $T_C$ = 25°C, unless otherwise noted. See associated figures for general trend data.

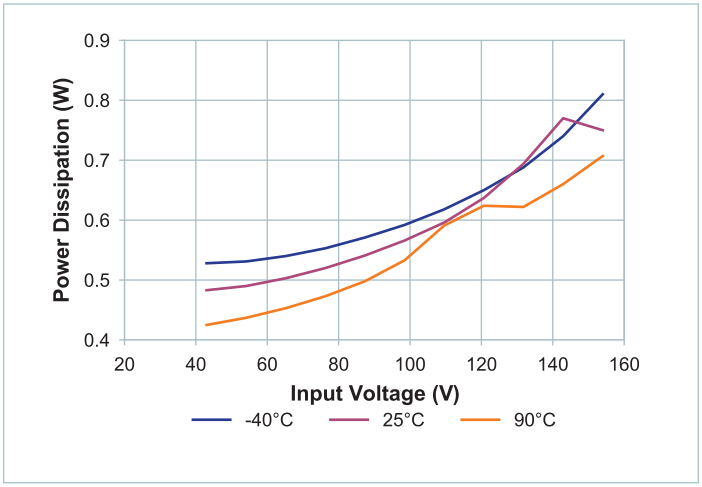



***Figure 4 —*** *Disabled power dissipation vs. $V_{IN}$*

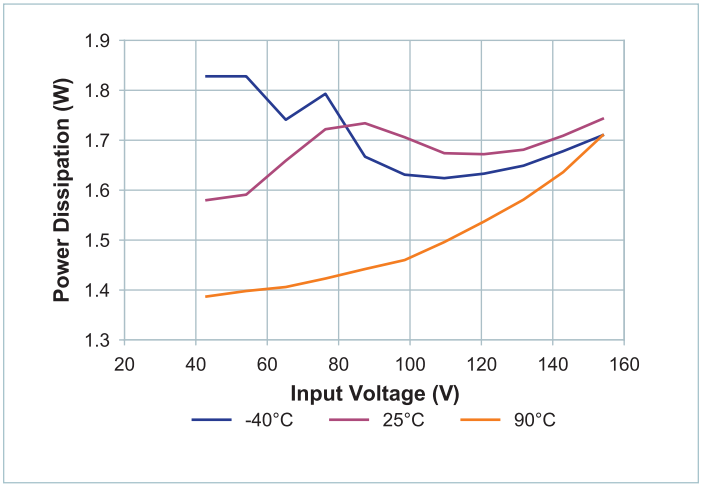



***Figure 5 —*** *No-load power dissipation vs. $V_{IN}$, at nominal trim*

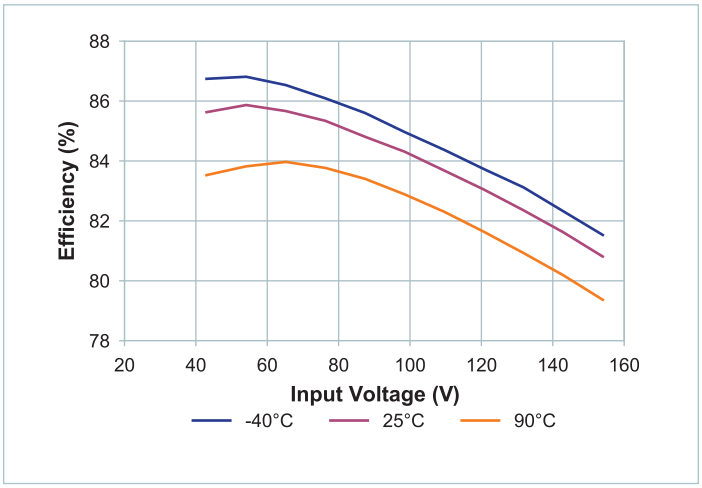



***Figure 6 —*** *Full-load efficiency vs. $V_{IN}$, at low trim*

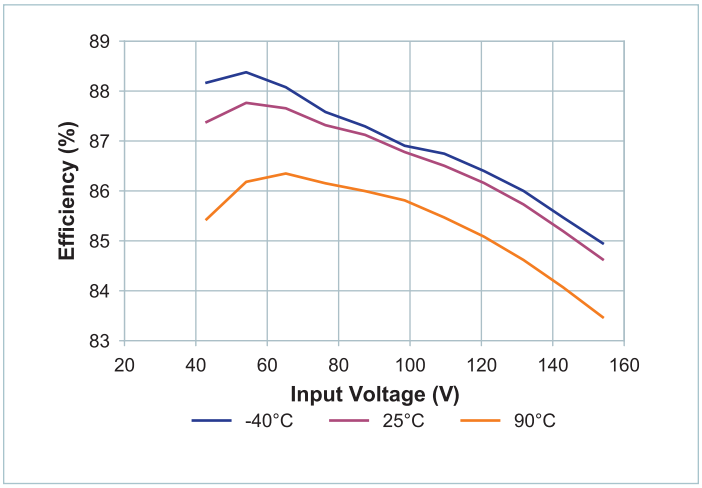



***Figure 7 —*** *Full-load efficiency vs. $V_{IN}$, at nominal trim*

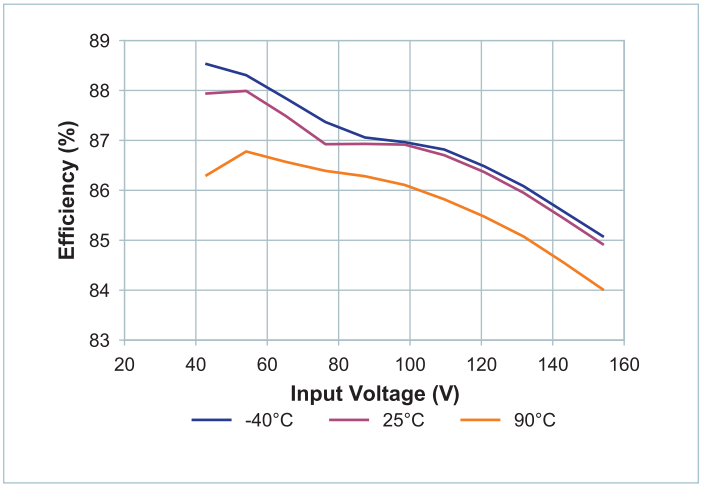



***Figure 8 —*** *Full-load efficiency vs. $V_{IN}$, at high trim*

## Common Typical Performance Characteristics for Array and Enhanced $V_{OUT}$ Regulation Operation (Cont.)

The following figures present typical performance at $T_C$ = 25°C, unless otherwise noted. See associated figures for general trend data.

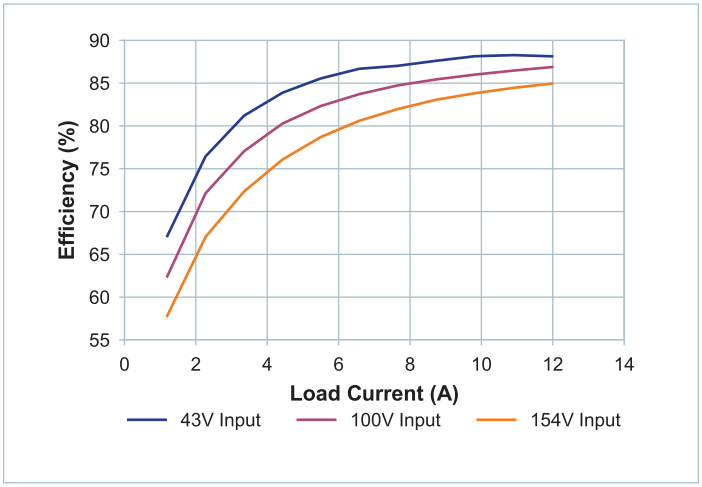



***Figure 9 —*** *Efficiency vs. load at $T_{CASE}$ = -40°C, nominal trim*

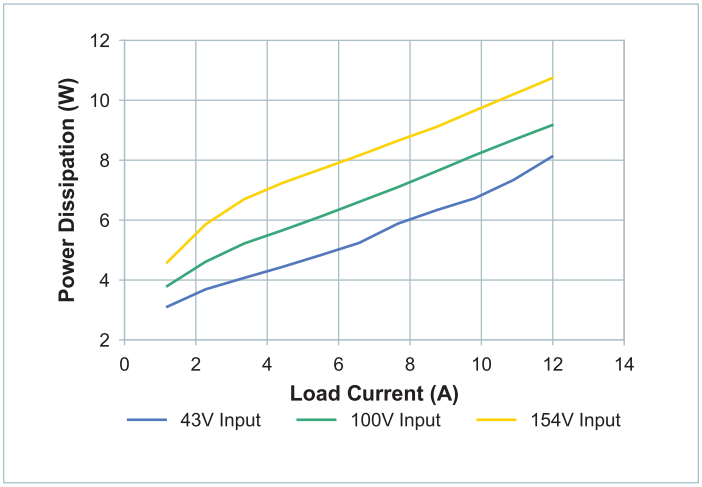



***Figure 10 —*** *Power dissipation vs. load at $T_{CASE}$ = -40°C, nominal trim*

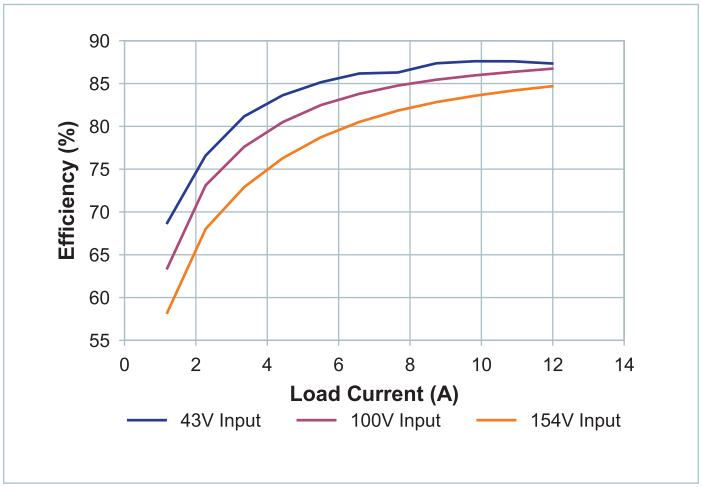



***Figure 11 —*** *Efficiency vs. load at $T_{CASE}$ = 25°C, nominal trim*

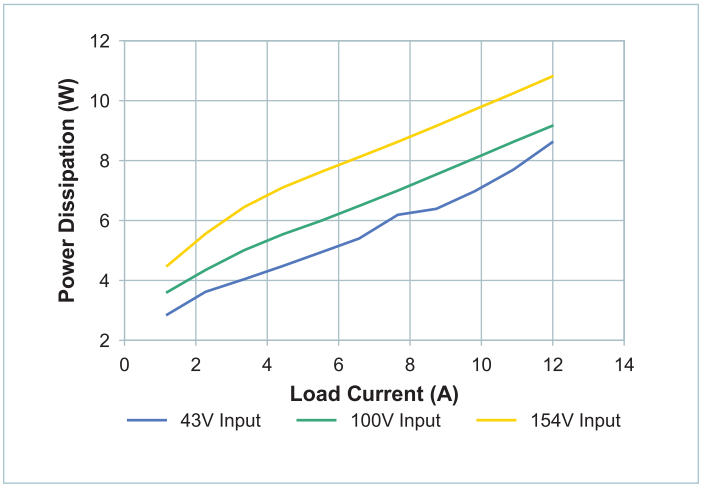



***Figure 12 —*** *Power dissipation vs. load at $T_{CASE}$ = 25°C, nominal trim*

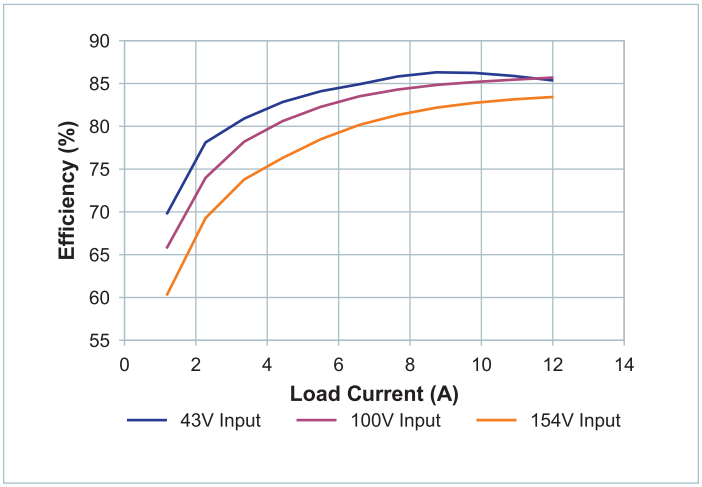



***Figure 13 —*** *Efficiency vs. load at $T_{CASE}$ = 90°C, nominal trim*

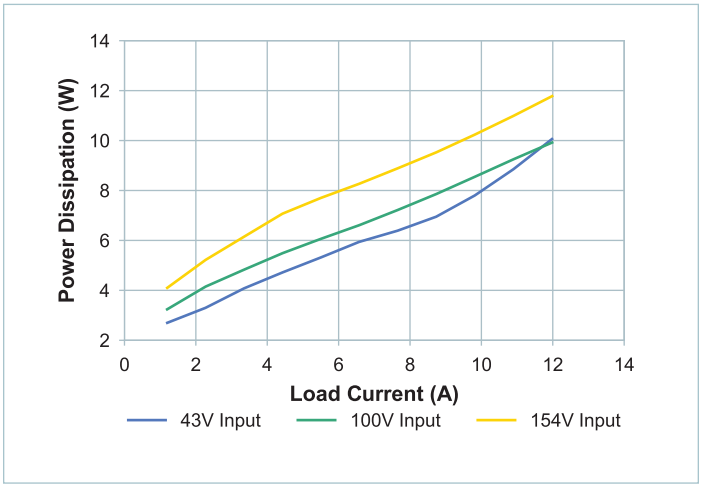



***Figure 14 —*** *Power dissipation vs. load at $T_{CASE}$ = 90°C, nominal trim*

## Common Typical Performance Characteristics for Array and Enhanced $V_{OUT}$ Regulation Operation (Cont.)

The following figures present typical performance at $T_C$ = 25°C, unless otherwise noted. See associated figures for general trend data.

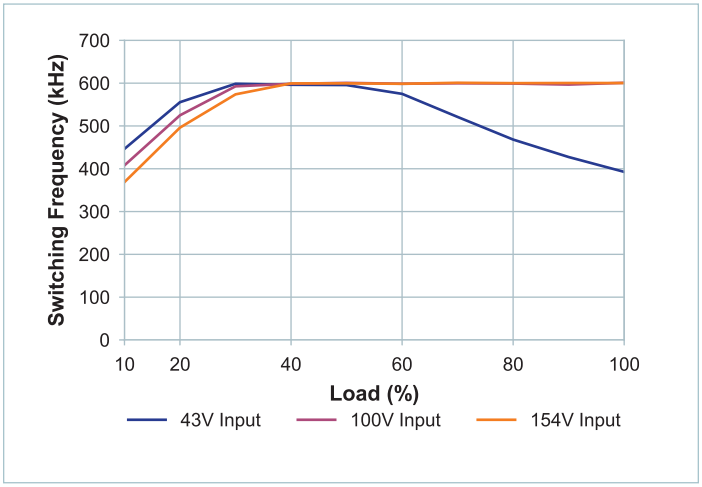



***Figure 15 —*** *Nominal powertrain switching frequency vs. load at nominal trim*

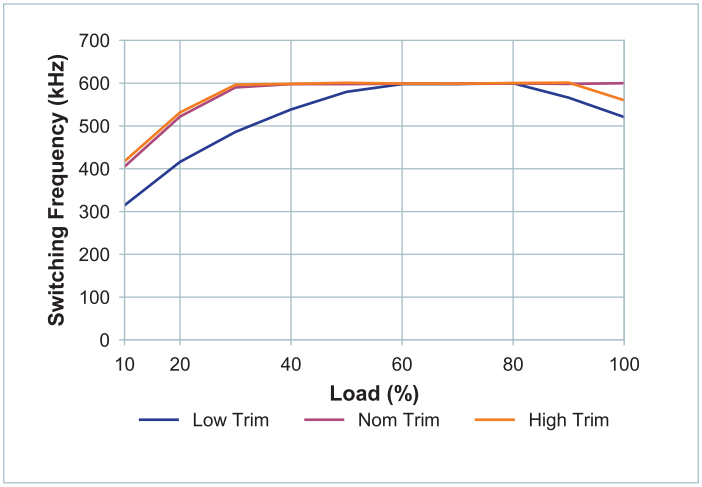



***Figure 16 —*** *Nominal powertrain switching frequency vs. load at nominal $V_{IN}$*

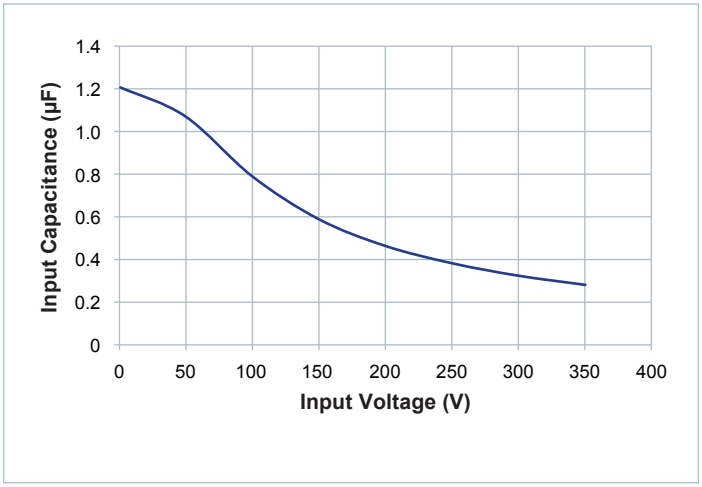



***Figure 17 —*** *Effective internal input capacitance vs. applied voltage*

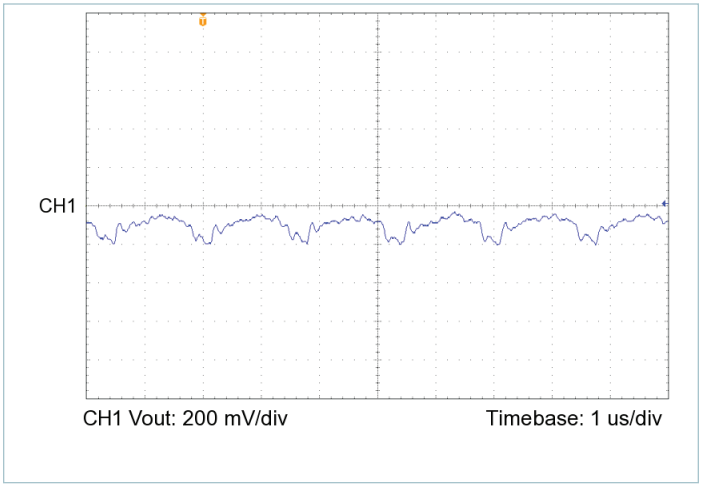



***Figure 18 —*** *Output voltage ripple, $V_{IN}$ = 100V, $V_{OUT}$ = 5.0V, $C_{OUT\_EXT}$ = 470µF, $R_{LOAD}$ = 0.417Ω*

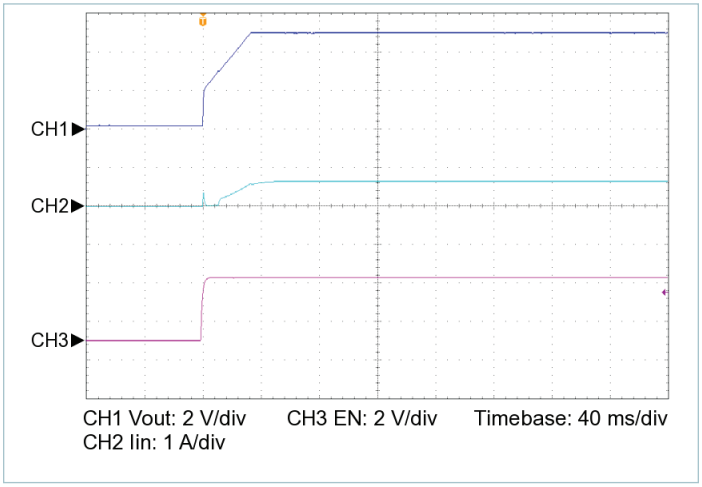



***Figure 19 —*** *Start up from EN, $V_{IN}$ = 100V, $C_{OUT\_EXT}$ = 10000µF, $R_{LOAD}$ = 0.417Ω*

## Typical Performance Characteristics: Array Operation Only

The following figures present typical performance at $T_C$ = 25°C, unless otherwise noted. See associated figures for general trend data.

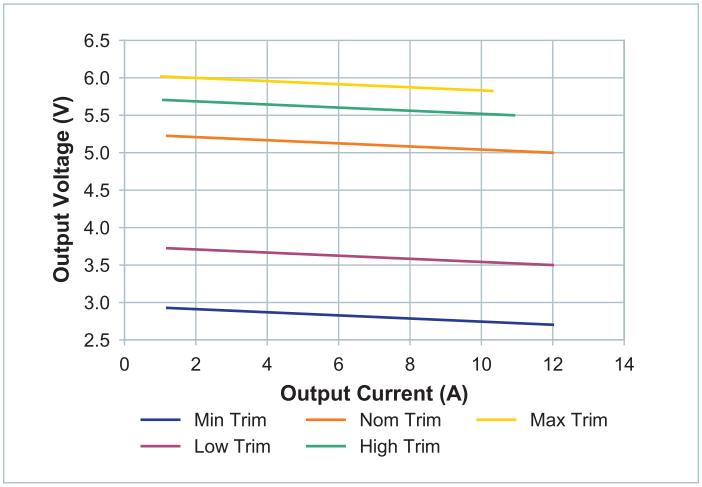



***Figure 20 —*** *Ideal $V_{OUT}$ vs. load current, at 25°C case*

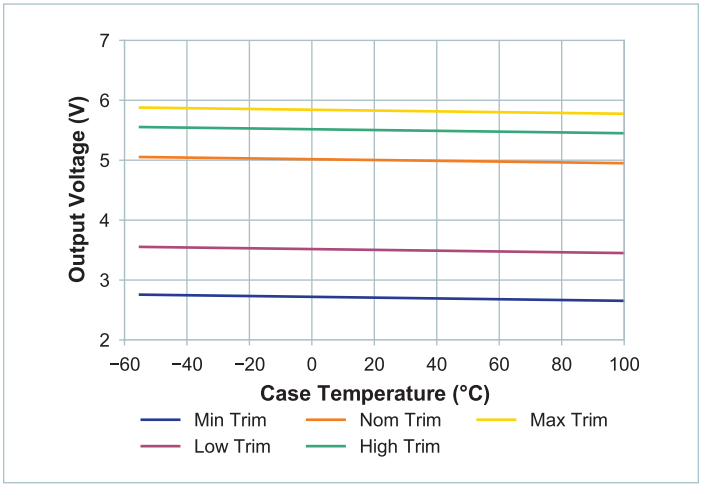



***Figure 21 —*** *Ideal $V_{OUT}$ vs. case temperature, at full load*

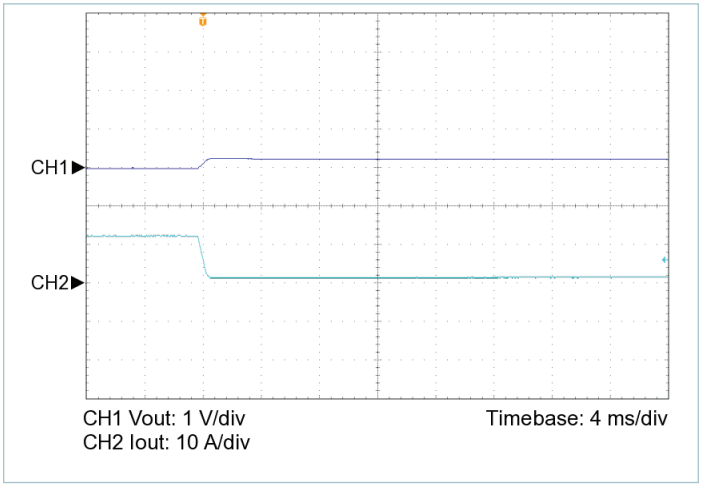



***Figure 22 —*** *100 – 10% load transient response, $V_{IN}$ = 100V, nominal trim, $C_{OUT\_EXT}$ = 470µF*

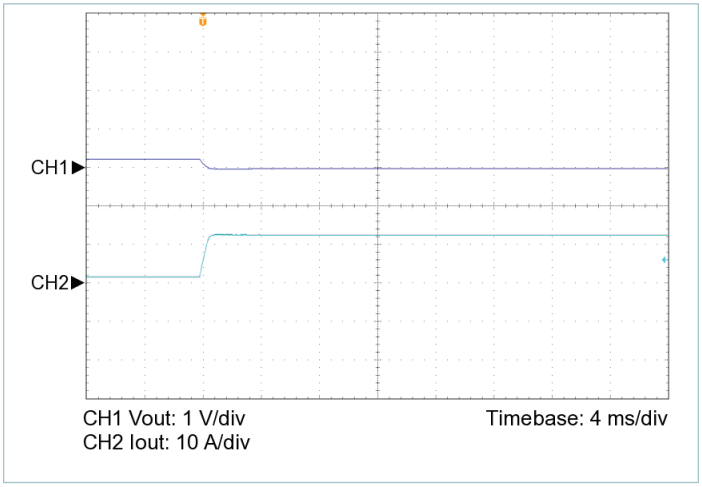



***Figure 23 —*** *10 – 100% load transient response, $V_{IN}$ = 100V, nominal trim, $C_{OUT\_EXT}$ = 470µF*

## Typical Performance Characteristics: Enhanced $V_{OUT}$ Regulation Operation Only

The following figures present typical performance at $T_C$ = 25°C, unless otherwise noted. See associated figures for general trend data.

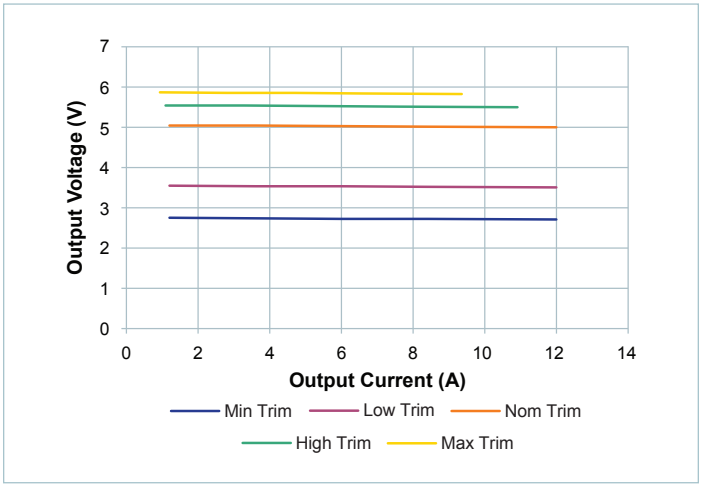



***Figure 24 —*** *Ideal $V_{OUT}$ vs. load current, at 25°C case, operating in Enhanced $V_{OUT}$ Regulation Mode*

## Pin Functions

### +IN, –IN

Input power pins. –IN is the reference for all control pins, and therefore a Kelvin connection for the control signals is recommended as close as possible to the pin on the package, to reduce effects of voltage drop due to –IN currents.

### +OUT, –OUT

Output power pins.

### EN (Enable)

The EN pin provides two functionalities:

- Enables and disables the DCM converter.
- Selects Array mode or Enhanced $V_{OUT}$ Regulation Mode.

The EN pin is referenced to the –IN pin of the converter. It has an internal pull-up to $V_{CC}$ through a 10kΩ resistor.

EN is an input only, it does not pull low in the event of a fault.

#### *Enable/Disable Control*

- Output disable: when EN is pulled down externally below the disable threshold ($V_{ENABLE-DIS-TH}$), the DCM converter will be disabled.
- Output enable: when EN is allowed to pull up above the enable threshold ($V_{ENABLE-EN-TH}$) through the internal pull-up to $V_{CC}$, the DCM converter will be enabled.

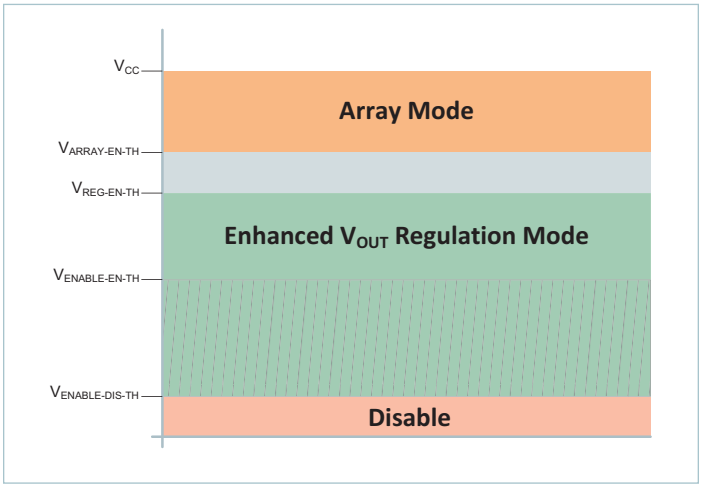



***Figure 25 —*** *EN pin voltage thresholds*

#### *Selecting Array Mode or Enhanced $V_{OUT}$ Regulation Mode*

The EN pin can also be used to select Array mode operation or Enhanced $V_{OUT}$ Regulation Mode operation. The DCM mode of operation is dependent on the voltage seen by the DCM at its EN pin at first start up following application of $V_{IN}$. The DCM will latch in selected mode of operation at the end of soft start and persist in that same mode until loss of input voltage.

At the first start up after application of $V_{IN}$, if EN is allowed to float to:

- A value above $V_{ENABLE-EN-TH}$ but below $V_{REG-EN-TH}$, the DCM will implement Enhanced $V_{OUT}$ Regulation Mode.
- A value above $V_{ARRAY-EN-TH}$ and up to $V_{CC}$, the DCM will implement array mode operation.

Note that the selected mode of operation is not changed when a DCM recovers from any fault condition, or after a disable event through EN. The operation mode is reset only with cycling of input power.

### TR (Trim)

The TR pin is used to select the trim mode and to trim the output voltage of the DCM converter. The TR pin has an internal pull-up to $V_{CC}$ through a 10.0kΩ resistor.

The DCM will latch trim behavior at application of $V_{IN}$ (once $V_{IN}$ exceeds $V_{IN-UVLO+}$) and persist in that same behavior until loss of input voltage

- At application of $V_{IN}$, if TR is sampled at above $V_{TRIM-DIS-TH}$, the module will latch in a non-trim mode, and will ignore the TR input for as long as $V_{IN}$ is present.
- At application of $V_{IN}$, if TR is sampled at below $V_{TRIM-EN-TH}$, the TR will serve as an input to control the real time output voltage, relative to full load, 25°C. It will persist in this behavior until $V_{IN}$ is no longer present.

If trim is active when the DCM is operating, the TR pin provides dynamic trim control at a typical 30Hz of –3dB bandwidth over the output voltage. TR also decreases the current limit threshold when trimming above $V_{OUT-NOM}$.

### FT (Fault)

The FT pin provides a Fault signal.

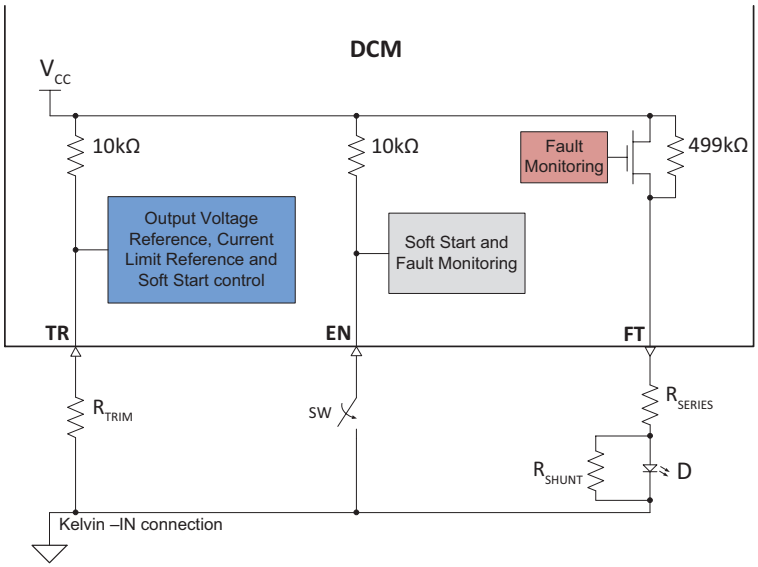
Any time the module is enabled and has not recognized a fault, the FT pin is inactive. FT has an internal 499kΩ pull-up to $V_{CC}$, therefore a shunt resistor, $R_{SHUNT}$, of approximately 50kΩ can be used to ensure the LED is completely off when there is no fault, per the diagram below.

Whenever the powertrain stops (due to a fault protection or disabling the module by pulling EN low), the FT pin becomes active and provides current to drive an external circuit.

When active, FT pin drives to $V_{CC}$, with up to 4mA of external loading. Module may be damaged from an overcurrent FT drive, thus a resistor in series for current limiting is recommended.

The FT pin becomes active momentarily when the module starts up.

## Typical External Circuits for Signal Pins (TR, EN, FT)




## Design Guidelines

### Building Blocks and System Design

The DCM converter input accepts the full 43 – 154V range, and it generates an isolated trimmable 5.0$V_{DC}$ output. Multiple DCMs may be paralleled for higher power capacity via wireless load sharing, even when they are operating off of different input voltage supplies.

The DCM converter provides a regulated output voltage around defined nominal load line and temperature coefficients. The load line and temperature coefficients enable configuration of an array of DCM converters which manage the output load with no share bus among modules. Downstream regulators may be used to provide tighter voltage regulation, if required.

The DCM2322xA5N0660y6z may be used in standalone applications where the output power requirements are up to 60W. However, it is easily deployed as arrays of modules to increase power handling capacity. Arrays of up to eight units have been qualified for 480W capacity. Application of DCM converters in an array requires no de-rating of the maximum available power versus what is specified for a single module.

**Note:** For more information on operation of single DCM, refer to "Single DCM as an Isolated, Regulated DC-DC Converter" application note AN:029.

### Soft Start

When the DCM starts, it will go through a soft start. The soft-start routine ramps the output voltage by modulating the internal error amplifier reference. This causes the output voltage to approximate a piecewise linear ramp. The output ramp finishes when the voltage reaches either the nominal output voltage, or the trimmed output voltage in cases where trim mode is active.

During soft start, the maximum load current capability is reduced. Until $V_{OUT}$ achieves at least $V_{OUT\text{-}FL\text{-}THRESH}$, the output current must be less than $I_{OUT\text{-}START}$ in order to guarantee start up. Note that this is current available to the load, above that which is required to charge the output capacitor.

### Nominal Output Voltage Load Line

*DCM in Array Mode*

Throughout this document, the programmed output voltage (either the specified nominal output voltage if trim is inactive or the trimmed output voltage if trim is active), is specified at full load and at room temperature. The actual output voltage of the DCM is given by the programmed trimmed output voltage, with modification based on load and temperature. The nominal output voltage is 5.0V, and the actual output voltage will match this at full load and room temperature with trim inactive.

The largest modification to the actual output voltage compared to the programmed output is due to the 5.263% $V_{OUT\text{-}NOM}$ load line, which for this model corresponds to $\Delta V_{OUT\text{-}LOAD}$ of 0.2632V. As the load is reduced, the internal error amplifier reference, and by extension the output voltage, rises in response. This load line is the primary enabler of the wireless current sharing among an array of DCMs.

The load line impact on the output voltage is absolute, and does not scale with programmed trim voltage.

For a given programmed output voltage, the actual output voltage versus load current at nominal trim and room temperature is given by the following equation:

$$V_{OUT}\,at\,25°C = 5.0 + 0.2632 \bullet (1 - I_{OUT} / 12.00) \qquad (1)$$

*DCM in Enhanced $V_{OUT}$ Regulation Mode*

In Enhanced $V_{OUT}$ Regulation Mode, output voltage is not a function of load line.

### Nominal Output Voltage Temperature Coefficient

*DCM in Array Mode*

A second additive term to the programmed output voltage is based on the temperature of the module. This term permits improved thermal balancing among modules in an array, especially when the factory nominal trim point is utilized (trim mode inactive). This term is much smaller than the load line described above, representing only a -0.67mV/°C change. Regulation coefficient is relative to 25°C.

For nominal trim and full load, the output voltage relates to the temperature according to the following equation:

$$V_{OUT\text{-}FL} = 5.0 - 0.667 \bullet 0.001 \bullet (T_{INT} - 25) \quad (2)$$

where $T_{INT}$ is in °C.

The impact of temperature coefficient on the output voltage is absolute and does not scale with trim or load.

*DCM in Enhanced $V_{OUT}$ Regulation Mode*

In Enhanced $V_{OUT}$ Regulation Mode, output voltage is not a function of temperature coefficient.

### Trim Mode and Output Trim Control

*DCM in Array and Enhanced $V_{OUT}$ Regulation Modes*

When the input voltage is initially applied to a DCM, and after $t_{INIT}$ elapses, the trim pin voltage $V_{TR}$ is sampled. The TR pin has an internal pull-up resistor to $V_{CC}$, so unless external circuitry pulls the pin voltage lower, it will pull up to $V_{CC}$. If the initially sampled trim pin voltage is higher than $V_{TRIM\text{-}DIS}$, then the DCM will disable trimming as long as the $V_{IN}$ remains applied. In this case, for all subsequent operation the output voltage will be programmed to the nominal. This minimizes the support components required for applications that only require the nominal rated $V_{OUT}$, and also provides the best output set-point accuracy, as there are no additional errors from external trim components.

If at initial application of $V_{IN}$, the TR pin voltage is prevented from exceeding $V_{TRIM\text{-}EN}$, then the DCM will activate trim mode, and it will remain active for as long as $V_{IN}$ is applied.

$V_{OUT}$ set point under full load and room temperature can be calculated using the equation below:

$$V_{OUT\text{-}FL} \text{ at } 25°C = 2.70 + (3.260 \bullet V_{TR} / V_{CC}) \quad (3)$$

Note that the trim mode is not changed when a DCM recovers from any fault condition or being disabled.

Module performance is guaranteed through output voltage trim range $V_{OUT\text{-}TRIMMING}$. If $V_{OUT}$ is trimmed above this range, then certain combinations of line and load transient conditions may trigger the output OVP.

### Overall Output Voltage Transfer Function

*DCM in Array Mode*

Taking load line (Equation 1), temperature coefficient (Equation 2) and trim (Equation 3) into account, the general equation relating the DC $V_{OUT}$ to programmed trim (when active), load and temperature is given by:

$$\begin{aligned} V_{OUT} = {} & 2.70 + (3.260 \bullet V_{TR} / V_{CC}) \\ & + 0.2632 \bullet (1 - I_{OUT} / 12.00) \\ & - 0.667 \bullet 0.001 \bullet (T_{INT} - 25) + \Delta V_{OUT\text{-}LL} \end{aligned} \quad (4)$$

*DCM in Enhanced $V_{OUT}$ Regulation Mode*

In Enhanced $V_{OUT}$ Regulation Mode, only trim (Equation 3) is applicable. The general equation relating the DC $V_{OUT}$ to programmed trim is given by:

$$V_{OUT} = 2.70 + (3.260 \bullet V_{TR} / V_{CC}) + \Delta V_{OUT\text{-}LL} \quad (5)$$

Finally, note that when the load current is below 10% of the rated capacity, there is an additional ΔV which may add to the output voltage, depending on the line voltage which is related to light-load boosting. Please see the section on light-load boosting below for details.

Use 0V for $\Delta V_{OUT\text{-}LL}$ when load is above 10% of rated load. See section on light-load boosting operation for light-load effects on output voltage.

### Output Current Limit

The DCM features a fully operational current limit which effectively keeps the module operating inside the Safe Operating Area (SOA) for all valid trim and load profiles. The current limit approximates a “brick wall” limit, where the output current is prevented from exceeding the current limit threshold by reducing the output voltage via the internal error amplifier reference. The current limit threshold at nominal trim and below is typically 120% of rated output current, but it can vary between 100% to 140%. In order to preserve the SOA, when the converter is trimmed above the nominal output voltage, the current limit threshold is automatically reduced to limit the available output power.

When the output current exceeds the current limit threshold, current limit action is held off by 1ms, which permits the DCM to momentarily deliver higher peak output currents to the load. Peak output power during this time is still constrained by the internal Power Limit of the module. The fast Power Limit and relatively slow Current Limit work together to keep the module inside the SOA. Delaying entry into current limit also permits the DCM to minimize droop voltage for load steps.

Sustained operation in current limit is permitted, and no de-rating of output power is required, even in an array configuration.

Some applications may benefit from well-matched current distribution, in which case fine tuning sharing via the trim pins permits control over sharing. The DCM does not require this for proper operation, due to the power limit and current limit behaviors described here.

Current limit can reduce the output voltage to as little as the UVP threshold ($V_{OUT\text{-}UVP}$). Below this minimum output voltage compliance level, further loading will cause the module to shut down due to the output undervoltage fault protection.

### Line Impedance, Input Slew Rate and Input Stability Requirements

Connect a high-quality, low-noise power supply to the +IN and –IN terminals. Additional capacitance may have to be added between +IN and –IN to make up for impedances in the interconnect cables as well as deficiencies in the source.

Excessive source impedance can bring about system stability issues for a regulated DC-DC converter, and must either be avoided or compensated by filtering components. A 100µF input capacitor is the minimum recommended in case the source impedance is insufficient to satisfy stability requirements.

Additional information can be found in the filter design application note AN:023.

Please refer to this input filter design tool to ensure input stability.

Ensure that the input voltage slew rate is less than 1V/µs, otherwise a pre-charge circuit is required for the DCM input to control the input voltage slew rate and prevent overstress to input stage components.

### Input Fuse Selection

The DCM is not internally fused in order to provide flexibility in configuring power systems. Input line fusing is recommended at the system level, in order to provide thermal protection in case of catastrophic failure. The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than the DCM converter's maximum current)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Breaking capacity per application requirements
- Nominal melting $I^2t$
- Recommended fuse:
  See Safety Approvals for recommended fuse

### Fault Handling

#### *Input Undervoltage Fault Protection (UVLO)*

The converter's input voltage is monitored to detect an input undervoltage condition. If the converter is not already running, then it will ignore enable commands until the input voltage is greater than $V_{IN\text{-}UVLO+}$. If the converter is running and the input voltage falls below $V_{IN\text{-}UVLO–}$, the converter recognizes a fault condition, the powertrain stops switching, and the output voltage of the unit falls.

Input voltage transients which fall below UVLO for less than $t_{UVLO}$ may not be detected by the fault proection logic, in which case the converter will continue regular operation. No protection is required in this case.

Once the UVLO fault is detected by the fault protection logic, the converter shuts down and waits for the input voltage to rise above $V_{IN\text{-}UVLO+}$. Provided the converter is still enabled, it will then restart.

#### *Input Overvoltage Fault Protection (OVLO)*

The converter's input voltage is monitored to detect an input overvoltage condition. When the input voltage is more than the $V_{IN\text{-}OVLO+}$, a fault is detected, the powertrain stops switching, and the output voltage of the converter falls.

After an OVLO fault occurs, the converter will wait for the input voltage to fall below $V_{IN\text{-}OVLO–}$. Provided the converter is still enabled, the powertrain will restart.

The powertrain controller itself also monitors the input voltage. Transient OVLO events which have not yet been detected by the fault sequence logic may first be detected by the controller if the input slew rate is sufficiently large. In this case, powertrain switching will immediately stop. If the input voltage falls back in range before the fault sequence logic detects the out of range condition, the powertrain will resume switching and the fault logic will not interrupt operation. Regardless of whether the powertrain is running at the time or not, if the input voltage does not recover from OVLO before $t_{OVLO}$, the converter fault logic will detect the fault.

#### *Output Undervoltage Fault Protection (UVP)*

The converter determines that an output overload or short circuit condition exists by measuring its primary sensed output voltage and the output of the internal error amplifier. In general, whenever the powertrain is switching and the primary-sensed output voltage falls below $V_{OUT\text{-}UVP}$ threshold, a short circuit fault will be registered. Once an output undervoltage condition is detected, the powertrain immediately stops switching, and the output voltage of the converter falls. The converter remains disabled for a time $t_{FAULT}$. Once recovered and provided the converter is still enabled, the powertrain will again enter the soft-start sequence after $t_{INIT}$ and $t_{ON}$.

*Temperature Fault Protections (OTP)*

The fault logic monitors the internal temperature of the converter. If the measured temperature exceeds $T_{INT-OTP}$, a temperature fault is registered. As with the undervoltage fault protection, once a temperature fault is registered, the powertrain immediately stops switching, the output voltage of the converter falls, and the converter remains disabled for at least time $t_{FAULT}$. Then, the converter waits for the internal temperature to return to below $T_{INT-OTP}$ before recovering. Provided the converter is still enabled, the DCM will restart after $t_{INIT}$ and $t_{ON}$.

*Output Overvoltage Fault Protection (OVP)*

The converter monitors the output voltage during each switching cycle by a corresponding voltage reflected to the primary side control circuitry. If the primary sensed output voltage exceeds $V_{OUT-OVP}$, the OVP fault protection is triggered. The control logic disables the powertrain, and the output voltage of the converter falls.

This type of fault is latched, and the converter will not start again until the latch is cleared. Clearing the fault latch is achieved by either disabling the converter via the EN pin, or else by removing the input power such that the input voltage falls below $V_{IN-INIT}$.

**External Output Capacitance**

The DCM converter internal compensation requires a minimum external output capacitor. An external capacitor in the range of 470 – 10000µF with ESR of 10mΩ is required, per DCM for control loop compensation purposes.

However some DCM models require an increase to the minimum external output capacitor value in certain loading and trim condition. In applications where the load can go below 10% of rated load but the output trim is held constant, the range of output capacitor required is given by $C_{OUT-EXT-TRANS}$ in the Electrical Specifications table. If the load can go below 10% of rated load and the DCM output trim is also dynamically varied, the range of output capacitor required is given by $C_{OUT-EXT-TRANS-TRIM}$ in the Electrical Specifications table.

**Light-Load Boosting**

Under light-load conditions, the DCM converter may operate in light-load boosting depending on the line voltage. Light-load boosting occurs whenever the internal power consumption of the converter combined with the external output load is less than the minimum power transfer per switching cycle. In order to maintain regulation, the error amplifier will switch the powertrain off and on repeatedly, to effectively lower the average switching frequency, and permit operation with no external load. During the time when the powertrain is off, the module internal consumption is significantly reduced, and so there is a notable reduction in no-load input power in light-load boosting. When the load is less than 10% of rated $I_{OUT}$, the output voltage may rise by a maximum of 0.53V, above the output voltage calculated from trim, temperature and load line conditions.

## Thermal Design

Based on the thermal specified operating area shown on page 11, the full rated power of the DCM2322xA5N0660y6z can be processed provided that the top, bottom and leads are all held below 100°C. These curves highlight the benefits of dual sided thermal management, but also demonstrate the flexibility of the Vicor ChiP™ platform for customers who are limited to cooling only the top or the bottom surface.

The OTP sensor is located on the top side of the internal PCB structure. Therefore in order to ensure effective overtemperature fault protection, the case bottom temperature must be constrained by the thermal solution such that it does not exceed the temperature of the case top.

The ChiP package provides a high degree of flexibility in that it presents three pathways to remove heat from internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component for determining the maximum power that is available from a ChiP, as can be seen from Figure 26.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a real thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 26 shows the "thermal circuit" for a DCM2322 ChiP in an application where case top, case bottom and leads are cooled. In this case, the DCM power dissipation is $PD_{TOTAL}$ and the three surface temperatures are represented as $T_{CASE\_TOP}$, $T_{CASE\_BOTTOM}$, and $T_{LEADS}$. This thermal system can now be very easily analyzed with simple resistors, voltage sources and a current source.

This analysis provides an estimate of heat flow through the various pathways as well as internal temperature.

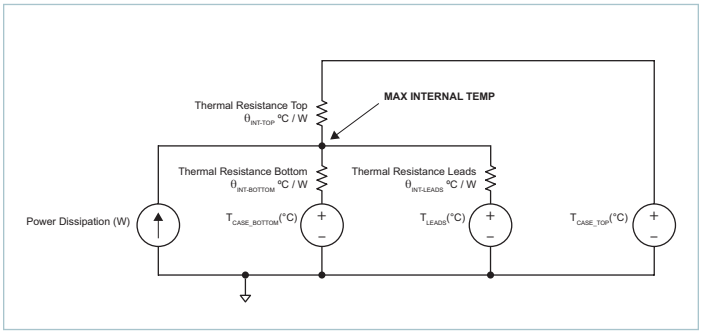



***Figure 26 —*** *Double-side cooling and leads thermal model*

Alternatively, equations can be written around this circuit and analyzed algebraically:

$$T_{INT} - PD_1 \bullet \theta_{INT\text{-}TOP} = T_{CASE\_TOP}$$
$$T_{INT} - PD_2 \bullet \theta_{INT\text{-}BOTTOM} = T_{CASE\_BOTTOM}$$
$$T_{INT} - PD_3 \bullet \theta_{INT\text{-}LEADS} = T_{LEADS}$$
$$PD_{TOTAL} = PD_1 + PD_2 + PD_3$$

Where $T_{INT}$ represents the internal temperature and $PD_1$, $PD_2$, and $PD_3$ represent the heat flow through the top side, bottom side and leads respectively.

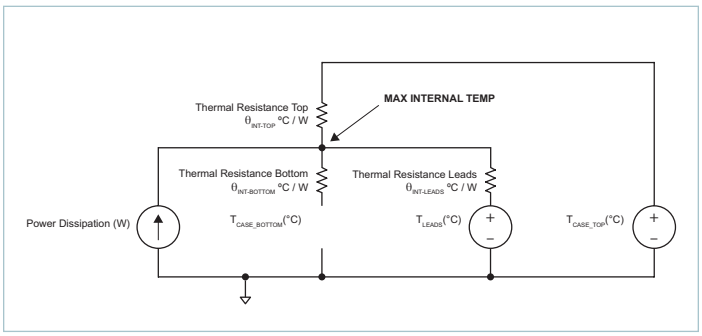



***Figure 27 —*** *One-side cooling and leads thermal model*

Figure 27 shows a scenario where there is no bottom-side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \theta_{INT\text{-}TOP} = T_{CASE\_TOP}$$
$$T_{INT} - PD_3 \bullet \theta_{INT\text{-}LEADS} = T_{LEADS}$$
$$PD_{TOTAL} = PD_1 + PD_3$$

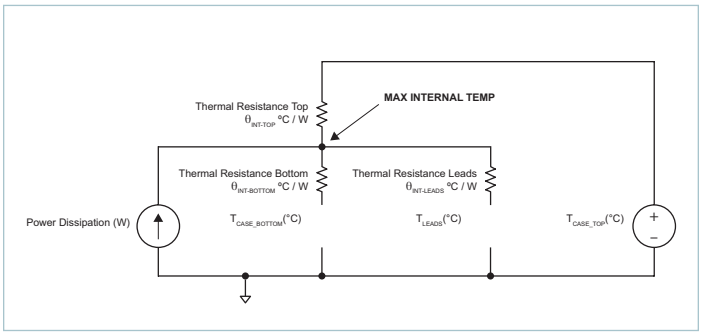



***Figure 28 —*** *One-side cooling thermal model*

Figure 28 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \theta_{INT\text{-}TOP} = T_{CASE\_TOP}$$
$$PD_{TOTAL} = PD_1$$

Vicor provides a suite of online tools, including a simulator and thermal estimator which greatly simplify the task of determining whether or not a DCM thermal configuration is sufficient for a given condition. These tools can be found at: www.vicorpower.com/powerbench.

| Symbol | Thermal Impedance (°C/W) | Definition of Estimated Thermal Resistance |
|---|---|---|
| $\theta_{INT\text{-}TOP}$ | 5.1 | to maximum-temperature internal component from isothermal top |
| $\theta_{INT\text{-}LEADS}$ | 11.4 | to maximum-temperature internal component from isothermal leads |
| $\theta_{INT\text{-}BOTTOM}$ | 5.7 | to maximum-temperature internal component from isothermal bottom |
| **Thermal Capacity** | | |
| 10.3Ws/°C | | |

***Table 1 —*** *Thermal data*

### Array Operation

*A decoupling network is needed to facilitate paralleling:*

- An output inductor should be added to each DCM, before the outputs are bussed together to provide decoupling.
- Each DCM needs a separate input filter, even if the multiple DCMs share the same input voltage source. These filters limit the ripple current reflected from each DCM, and also help suppress generation of beat frequency currents that can result when multiple powertrains input stages are permitted to directly interact.

If signal pins (TR, EN, FT) are not used, they can be left floating, and DCM will work in the nominal output condition.

When common-mode noise in the input side is not a concern, TR and EN can be driven and FT received using a single Kelvin connection to the shared –IN as a reference.

Note: For more information on parallel operation of DCMs, refer to "Parallel DCMs" application note AN:030.

An example of DCM paralleling circuit is shown in Figure 29.

*Filter components*

**Input filter:** The choice of the input filter components varies up on the low line and maximum output power of the DCM. Refer to the Filtering Guidelines Introduction section in the DCM Design Guide to design an input filter.

**Output filter:**

| Reference Designator | Value | Mfg. Part Number & Count/DCM |
|---|---|---|
| $C_{2\_x}$ | 80µF | GRM32EC72A106KE05L, #8 |
| $L_{2\_x}$ | 0.33µH | 744309033, #1 |
| $R_{dm\_x}$ | 1.5Ω | Generic |
| $L_{b\_x}$ | 72nH | IFLR2727EZER72NM01, #1 |

**$C_{OUT-EXT-x}$:** electrolytic or tantalum capacitor with at least 10mΩ ESR, 470µF ≤ **$C_{OUT-EXT}$** ≤ 10000µF;

**$C_3$, $C_4$:** additional ceramic /electrolytic capacitors, if needed for output ripple filtering;

*In order to help sensitive signal circuits reject potential noise, additional components are recommended:*

**$R_{2\_x}$:** 301Ω, facilitate noise attenuation for TR pin;

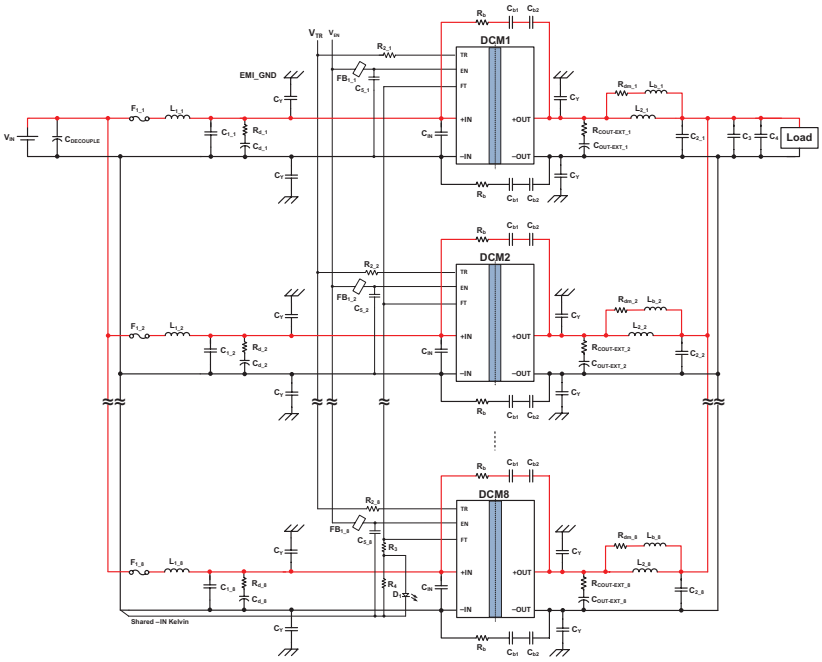
**$FB_{1\_x}$, $C_{5\_x}$:** **$FB_1$** is a ferrite bead with an impedance of at least 10Ω at 100MHz. **$C_{5\_x}$** can be a ceramic capacitor of 0.1µF. Facilitate noise attenuation for EN pin.

Note: Use an RCR filter network as suggested in the application note AN:030 to reduce the noise on the signal pins.

Note: In case of the excessive line inductance, a properly sized decoupling capacitor $C_{DECOUPLE}$ is required as shown in Figure 29 and Figure 30.

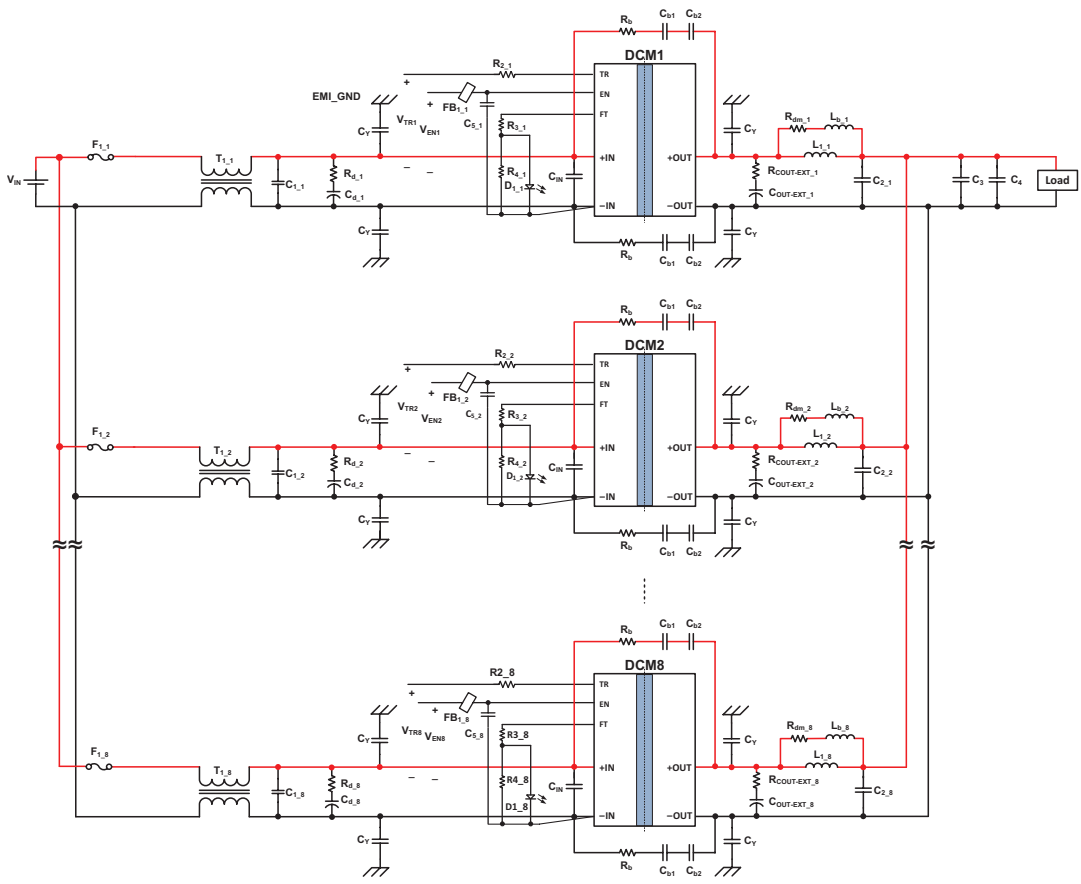
When common-mode noise rejection in the input side is needed, common-mode chokes can be added in the input side of each DCM. An example of DCM paralleling circuit is shown in Figure 30.

Notice that each group of control pins need to be individually driven and isolated from the other groups control pins. This is because –IN of each DCM can be at a different voltage due to the common mode chokes. Attempting to share control pin circuitry could lead to incorrect behavior of the DCMs.




**Note:** $C_{IN}$, $R_b$, $C_{b1}$ and $C_{b2}$ are required components for proper operation of the DCM. See required components table on page 2.

***Figure 29 —*** *DCM paralleling configuration circuit 1*




**Note:** $C_{IN}$, $R_b$, $C_{b1}$ and $C_{b2}$ are required components for proper operation of the DCM. See required components table on page 2.

***Figure 30 —*** *DCM paralleling configuration circuit 2*

Notice that each group of control pins needs to be individually driven and isolated from the other groups control pins. This is because –IN of each DCM can be at a different voltage due to the common-mode chokes. Attempting to share control pin circuitry could lead to incorrect behavior of the DCMs.

An array of DCMs used at the full array-rated power may generally have one or more DCMs operating at current limit, due to sharing errors. Load sharing is functionally managed by the load line. Thermal balancing is improved by the nominal effective temperature coefficient of the output voltage set point.

DCMs in current limit will operate with higher output current or power than the rated levels. Therefore the following Thermal Safe Operating Area plot should be used for arrays or loads that drive the DCM in to current limit for sustained operation.

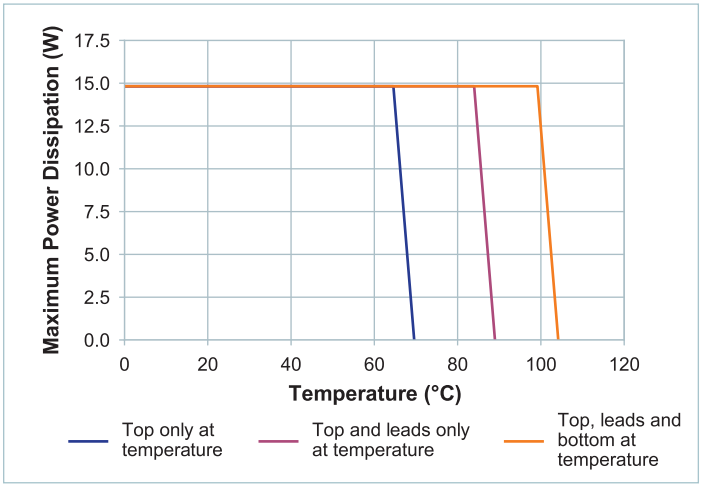
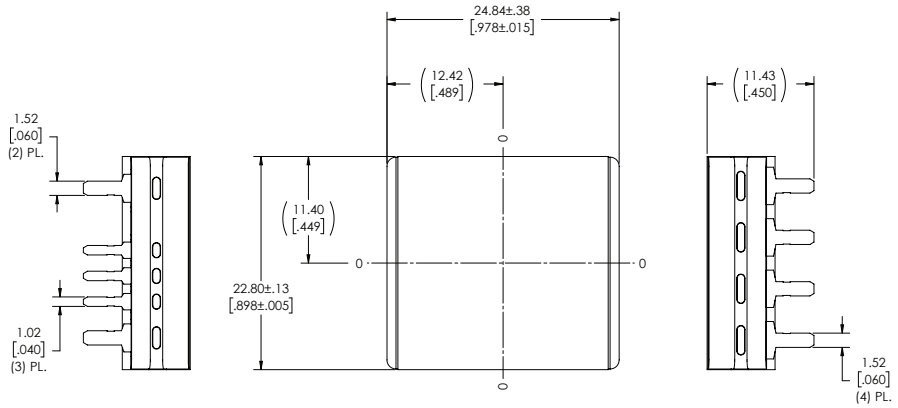


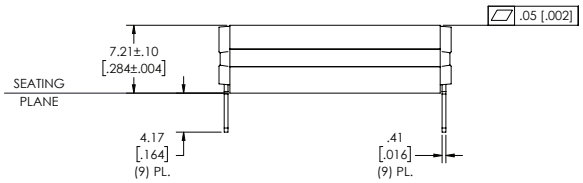

***Figure 31 —*** *Thermal specified operating area: max power dissipation vs. case temp for arrays or current-limited operation*

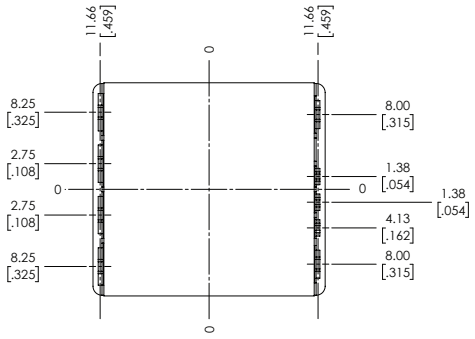
## DCM Module Product Outline Drawing Recommended PCB Footprint and Pinout

***2322 THRU HOLE***
(Reference DWG # 40292 Rev 5)

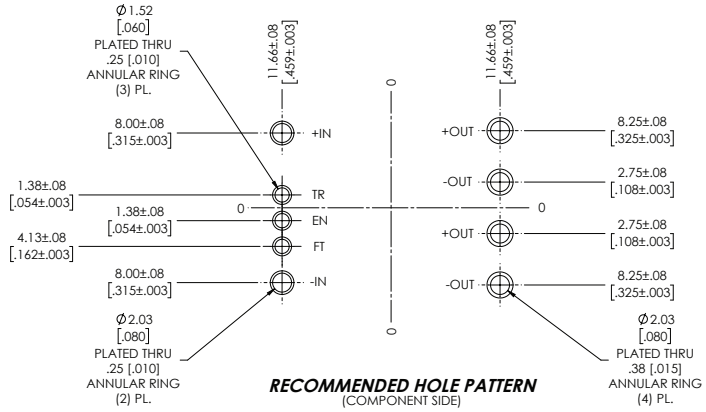



***TOP VIEW (COMPONENT SIDE)***




***BOTTOM VIEW***




***RECOMMENDED HOLE PATTERN***
(COMPONENT SIDE)

NOTES:
1- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM [INCH]
2- TOLERANCES ARE:
DECIMALS
X.XX [X.XX] = ±0.25 [0.01]
X.XXX [X.XXX] = ±0.127 [0.005]
ANGLES = ±1°

## Revision History

| Revision | Date | Description | Page Number(s) |
|---|---|---|---|
| 1.0 | 08/13/19 | Initial release | N/A |
| 1.1 | 09/05/19 | Updated signal pin names on mechanical drawing | 29 |
| 1.2 | 01/30/20 | Output voltage regulation specification format change | 8 |
| 1.3 | 11/04/22 | Updated agency approvals<br>Added insulation resistance specification<br>Added C-grade part number and related specs<br>Revised array operation section<br>Updated format, pages added<br>Corrected equation 1 notes | 1, 5<br>5<br>5, 7, 8<br>29<br>ALL<br>24 |
| 1.4 | 03/26/24 | Updated agency approvals<br>Removed C-grade part number and related specs<br>Revised thermal specified operating area | 1, 5<br>5, 7, 8<br>11 |

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