DCM™ DC-DC Converter

DCM3717S60E14G5TN0

48V to Point-of-Load Non-Isolated, Regulated DC Converter

Features & Benefits

- Wide input range 40 – 60V_{DC}
- Wide output range 10.0 – 13.5V_{DC}
- 97.0% peak efficiency
- Up to 750W or 62.5A continuous operation
- Up to 900W or 75A transient peak
- >1MHz switching frequency
- PMBus® compatible telemetry
- Internal voltage, current and temperature shut down
- Parallel-capable up to four units

Typical Applications

- Data Center Applications
- High-Performance Computing Systems (HPC)
- Mild Hybrid and Autonomous Vehicles
- Industrial Systems

Product Ratings	
V_{IN} = 40 – 60V	P_{OUT} = 750W
V_{OUT} = 12.2V Nominal (10.0 – 13.5V)	I_{OUT} = 62.5A (max)

Product Description

The DCM3717 is non-isolated, regulated DC-DC converter module that operates from a semi-regulated 40 – 60V input to generate a regulated point-of-load output voltage range of 10.0 – 13.5V. The DCM3717 in the SM-ChiP package configuration utilizes the Vicor patented zero-voltage switching (ZVS) buck-boost regulator stage followed by the Sine Amplitude Converter (SAC™).

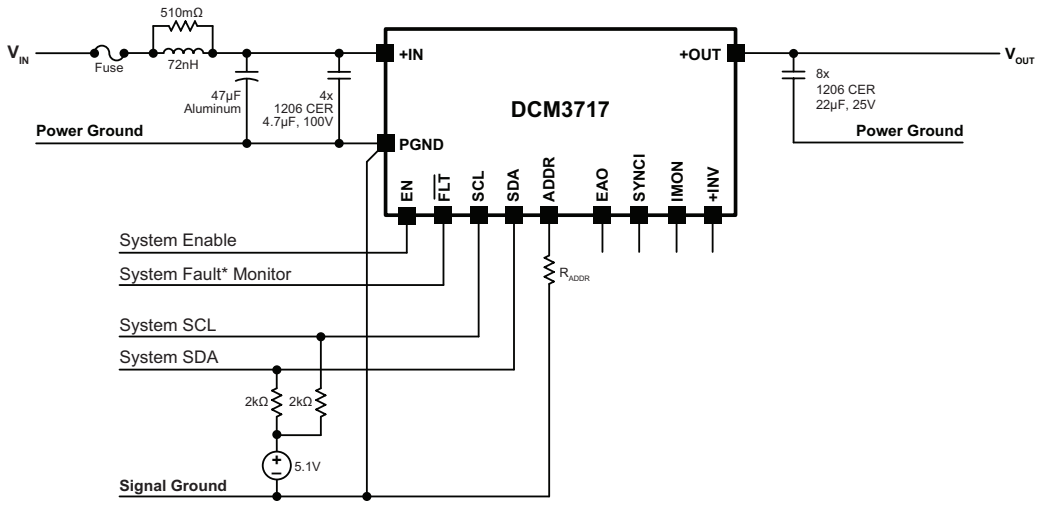
Leveraging the thermal density benefits of the Vicor SM-ChiP packaging technology, the DCM offers flexible thermal management options with very low top- and bottom-side thermal impedances. Thermally adept SM-ChiP based power components enable customers to achieve low-cost power system solutions with previously unattainable system size, weight and efficiency attributes quickly and predictably.

Package Information

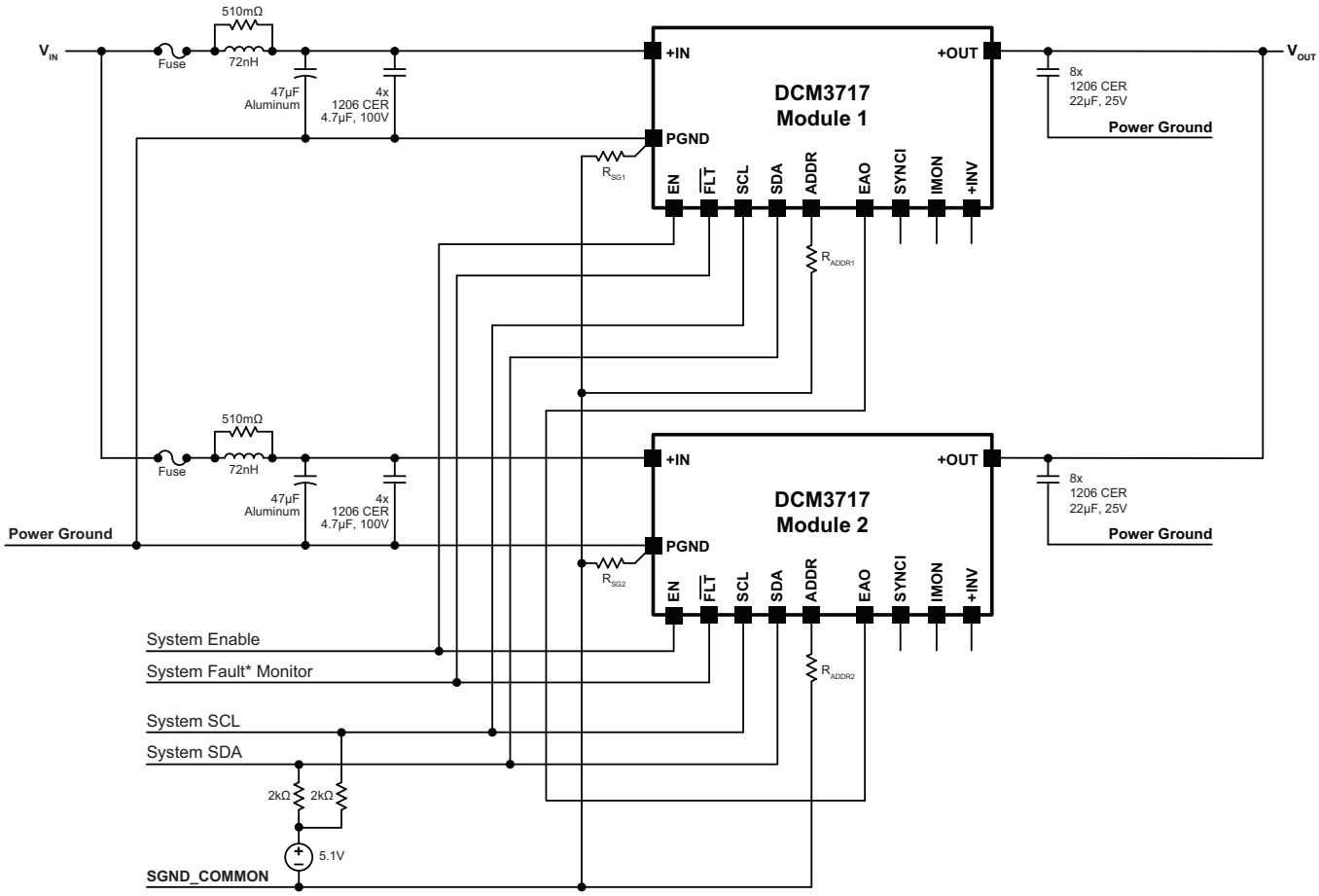
- Vicor DCM3717 SM-ChiP™ package enables low-impedance interconnect to system board
- 36.7 x 17.3 x 7.42mm

Note: Product images may not highlight current product markings.

Typical Application

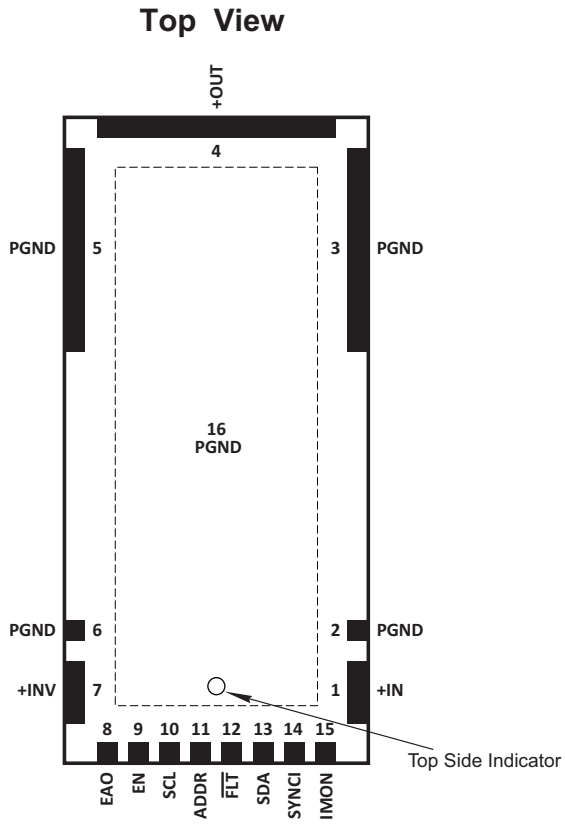


Typical application 1



Typical application 2: parallel array of two DCM3717 modules

Terminal Configuration



DCM3717 SM-ChiP™

Terminal Descriptions

Signal Name	Pin Number	Description
+IN	1	Positive input power terminal.
PGND	2, 3, 5, 6, 16 [a]	Power ground.
+OUT	4	Positive output power terminal.
+INV	7	Intermediate power terminal.
EAO	8	Transconductance error amplifier output and powertrain modulator control node.
EN	9	DCM Enable control.
SCL	10	Digital serial communication clock pin.
ADDR	11	I^2C™ address assignment.
$\overline{FLT}$ [b]	12	Fault Flag; pulled low when a fault is detected.
SDA	13	Digital serial communication data pin.
SYNCI	14	Factory use only.
IMON	15	Factory use only.

[a] Pin 16 represents the package top and bottom conductive plating. Refer to product outline for additional details.
[b] Overbar ($\overline{FLT}$) or star (FLT*) marking signify an active low designation.

Part Ordering Information

Part Number	Temperature Grade	Option	Tray Size
DCM3717S60E14G5**T**N**0**	**T** = –20 to 125°C	**0** = 12.2V nominal output	24 parts per tray

All products shipped in JEDEC standard high-profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

Storage and Handling Information

Note: For compressive loading refer to Application Note AN:036, "Recommendations for Maximum Compressive Force of Heat Sinks."

Attribute	Comments	Specification
Storage Temperature Range		–20 to 125°C
Operating Internal Temperature Range (T_{INT})		–20 to 125°C
Weight		19.5g
Package Plating		75µm copper with ENiG surface finish
MSL Rating		MSL4, 245°C maximum reflow temperature
ESD Rating	Human Body Model JEDEC JS-001-2017, Table 2B	Class 1B, ≤ 1000V
	Charged Device Model JESD22C101-E, JS-002-2018	CLASS 1C, ≥ 200V to < 500V

Reliability and Agency Approvals

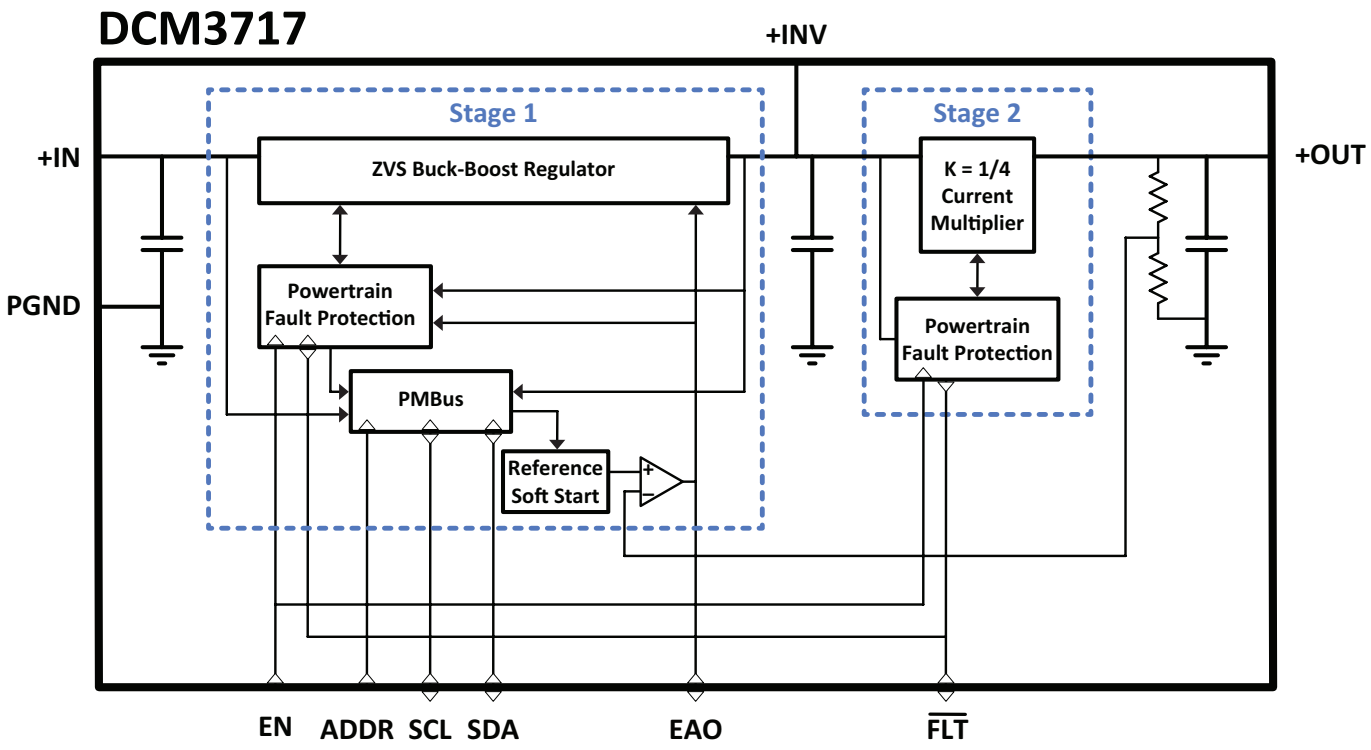
Attribute	Comments	Value	Unit
MTBF	Telcordia Issue 2, Method I Case 3	11.1	MHrs
	MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer	4.79	
Agency Approvals/Standards			
	CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable		

Absolute Maximum Ratings

Note: ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Operating beyond rated operating conditions for an extended period of time may affect device reliability. All voltages are referenced to PGND.

Parameter	Comments	Min	Max	Unit
+IN	Continuous, non-operating	–0.3	80	V
+INV	Continuous, non-operating	–0.3	80	V
			±40	A
+OUT	Continuous, non-operating	–0.3	15	V
			±120	A
EAO		–0.3	5.5	V
EN		–0.3	5.5	V
SCL, SDA, ADDR		–0.3	5.5	V
$\overline{FLT}$		–0.3	5.5	V
			±20	mA

Functional Block Diagram



Electrical Characteristics

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –20°C ≤ T_{INT} ≤ 125°C (T-Grade). All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Input Specifications						
Input Voltage Range	V_{IN}	Continuous, operating	**40.0**	54.0	**60.0**	V
Input Voltage Slew Rate	dV_{IN}/dt				1	V/µs
Input Voltage for ADDR Latch	V_{IN_ADDR}	Initial power up			**12**	V
No-Load Input Power	P_{NL}	ENABLE HIGH, V_{IN} = 54.0V, V_{OUT} = 12.2V		6	**7**	W
Input Quiescent Current	I_{QC}	ENABLE LOW, V_{IN} = 54.0V		6.8	**8**	mA
Input Current	I_{IN_DC}	I_{OUT} = 61.5A, V_{IN} = 54.0V, V_{OUT} = 12.2V		14.35	**14.5**	A
Input Capacitance (Internal)	C_{IN_INT}	Effective value, V_{IN} = 54.0V		2.25		µF
Input Capacitance (Internal) ESR	R_{C-IN}	Effective value, V_{IN} = 54.0V		8		mΩ
Powertrain Output Specifications						
Output Voltage Set Point	V_{OUT_SET}	DCM3717S60E14G5TN0, no load; typical value lists product nominal V_{OUT}	**12.07**	12.2	**12.32**	V
Output Voltage Trim Range	V_{OUT}		**10.0**		**13.5**	V
Output Voltage Load Regulation	$V_{OUT-REG-LOAD}$	For load > 10%		0.1	**0.2**	%
Output Voltage Line Regulation	$V_{OUT-REG-LINE}$			0.1	**0.3**	%
Total Regulation Error	$V_{OUT-REG-TOTAL}$				**0.5**	%
Rated Output Current, Continuous	I_{OUT}	V_{OUT} ≤ 12.0V			**62.5**	A
Rated Output Power, Continuous	P_{OUT}	12.0V < V_{OUT}			**750**	W
Rated Output Current, Peak	I_{OUT_PK}	V_{OUT} ≤ 12.0V, ≤ 1ms pulse width, ≤ 10% duty cycle			**75**	A
Rated Output Power, Peak	P_{OUT_PK}	12.0 < V_{OUT} ≤ 13.0V, ≤ 1ms pulse width, ≤ 10% duty cycle			**900**	W
		V_{OUT} = 13.5V, ≤ 1ms pulse width, ≤ 10% duty cycle; Rating is linear with V_{OUT}; see Figure 1			**850**	W
Array Size	n_{ARRAY}				**4**	DCMs
Switching Frequency, Buck-Boost Stage 1	F_{SW1}	V_{IN} = 54.0V, V_{OUT} = 12.2V, I_{OUT} = 61.5A	0.65	0.72	0.80	MHz
		Over rated line, continuous load, trim and temperature, exclusive of burst mode	**0.35**		**1.4**	
Switching Frequency, Current Multiplier Stage 2	F_{SW2}	V_{IN} = 54.0V, V_{OUT} = 12.2V, I_{OUT} = 61.5A	1.3	1.4	1.5	MHz
		Over rated line, continuous load, trim and temperature	**1.3**		**1.8**	
Transfer Ratio, Current Multiplier Stage 2	K			1/4		V/V
Minimum Off Time to Restart	t_{OFF}	When externally disabled with EN or $\overline{FLT}$ pin	**0**		**500**	µs
Off Time for Monotonic Restart	$t_{OFF-MONO}$	Extend disable time with EN or $\overline{FLT}$			**15**	s
Output Turn-On Delay	t_{ON}	From EN release to soft-start ramp, V_{IN} pre-applied		480		µs
Output Voltage Rise Time	t_{SS}	From soft start begin to V_{OUT} settled to within 5% for nominal V_{OUT}	**11**	16	**26**	ms
Output Voltage Soft-Start Slew Rate	dV_{OUT}/dt	All rated V_{OUT} trim range	0.47	0.76	1.1	V/ms

Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –20°C ≤ T_{INT} ≤ 125°C (T-Grade). All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Output Specifications (Cont.)						
Efficiency, Ambient	η_{AMB}	V_{IN} = 54.0V, V_{OUT} = 12.2V, I_{OUT} = 61.5A, T_{CASE} = 25°C	96.2	96.8		%
		V_{IN} = 54.0V, V_{OUT} = 12.2V, I_{OUT} = 31A, T_{CASE} = 25°C	96.4	96.6		
		V_{IN} = 40.0 – 60.0V, V_{OUT} = 12.2V, I_{OUT} = 31A, T_{CASE} = 25°C	95.0			
		V_{IN} = 40.0 – 60.0V, I_{OUT} = 55.6A, T_{CASE} = 25°C, over trim	94.0			
Efficiency, Hot	η_{HOT}	V_{IN} = 54.0V, V_{OUT} = 12.2V, I_{OUT} = 61.5A, T_{CASE} = 100°C	95.6	96.2		%
		V_{IN} = 54.0V, V_{OUT} = 12.2V, I_{OUT} = 31A, T_{CASE} = 100°C	95.7	96.3		
		V_{IN} = 40.0 – 60.0V, V_{OUT} = 12.2V, I_{OUT} = 31A, T_{CASE} = 100°C	94.8			
		V_{IN} = 40.0 – 60.0V, I_{OUT} = 55.6A, T_{CASE} = 100°C, over trim	93.2			
Efficiency Over Temperature	η	V_{IN} = 40.0 – 60.0V, V_{OUT} = 12.2V, >50% rated load current, over temperature	**94.2**			%
		V_{IN} = 40.0 – 60.0V, >50% rated load current, over temperature and trim	**93.2**			
Output Voltage Ripple	V_{OUT_PP}	V_{IN} = 54.0V, V_{OUT} = 12.2V, I_{OUT} = 61.5A, $C_{OUT-EXT}$ = 0µF, 20 MHz BW		280		mV_{P-P}
Output Capacitance (Internal)	C_{OUT_INT}	Effective value, V_{OUT} = 12.2V		45.5		µF
Output Capacitance (Internal) ESR	$R_{C_{OUT}}$	Effective value, V_{OUT} = 12.2V		2.9		mΩ
Load Capacitance (Electrolytic)	C_{LOAD_ALEL}		**0**		**10**	mF
Load Capacitance (Ceramic)	C_{LOAD_CER}	ESR ≤ 100mΩ, nominal value	**0**		**200**	µF
Load Capacitance (Total)	C_{LOAD_TOTAL}		**0**		**10**	mF
Load Transient Voltage Deviation	V_{TRANS}	10 ↔ 100% load step, 10A/µs, $C_{OUT-EXT}$ = 5x 22µF ceramic and 2x 1000µF aluminum		0.37	**0.5**	V
Load Transient Recovery Time	t_{TRANS}	10 ↔ 100% load step, 10A/µs, $C_{OUT-EXT}$ = 5x 22µF ceramic and 2x 1000µF aluminum		200		µs

Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –20°C ≤ T_{INT} ≤ 125°C (T-Grade). All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protections						
Input Undervoltage Turn-ON	V_{IN_UVLO+}	Powertrain recovery		37.3	**38.9**	V
Input Undervoltage Turn-OFF	$V_{IN\_UVLO–}$	Powertrain shut down	**34.8**	36.5		V
Input Overvoltage Turn-ON	$V_{IN\_OVLO–}$	Powertrain recovery	**61.0**	63.7		V
Input Overvoltage Turn-OFF	V_{IN_OVLO+}	Powertrain shut down		66.0	**69.2**	V
Overtemperature Shut Down	T_{OT}		**125**			°C
EAO Overload	V_{EAO_OL}		**3.23**	3.3		V
EAO Overload Timeout	t_{EAO_OL}	EAO continuously above V_{EAO_OL}		1000		µs
Overcurrent Shut Down	I_{OC}		**70**	87		A
Overcurrent Timeout	t_{IOC}	Output current above I_{OC}	**1**	4		ms
Short Circuit Shut Down	I_{SHORT}		**85**			A
Output OVP Turn-OFF	V_{OUT_OVP}	Relative to module +INV terminal	**55.5**		**56.7**	V
Output OVP Relative	$\%_{EAIN\_HI}$	Relative to the VOUT_COMMAND; inactive during start up and for t_{EAIN_HI} after a VOUT_COMMAND	**4**	15		%
Output OVP Relative Timeout	t_{EAIN_HI}	Blanking time for output OVP relative shut down following VOUT_COMMAND		2.1		s
Fault Protection Response Time	t_{PROT}	Excluding t_{EAO_OL} and t_{IOC} timeout periods		1		µs
Fault Protection Recovery Time	$t_{PROT\_RECOVERY}$	Excluding I_{OC}, I_{SHORT} and T_{OT} shut downs		30		ms
Overcurrent Protection Recovery Time	$t_{OC\_RECOVERY}$	Recovery from stage-2 multiplier OVP, I_{OC} shut downs only		140		ms
PMBus® Characteristics						
READ_VIN Accuracy	$V_{READ\_VIN\_ACC}$	At nominal V_{IN}	–1.4		1.4	V
READ_VIN Resolution	$V_{READ\_VIN\_RES}$	Limited to PMBus READ_VIN format resolution		125		mV
VOUT_COMMAND Functional Range	$V_{READ\_VIN\_RNG}$	Limits from MFR_VOUT_MIN and MFR_VOUT_MAX; Rated voltage trim range given by V_{OUT}	**6.0**		**14.03**	V
VOUT_COMMAND Resolution	$V_{READ\_VIN\_RNG}$			21.5		mV
READ_VOUT Accuracy	$V_{READ\_VOUT\_ACC}$	At nominal trim, +INV referred	–1.4		1.4	V
READ_VOUT Resolution	$V_{READ\_VOUT\_RES}$			35.2		mV
READ_TEMPERATURE Accuracy	$V_{READ\_TEMP\_ACC}$	Disabled, with T_{CASE} = 25°C	–6		6	°C
PMBus Operating Frequency Range	f_{PMBUS}	Child mode			**400**	kHz
STORE_USER_CODE Capacity	$N_{STORE\_USER\_CODE}$	Permanent storage of VOUT_COMMAND	**8**			Writes

Signal Characteristics

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –20°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Control Node: EAO								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog	Normal Operation	EAO Voltage Range	V_{EAO}	Across line, trim, load, temperature	**0.0**		**3.15**	V
		EAO Current Drive	I_{EAO}		**300**		**600**	µA
	Pulse Skipping	EAO Pulse Skip Threshold	V_{EAO_SKIP}	Lower side of hysteretic range		0.4		V
	Fault Protection Active	EAO Sink Current	I_{EAO_FAULT}	Pull down to 0V		450		µA

Enable: EN								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Digital Input	Any	EN High Threshold	V_{EN_HIGH}		**1.1**			V
		EN Low Threshold	V_{EN_LOW}				**0.7**	V
	No Fault	EN Source Current	I_{EN}	Pull up to 2V		50		µA

Serial Clock: SCL Serial Data: SDA								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Digital Input/Output	Any	Rated Input Range	V_{SERIAL}		**0.0**		**5.0**	V
		SCL Frequency	F_{SCL}		**100**		**400**	kHz
		Input High Voltage	V_{IH}		**1.35**			V
		Input Low Voltage	V_{IL}				**0.8**	V
		Output Low Voltage	V_{OL}	Sinking 6mA			**0.4**	V

Address: ADDR								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Multi-level Digital Input	Initial Power Up	Address Registration Delay	t_{ADDR_DLY}	From V_{IN} crossing V_{IN_ADDR}		10.5	**30**	ms

Fault: $\overline{FLT}$								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Open Drain Digital I/O	Normal Operation	Pull-up Voltage	$V_{\overline{FLT}\_INACTIVE}$	Effective $R_{PULL-UP}$ = 10kΩ			**5.3**	V
Digital Output	Fault Protection Active	Sink Current	$I_{\overline{FLT}\_ACTIVE}$	Fault active, $V_{\overline{FLT}}$ = 400mV	**4**			mA
Digital Input	Transition to Fault	Input Voltage Threshold	$V_{\overline{FLT}\_ACTIVE}$	To externally induce shut down	**0.85**		**1.1**	V

Specified Operating Area

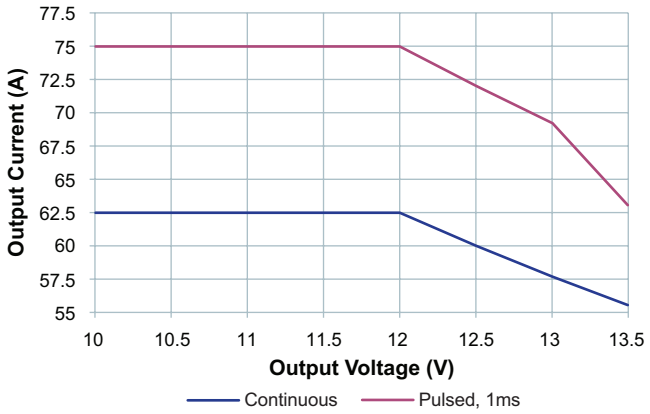


Figure 1 — *Electrical specified operating area vs. V_{OUT}*

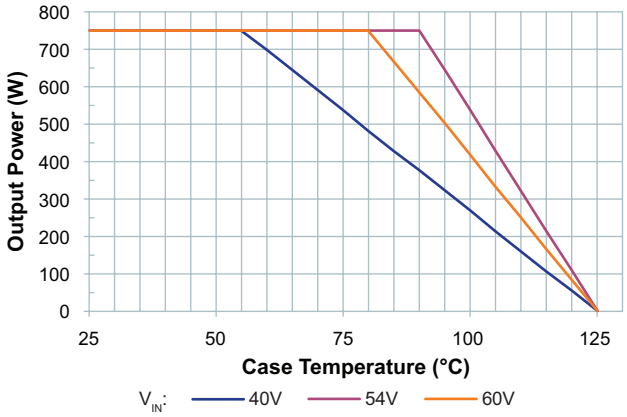


Figure 2 — *Thermal specified operating area; bottom-side cooling, output power vs. case temperature, nominal trim*

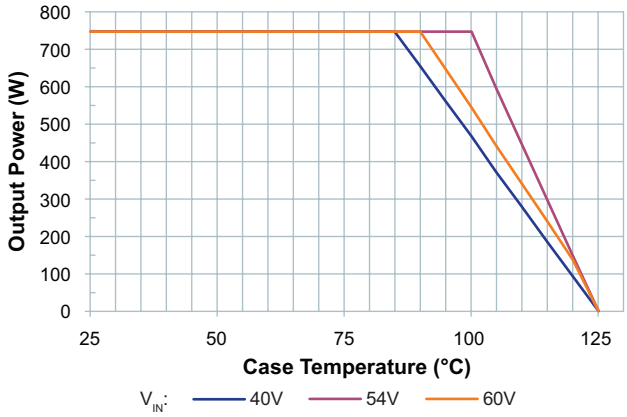


Figure 3 — *Thermal specified operating area; double-sided cooling, output power vs. case temperature, nominal trim*

Typical Performance Characteristics – Efficiency and Power Dissipation

The following figures present performance data in a typical application environment.

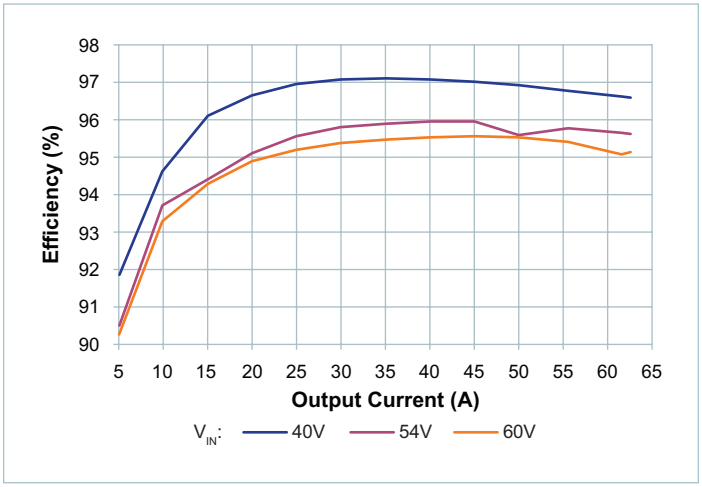


Figure 5 — *Efficiency at 25°C case temperature, V_{OUT} = 10.0V*

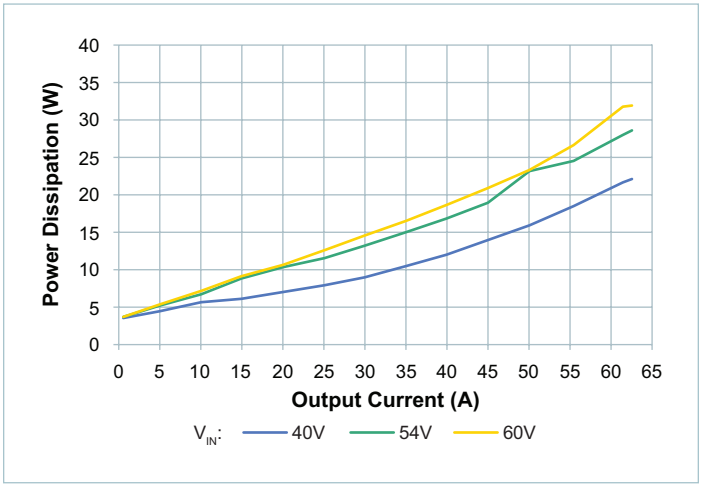


Figure 6 — *Power dissipation at 25°C case temperature, V_{OUT} = 10.0V*

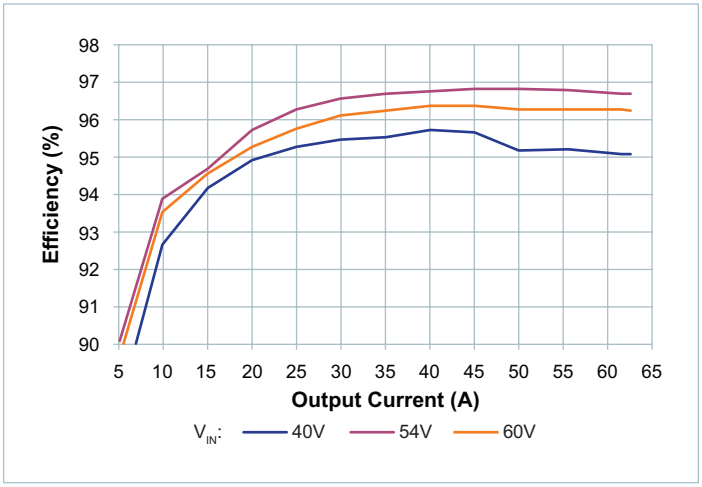


Figure 7 — *Efficiency at 25°C case temperature, V_{OUT} = 12.2V*

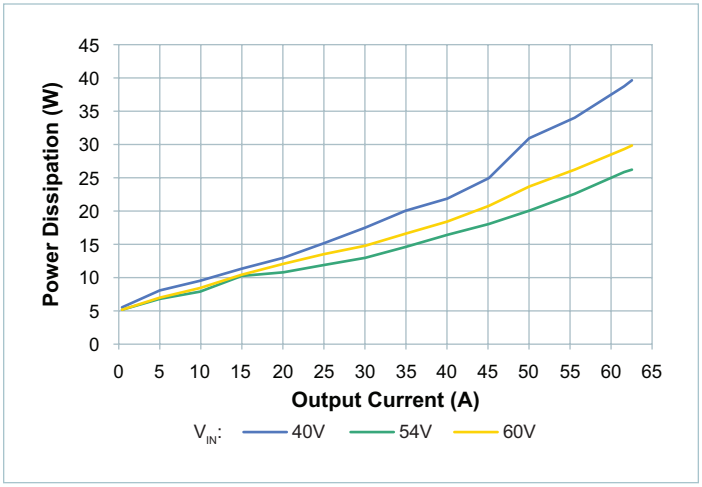


Figure 8 — *Power dissipation at 25°C case temperature, V_{OUT} = 12.2V*

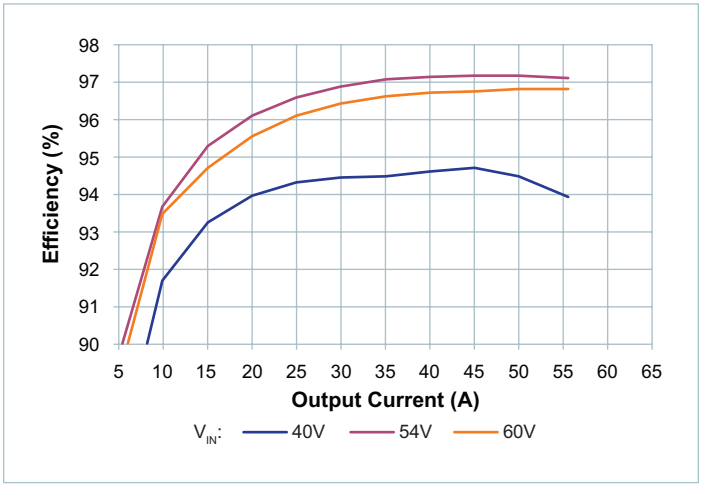


Figure 9 — *Efficiency at 25°C case temperature, V_{OUT} = 13.5V*

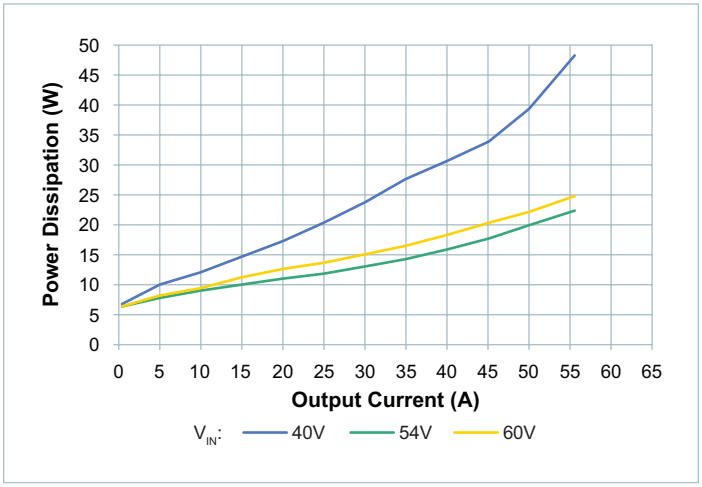


Figure 10 — *Power dissipation at 25°C case temperature, V_{OUT} = 13.5V*

Typical Performance Characteristics – Efficiency and Power Dissipation (Cont.)

The following figures present performance data in a typical application environment.

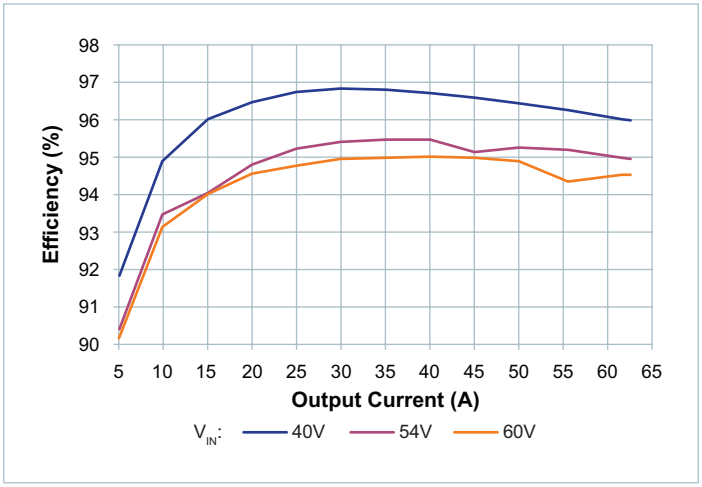


Figure 11 — *Efficiency at 100°C case temperature, V_{OUT} = 10.0V*

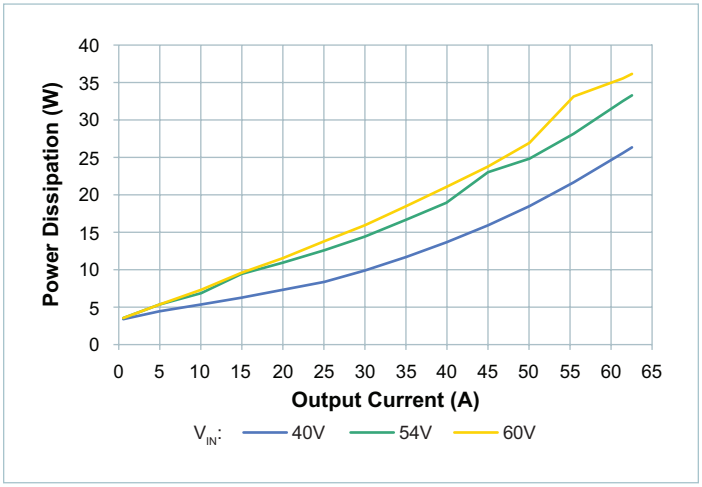


Figure 12 — *Power dissipation at 100°C case temperature, V_{OUT} = 10.0V*

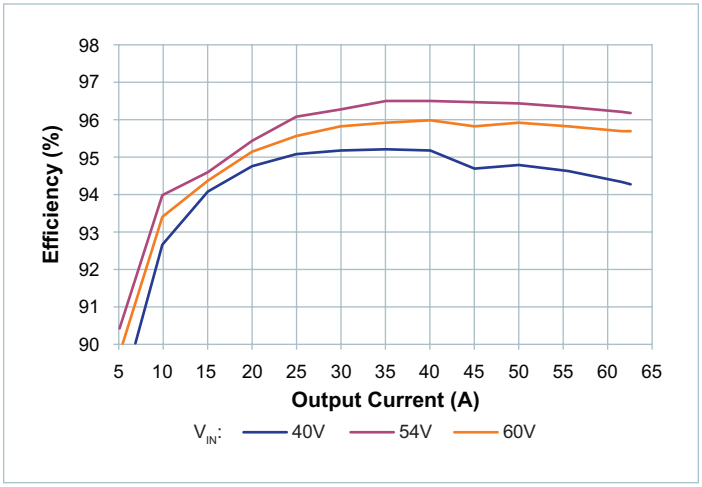


Figure 13 — *Efficiency at 100°C case temperature, V_{OUT} = 12.2V*

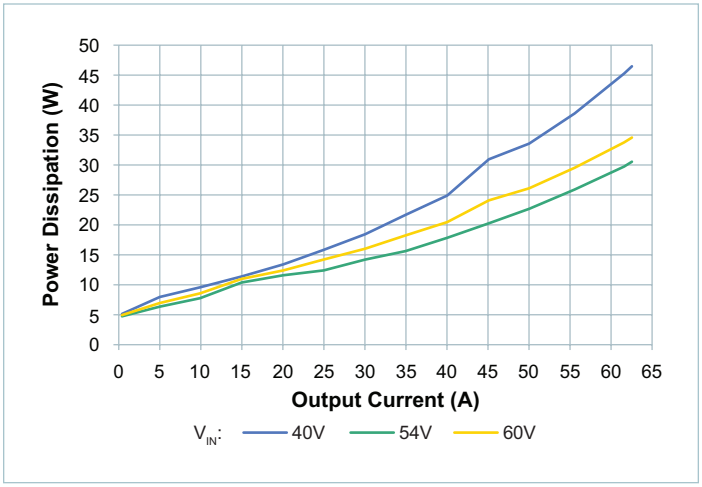


Figure 14 — *Power dissipation at 100°C case temperature, V_{OUT} = 12.2V*

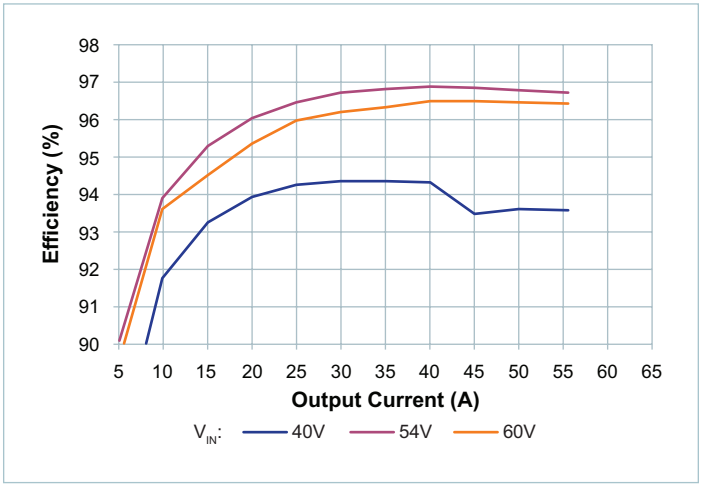


Figure 15 — *Efficiency at 100°C case temperature, V_{OUT} = 13.5V*

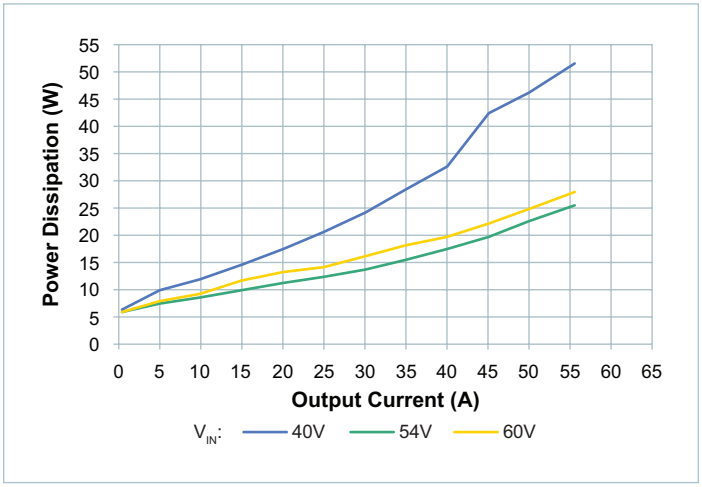


Figure 16 — *Power dissipation at 100°C case temperature, V_{OUT} = 13.5V*

Typical Performance Characteristics – Efficiency and Power Dissipation (Cont.)

The following figures present performance data in a typical application environment.

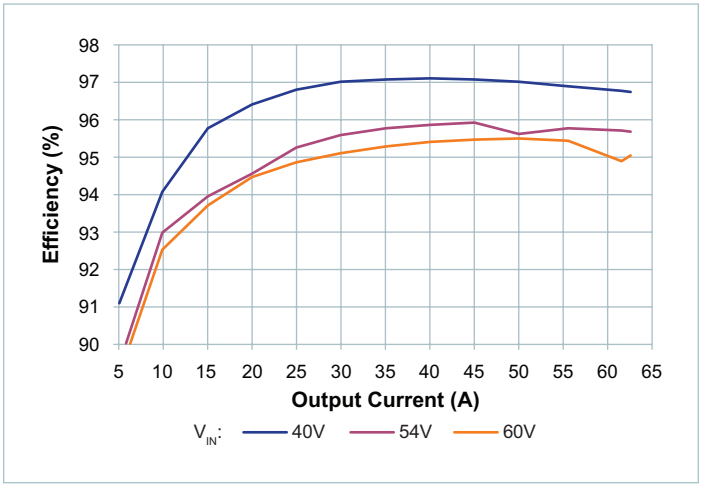


Figure 17 — *Efficiency at –20°C case temperature, V_{OUT} = 10.0V*

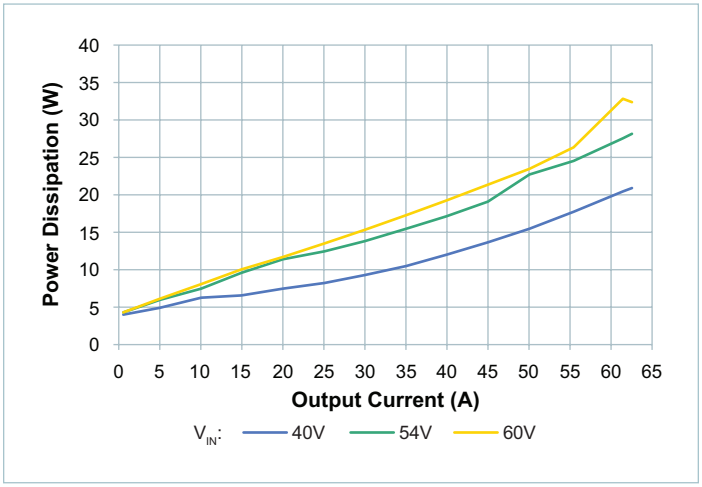


Figure 18 — *Power dissipation at –20°C case temperature, V_{OUT} = 10.0V*

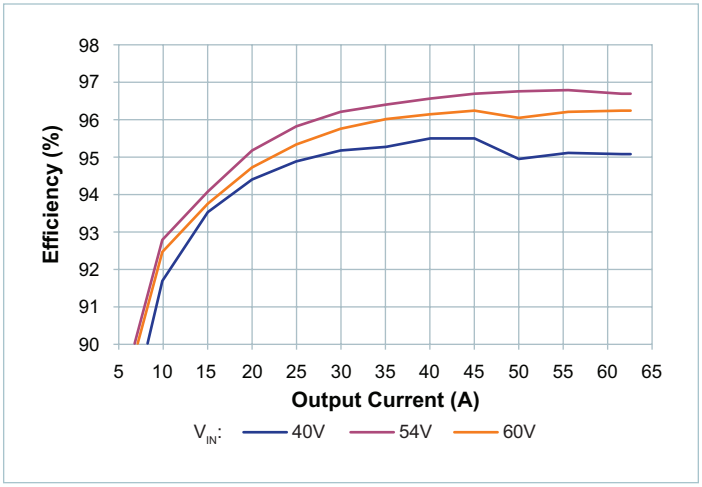


Figure 19 — *Efficiency at –20°C case temperature, V_{OUT} = 12.2V*

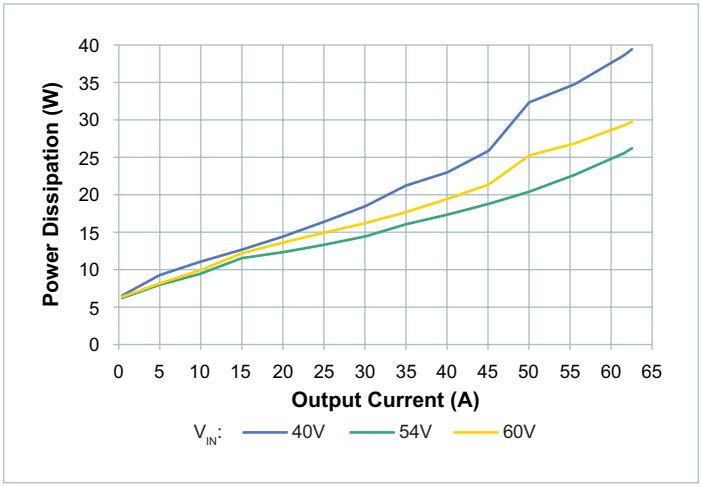


Figure 20 — *Power dissipation at –20°C case temperature, V_{OUT} = 12.2V*

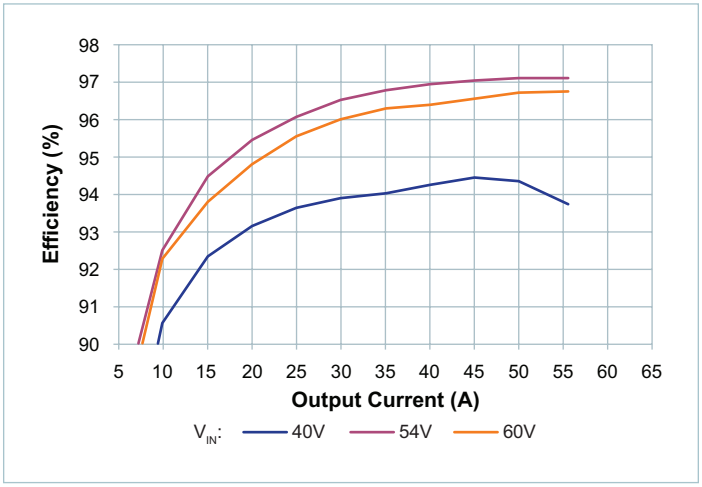


Figure 21 — *Efficiency at –20°C case temperature, V_{OUT} = 13.5V*

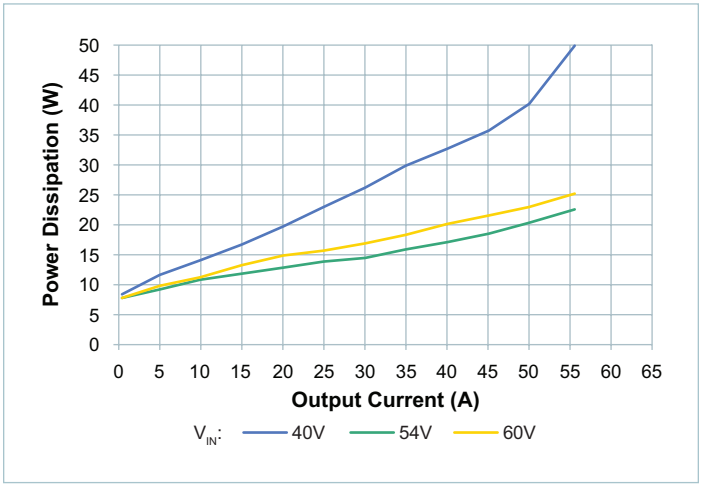


Figure 22 — *Power dissipation at –20°C case temperature, V_{OUT} = 13.5V*

Terminal Descriptions

+IN – DCM Input Power

The +IN pin is the power input to the regulation stage. External filtering and decoupling techniques are application-specific. Low-ESR ceramic capacitors are recommended between the DCM input and power ground.

PGND – Power Ground

The DCM is a three-terminal non-isolated regulator. PGND is the common power return for +IN and +OUT.

+OUT – DCM Output Power

The +OUT pin is the power output from the current multiplication stage. External filtering and decoupling techniques are application-specific. Low-ESR ceramic capacitors are recommended between the DCM output and power ground.

+INV – DCM Intermediate Power Node

The +INV pin is an intermediate power node between the regulation and current-multiplication powertrain stages.

EAO – Modulator Input

The EAO pin provides access to the error amplifier output and is the control node input to the regulation stage, which determines the DCM output power.

EN – Enable

If the EN pin is left floating or driven high, the DCM is enabled. When EN is pulled low, the DCM is disabled.

ADDR, SCL, SDA – PMBus Interface Address, Serial Clock and Serial Data

Address is a multi-level analog input which sets the address at initial power-up. See PMBus® interface section for details on device address.

Serial clock (SCL) and serial data (SDA) require external pull-up resistors for normal operation. Refer to System Management Bus (SMBus) Specification version 3.0 for details.

$\overline{\text{FLT}}$ – Fault Monitor

$\overline{\text{FLT}}$ is an open-drain pin with an internal pull-up and indicates fault status. $\overline{\text{FLT}}$ is active-low, so when any fault protection is active the pin will drive low. When the module is enabled and not in a fault condition, the pin will be pull high. The module monitors the status of this pin, and so if an external sub-circuit pulls $\overline{\text{FLT}}$ low, the module will also be disabled.

Note: $\overline{\text{FLT}}$ displayed as FLT* on the package drawing.

SYNCI – Factory Use Only

Do not connect to the SYNCI pin.

IMON – Factory Use Only

Do not connect to the IMON pin.

Functional Description

The DCM3717S60E14G5TN0 is a non-isolated, regulated DC-DC power converter with PMBus® control and telemetry, in a thermally adept package. It consists of a ZVS buck-boost first-stage block followed by a ZVS, ZCS Sine Amplitude Converter™ current multiplier second stage. The current multiplier operates at a fixed step-down ratio of 4, and so all regulation is performed by Stage 1. The output voltage sense for the regulation control loop is taken at the module output terminals after the current multiplier, for tight regulation accuracy. All PMBus output voltage set-point control and telemetry is provided by Stage 1.

The DCM offers peak current and power ratings that are generally 20% higher than the continuous ratings for up to 1ms for dynamic loads higher transient requirements. The full peak load capability is available up to an output voltage set point of 13.0V. Above 13.0V the peak current rating is linearly reduced to avoid risk of shut down due to overvoltage protection, as shown in Figure 1.

DCM Power Up

When input voltage is applied, the DCM PMBus address is sensed and latched based on the pull-down resistor applied to the ADDR pin. The address remains fixed until input voltage is removed.

DCM Start Up

Any time the DCM input voltage is within UVLO and OVLO, the DCM has not been disabled via the EN or $\overline{FLT}$ control pins, and it has recovered from any previously occurring fault protections, it will attempt to start.

At start up, the $\overline{FLT}$ pin goes inactive (high) and the Stage 2 current multiplier begins switching. Then the Stage 1 buck-boost regulator stage begins switching and its reference rises to generate the soft-start ramp of module output voltage. The module output is capable of full rated continuous output current during soft-start.

The DCM output voltage rise is monotonic during soft start into static loads, once V_{OUT} exceeds 1.2V, provided the module has been disabled for at least $t_{OFF\text{-}MONO}$. If the module restarts more quickly than $t_{OFF\text{-}MONO}$ then residual energy stored on the +INV node between the Stage 1 and Stage 2 powertrains can cause an output voltage transient to occur at the beginning of the soft-start ramp.

The DCM can start up into a precharged output up to 6.0V with no additional considerations. Starting the DCM into a precharged V_{OUT} higher than 6.0V is not recommended due to risk that ring-up could trigger $V_{OUT\text{-}OVP}$ fault.

Pulse-Skip Mode (PSM)

The ZVS buck-boost stage features a hysteretic pulse-skipping mode. At light-load conditions, switching cycles can be skipped in order to significantly reduce gate-drive power and improve efficiency. The regulator will automatically enter and exit PSM based on load. Depending on line and trim operating conditions, as well as capacitor and other component values, PSM may result in occasional skipping of one or many switching cycles.

Variable-Frequency Operation

The ZVS buck-boost stage is pre-programmed to a fixed, maximum base operating frequency. The maximum processed power determines the base frequency and associated power inductor with respect to other constraints to achieve peak efficiency at nominal operation. The operating frequency can be reduced from the base frequency as needed to maintain rated power capability at certain line voltage, trim voltage and load conditions. By reducing the operating frequency, or stretching the period of each switching cycle, the ZVS operation is preserved throughout the input line voltage range maintaining optimum efficiency. The current multiplication stage also exhibits variable frequency operation, though over a smaller frequency range relative to that of the ZVS buck-boost stage.

DCM Fault Response

If the DCM detects a fault condition, the $\overline{FLT}$ pin drives low and the module stops processing power within the fault protection response time t_{PROT}. The input overvoltage, input undervoltage, and overtemperature fault conditions, as well as $\overline{FLT}$ pin low are continuously monitored, and the DCM will not restart as long as they persist. Once the fault condition is removed and the appropriate fault recovery time ($t_{PROT\_RECOVERY}$ or $t_{OC\_RECOVERY}$) has elapsed, the DCM will release $\overline{FLT}$ and will attempt a restart. Other fault types like overload or short circuit condition can only occur when the module is operating. After shut down, the DCM will repeatedly attempt a restart after a delay, and will shut down again as long the load fault condition persists.

Input Undervoltage Recovery and Lockout Threshold (V_{IN_UVLO+} and V_{IN_UVLO-})

The regulator stage monitors the +IN pin. The DCM will not start until the input voltage exceeds the undervoltage recovery threshold (V_{IN_UVLO+}), and the DCM will shut down if the input voltage crosses below the undervoltage lockout threshold (V_{IN_UVLO-}).

A V_{IN_UVLO} will set byte 0, bit 3 in the MFR_STATUS_FAULTS (F0h) status register.

Input Overvoltage Lockout Threshold and Recovery (V_{IN_OVLO+} and V_{IN_OVLO-})

If the input voltage rises above the overvoltage lockout threshold (V_{IN_OVLO+}), the DCM will shut down. $\overline{FLT}$ is active continuously while the input voltage is too high.

For both input voltage fault protections, $\overline{FLT}$ drives low continuously when the input voltage is out of range. Once input voltage is reestablished and after Fault Protection Recovery Time ($t_{PROT\_RECOVERY}$) has elapsed, $\overline{FLT}$ is released and the regulator will restart.

A V_{IN_OVLO} will set byte 0, bit 4 in the MFR_STATUS_FAULTS (F0h) status register.

Overtemperature Fault Threshold (T_{OT})

The DCM features a thermal shut down, T_{OT}, which is designed to protect against catastrophic failure due to excessive temperatures. The overtemperature shut down cannot be used to ensure the device stays within the recommended operating temperature range, because it engages when the product is operated above the maximum rated temperature. As with other fault protections, when overtemperature shut down occurs, the DCM stops processing power and $\overline{FLT}$ drives low. The DCM will restart after the temperature has decreased.

If the Overtemperature fault threshold is exceeded, byte 2, bit 0 in the MFR_STATUS_FAULTS (F0h) status register will be set.

$\overline{FLT}$ Fault

If the $\overline{FLT}$ terminal is externally pulled low, the unit will shut down in the same manner as the other fault protections listed here.

When $\overline{FLT}$ fault is detected, the FLT_FALLING_EDGE bit will be set, MFR_STATUS_FAULTS (F0h) status register, byte 1, bit 0.

Output Overvoltage Threshold (V_{OUT_OVP})

The DCM will shut down if the output voltage rises above the OVP threshold, V_{OUT_OVP}. The sense point is taken before the second-stage current multiplier, and so the effective output-referred threshold depends on the voltage drop across the second stage.

A VOUT_OVP fault will set byte 0, bit 5 in the MFR_STATUS_FAULTS (F0h) status register.

Output OVP Relative ($\%_{EAIN\_HI}$)

The DCM will shut down if the module output voltage is more than $\%_{EAIN\_HI}$ higher than the programmed output voltage, for more than t_{EAIN_HI}. This protection is inactive during soft start as well as for timeout period t_{EAIN_HI} following a VOUT_COMMAND change to output voltage trim.

$\%_{EAIN\_HI}$ will set EAIN_HI, byte 1, bit 5 in the MFR_STATUS_FAULTS (F0h) status register.

EAO Overload (V_{EAO_OL})

EAO is the control input to the Stage 1 regulator. The EAO voltage is driven by the internal transconductance error amplifier closing the voltage control loop. The voltage on EAO can exceed the EAO Overload Threshold voltage (V_{EAO_OL}) when the DCM is overloaded.

A timer permits transient overload conditions to occur without triggering fault protection. However if EAO remains above its overload threshold for longer than t_{EAO_OL}, the DCM will shut down and $\overline{FLT}$ will be driven low.

The EAO Overload fault will set byte 2, bit 2 in the MFR_STATUS_FAULTS (F0h) status register.

Overcurrent Threshold (I_{OC})

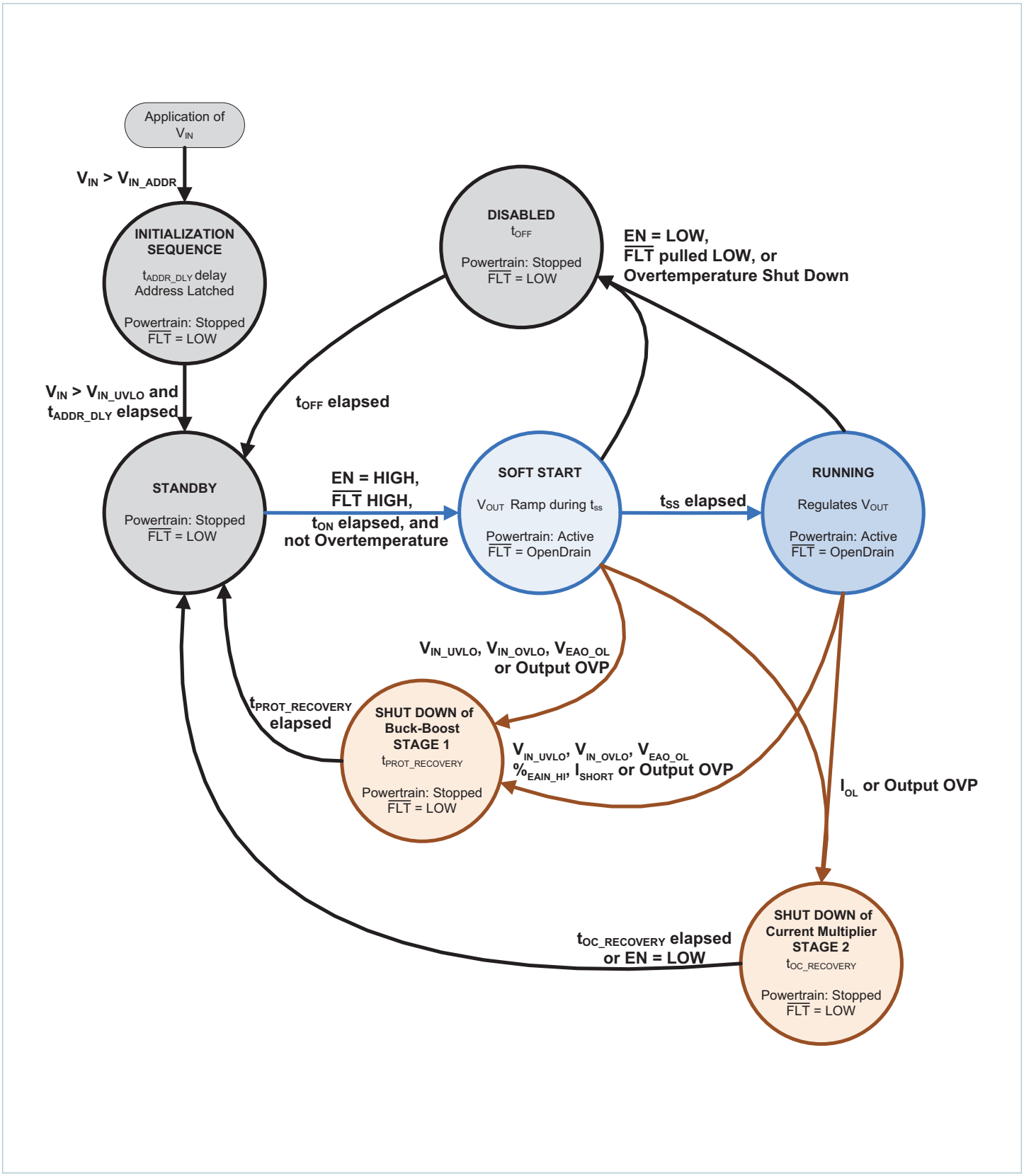
The DCM output current is continuously measured during operation, and if it exceeds the overcurrent shutdown threshold (I_{OC}), for longer than overcurrent timeout (t_{IOC}), the DCM will shutdown and $\overline{FLT}$ is driven low. Unlike the other fault protections, overcurrent is monitored by both the current multiplier stage and the buck-boost regulation stage. If the buck-boost stage detects the overcurrent, then the MFR_STATUS_FAULT bits VOUT_NEG or Q3_SIL may set. If only the current multiplier stage detects the fault, then only the $\overline{FLT}$ pin falling edge will be set. Any of these bits indicate the presence of an overcurrent condition. The DCM will restart after the recovery time $t_{PROT\_RECOVERY}$ or $t_{OC\_RECOVERY}$ depending on which powertrain stage shut down.

Short Circuit Protection (I_{SHORT})

In the event of a short circuit occurring during operation or during start up, the DCM fast short-circuit protection will shut down the powertrain and drive $\overline{FLT}$ low. The MFR_STATUS_FAULT bits Q1_FIL or Q3_FIL should set. The VOUT_NEG may also set. The DCM will restart after the recovery time $t_{PROT\_RECOVERY}$.

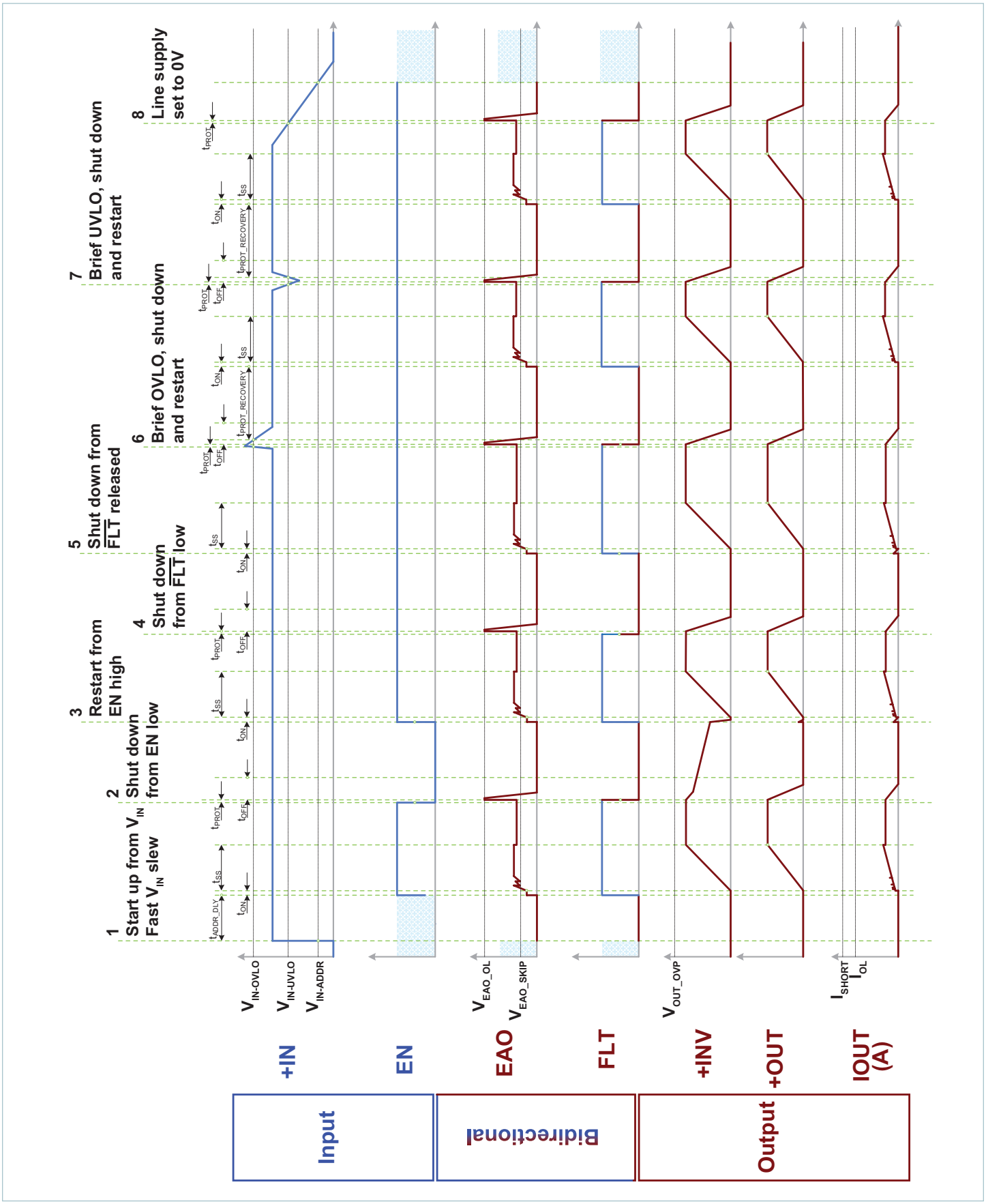
High-Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



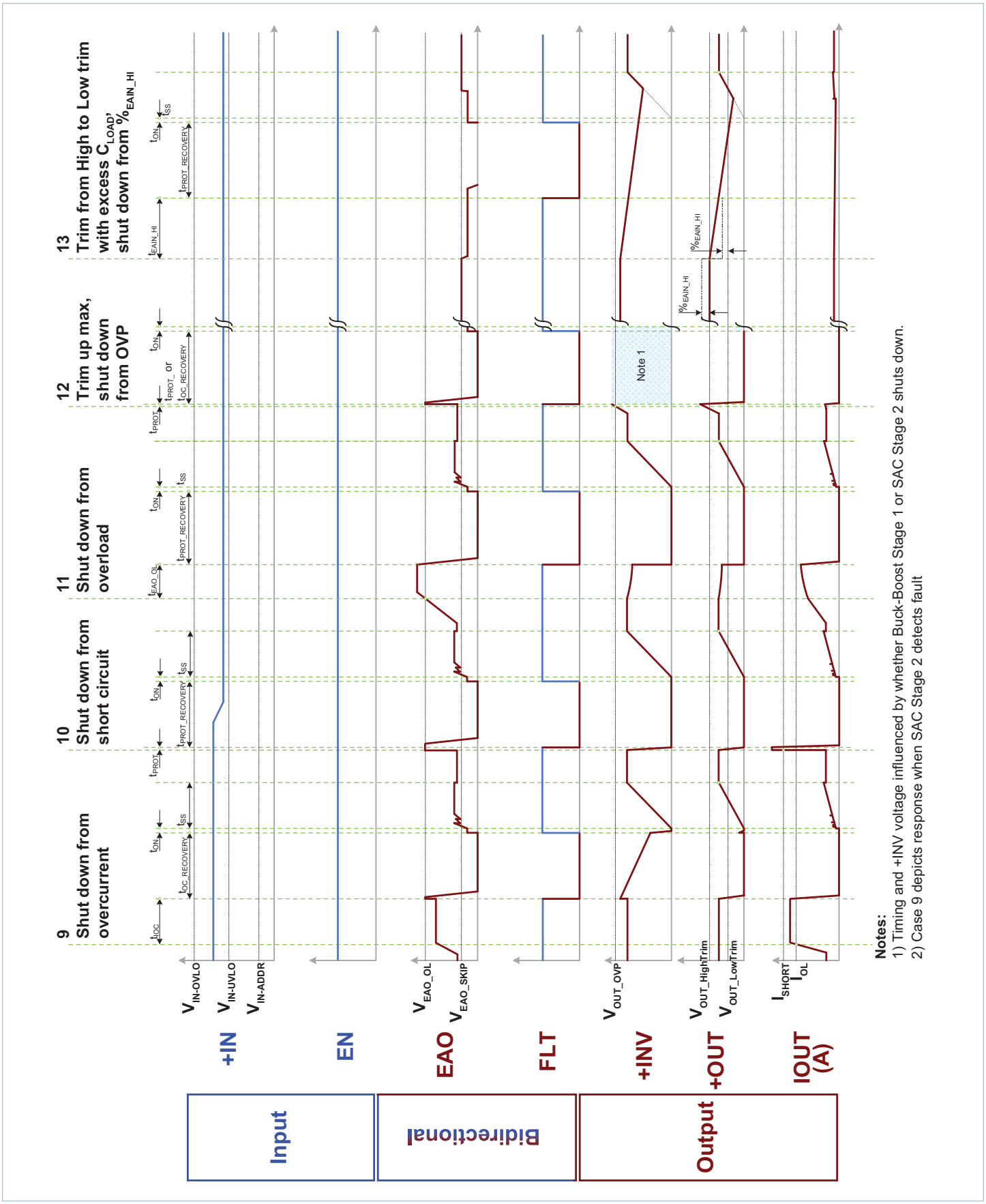
Timing Diagrams

Module inputs are shown in blue; module outputs are shown in brown.



Timing Diagrams (Cont.)

Module inputs are shown in blue; module outputs are shown in brown.



Design Guidelines

Input Filter Stability

Regulating switch-mode power supplies like the DCM present a negative impedance to the voltage source that is powering them. To ensure stability of the regulation loop, the source impedance and the parasitic resistance and inductance of the interconnect lines must be considered. The high performance ceramic decoupling capacitors placed locally to the input to the DCM are effective in controlling reflected ripple current at the switching frequency. However their low ESR means they will not significantly damp an excessively high impedance of an upstream voltage source.

The regulator dynamic input impedance magnitude r_{EQ_IN} can be calculated by dividing the lowest line voltage by the full load input current. To ensure stability, two cases must be considered.

Input Filter case 1; inductive source and local, external, input decoupling capacitance with negligible ESR (i.e., ceramic type)

The voltage source impedance can be modeled as a series R_{LINE} L_{LINE} circuit. In order to guarantee stability the following conditions must be verified:

$$R_{LINE} > \frac{L_{LINE}}{(C_{IN} + C_{IN\_EXT}) \bullet \left| r_{EQ\_IN} \right|} \quad (1)$$

$$R_{LINE} << \left| r_{EQ\_IN} \right| \quad (2)$$

Notice that the local high-performance ceramic input capacitors should be included for this purpose. Equation 2 means that the line source impedance should be <10% of the regulator dynamic input resistance r_{EQ_IN}. for best performance, but the line source impedance must <50% of r_{EQ_IN}. However, R_{LINE} cannot be made arbitrarily low otherwise Equation 1 is violated and the system will show instability, due to under-damped RLC input network.

Input Filter case 2; inductive source and internal, external input decoupling capacitance with significant $R_{C_{IN\_EXT}}$ ESR (i.e., electrolytic type)

In order to simplify the analysis in this case, the input source impedance can be modeled as a simple inductor L_{LINE}. Notice that, the internal high-performance ceramic capacitors C_{IN} directly at the input of the DCM should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$\left| r_{EQ\_IN} \right| > R_{C_{IN\_EXT}} \quad (3)$$

$$\frac{L_{LINE}}{(C_{IN\_EXT} \bullet R_{C_{IN\_EXT}})} < \left| r_{EQ\_IN} \right| \quad (4)$$

Equation 4 shows that if the aggregate ESR is too small – for example by using only high-Q ceramic input capacitors (C_{IN_EXT}) – the system will be under-damped and may not be stable. As with Equation 2 above, a decade of margin in satisfying Equation 3 is preferred, but an octave of margin is considered the minimum.

Additional information can be found in the filter design application note AN:023. Also, refer to the Vicor online input filter design tool to ensure input stability. Lastly, consider the DCM maximum input voltage slew rate dV_{IN}/dt, which is needed to prevent overstress to input stage components in the module. Additional circuitry may be required at the DCM input if the filter solution can exceed that slew rate.

Input Fuse Recommendations

A fuse should be incorporated at the input to the DCM, in series with the +IN pin. A 30A or smaller input fuse (Littelfuse® Nano2® 456 Series) is required to comply with safety agency conditions of acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application.

Thermal Design

Figure 23 shows a thermal impedance model that can predict the temperature of the hottest internal components for a given line operating condition at nominal trim. The circuit model identifies groups of heat flow paths through the package and pins, and assumes each group is isothermal. In order to exclude a group of thermal resistances from a given cooling solution, set the heat current through that group of paths to zero.

The DCM SM-ChiP™ product is molded and overplated. The large plated area on the package top and bottom is connected to PGND, but note that other package terminals also extend to the top and bottom surfaces of the case. If an electrically conductive heat sink or coldplate is used, then an electrically isolating thermal interface material is required to avoid a short circuit condition or unexpected connection to signal terminals.

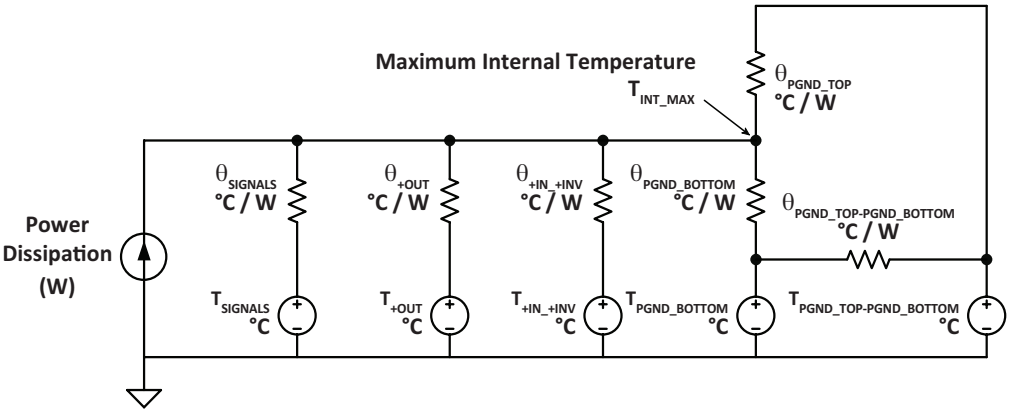


Figure 23 — *Thermal model*

Symbol	Thermal Impedance at Nominal Trim (°C / W)				Definition of Estimated Thermal Resistance
	Input Voltage				
	40V	44V	54V	60V	
$\theta_{SIGNALS}$	19				from the hottest component junction inside the DCM to the circuit board it is mounted on at SIGNALS
θ_{+OUT}	12				from the hottest component junction inside the DCM to the circuit board it is mounted on at +OUT
θ_{+IN_+INV}	24				from the hottest component junction inside the DCM to the circuit board it is mounted on at +IN_+INV
θ_{PGND_BOTTOM}	2.4	1.9	1.8	2.1	from the hottest component junction inside the DCM to the circuit board it is mounted on at PGND_BOTTOM
θ_{PGND_TOP}	1.9	1.6	1.4	2.3	from the hottest component junction inside the DCM to the circuit board it is mounted on at PGND_TOP
$\theta_{PGND\_TOP-PGND\_BOTTOM}$	7.9	6.4	9.3	3.6	between PGND_TOP and PGND_BOTTOM

Table 1 — *Thermal impedance*

Figure 24 — *Thermal model boundary conditions; area defined as shaded*

Thermal Design — Power Dissipation

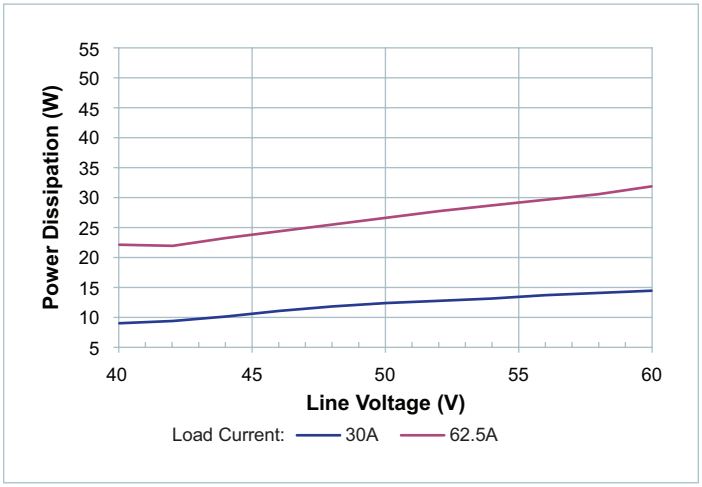


Figure 25 — *Power dissipation vs. line voltage, low trim at 25°C case temperature*

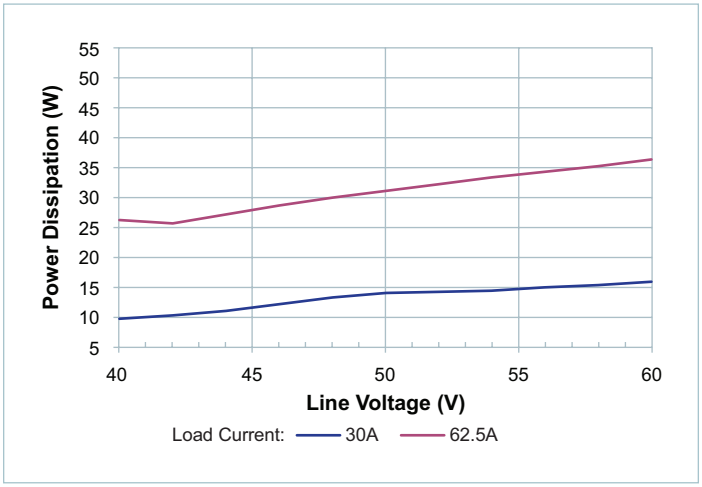


Figure 26 — *Power dissipation vs. line voltage, low trim at 100°C case temperature*

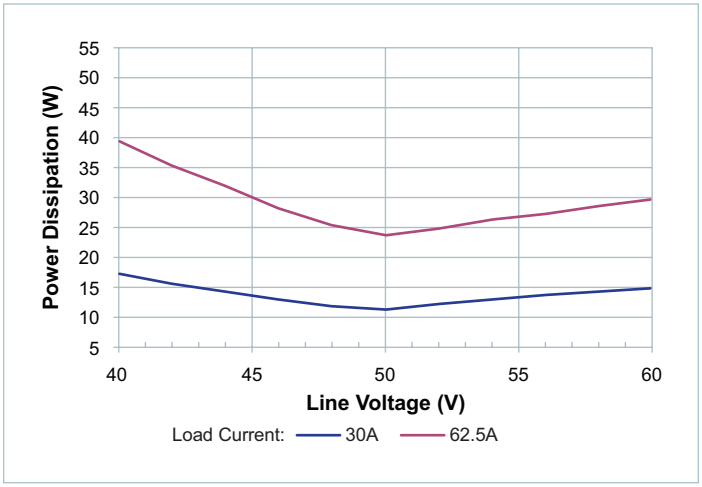


Figure 27 — *Power dissipation vs. line voltage, nominal trim at 25°C case temperature*

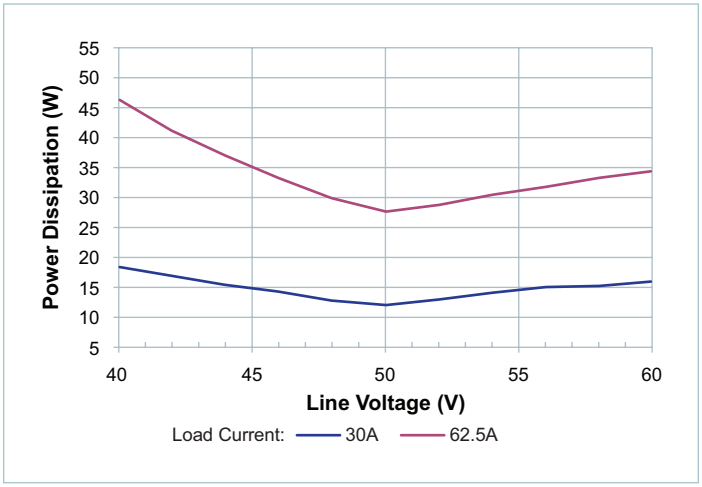


Figure 28 — *Power dissipation vs. line voltage, nominal trim at 100°C case temperature*

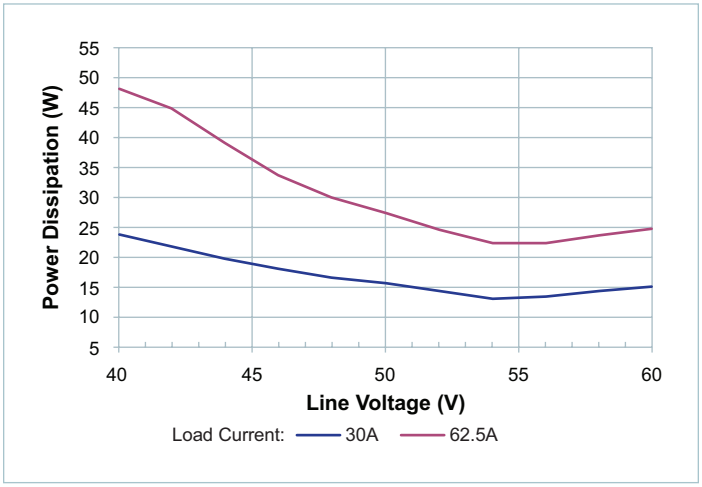


Figure 29 — *Power dissipation vs. line voltage, high trim at 25°C case temperature*

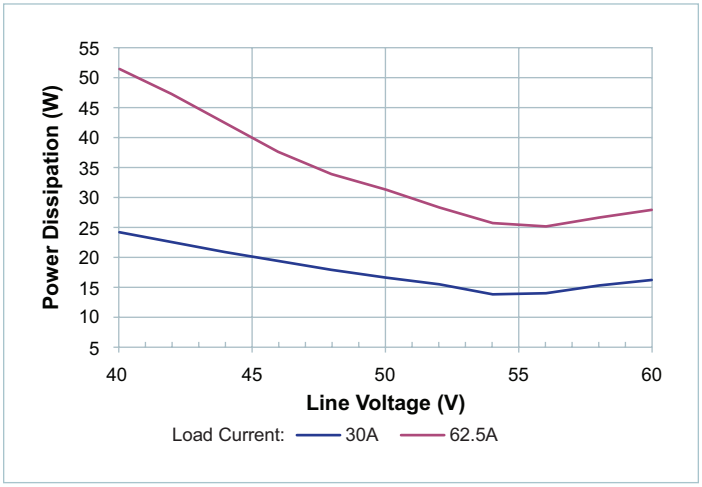


Figure 30 — *Power dissipation vs. line voltage, high trim at 100°C case temperature*

Additional PCB Layout Considerations

DCM output capacitance is needed to bypass the high-frequency ripple at its source. The amount of capacitance varies by design and should be distributed as shown in the diagram.

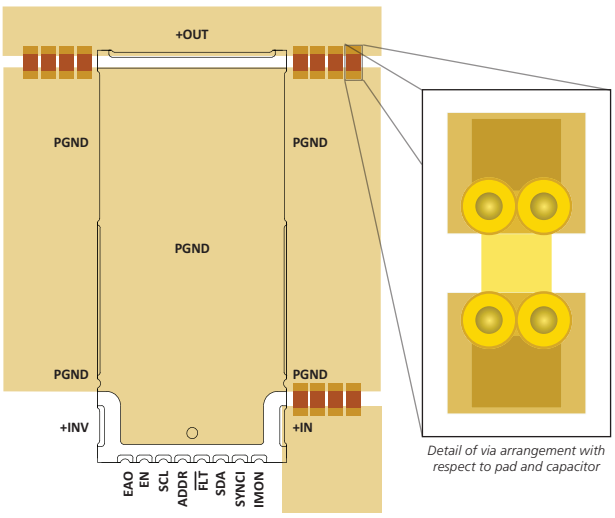


Figure 31 — *Recommended positioning of external capacitance relative to +OUT and PGND pins*

The mechanical drawings in later sections include the recommended land pattern to use when creating a PCB footprint. The recommend footprint pad is intentionally narrower than the actual product pin. This allows room for the pick-and-place machine worst-case placement tolerances. The worst case is a package pin exactly aligned with the inner edges of footprint pad.

If the product is water washed post assembly, then the PGND circular thermal pads under the product must be copper-defined.

If no-clean solder flux is used during assembly, then PGND thermal pad apertures may be solder-mask-defined.

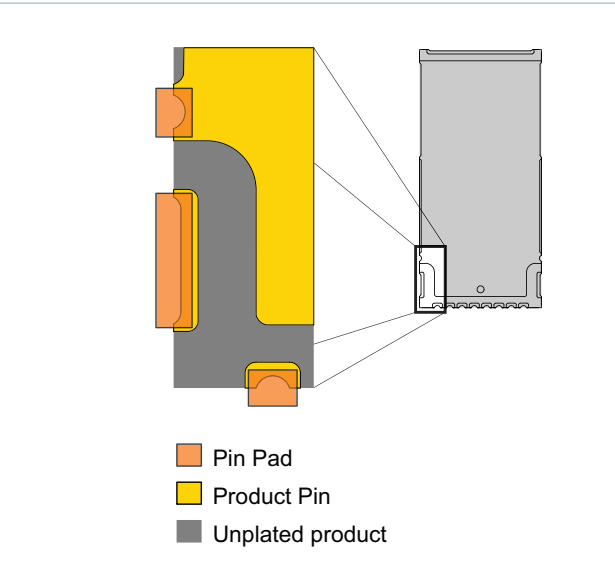


Figure 32 — *Product drawing vs. recommended land pattern*

Parallel Operation for High Power Arrays

Loads that exceed the rated current or power of a single DCM can be powered by an array of DCMs, with array sizes up to n_{ARRAY} max modules. A properly configured array of n DCMs provides the rated power or current of a single module times n, with no electrical de-rating required.

At the schematic level, a DCM array is configured by creating setting a unique address for each DCM, directly interconnecting the control pins, and creating a shared signal ground (SGND_COMMON) node which serves as the reference for those control pins.

- Each of the n DCMs should have a SGND_x node created by way of a Kelvin connection point at the DCM's PGND connection.
- A SGND_COMMON node is created by connecting to each of the n SGND_x nodes through a 1R resistor. The purpose of the resistor is to limit current flow in the SGND_x nodes in case of small voltage differences between DCM PGND potentials.
- The control pins EN, $\overline{\text{FLT}}$, SDA and SCL should all be directly interconnected
- The SGND_COMMON node serves as the reference for all sub-circuitry that interfaces with the shared EN, $\overline{\text{FLT}}$, SDA and SCL nodes, and the ADDR resistors for each DCM should connect to it.

For power connections in an array, each DCM should still have dedicated multi-layer chip capacitors at the input and output. The DCM +OUT terminals must be directly connected together. The DCM +IN terminals are not directly connected, but instead each has its own dedicated fuse and input filter. The fuse and filter of each DCM in the array must be powered from the same voltage source; different input voltages are not permitted.

PCB layout for an array of DCMs builds off of the recommended layout shown in Figure 31. The DCMs should be placed in close proximity so that interconnected control signals can be short, which improves stray capacitance and pickup of noise. However DCMs must still be separated sufficiently to permit adequate cooling avoid excess internal temperatures. If the PCB provides the dominant cooling path for heat to flow from the modules, physical separation of modules becomes more important. PGND should be carried on contiguous plane layers to optimize effectiveness of high-frequency bypassing and filtering. The +OUT connection should also be on plane layers to minimize inductance between DCM outputs. Control signal route lengths should be minimized but they should not be routed underneath the DCM body. This is especially true for EAO.

PMBus Interface

Refer to "PMBus Power System Management Protocol Specification Revision 1.3, Part I and II" for complete PMBus® specifications details visit http://pmbus.org

The DCM is a PMBus child and will respond only to host commands listed in this sections. Dedicated address (ADDR), Clock (SCL) and data (SDA) pins are available; the optional SMBALERT# signal is not supported.

Device Address

The DCM PMBus address can be set using a 1% resistor from the ADDR pin to ground. The following table lists the available addresses and the corresponding resistor value to use.

The DCM does not support SMBus Address Resolution protocol. The address is set at initial power up and then remains fixed until power is removed.

7-bit Hex Address	Resistor Value, 1% (kΩ)
51h	0.0
52h	12.1
53h	20.0
54h	28.0
55h	35.7
56h	44.2
57h	52.3
58h	open

Restricted Address

The DCM also responds to address 0x50, but this address is for factory use only and cannot be used for any Supported Command in the list below. This address is fixed and cannot be changed, and so care must be taken that no other device on the bus uses address 0x50 in order to avoid address collisions.

PMBus Command Definitions

A summary of the PMBus commands supported by the DCM are described in the following sections.

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted again once cleared, except for "$\overline{\text{FLT}}$ falling edge" bit, which is edge-triggered. All faults are latched once asserted in the DCM. Registered faults will not be cleared when DCM is powertrain is disabled through the $\overline{\text{FLT}}$ or EN pin.

STORE USER CODE Command (17h)

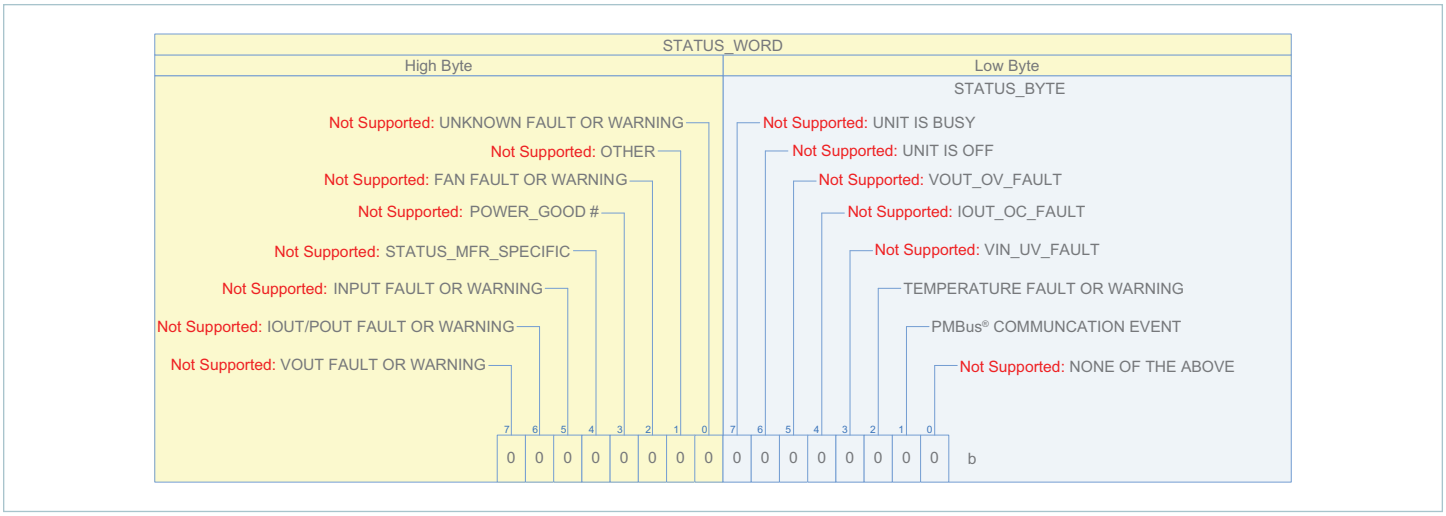
STORE_USER_CODE can save the VOUT_COMMAND value to non-volatile memory. At subsequent power ups, this stored value is used for the DCM output voltage trim set point.

The data for STORE_USER_CODE is the command code to be stored; the DCM can only accept command code VOUT_COMMAND (20h) to be stored.

STORE_USER_CODE can only be used $N_{STORE\_USER\_CODE}$ times before all non-volatile memory is consumed.

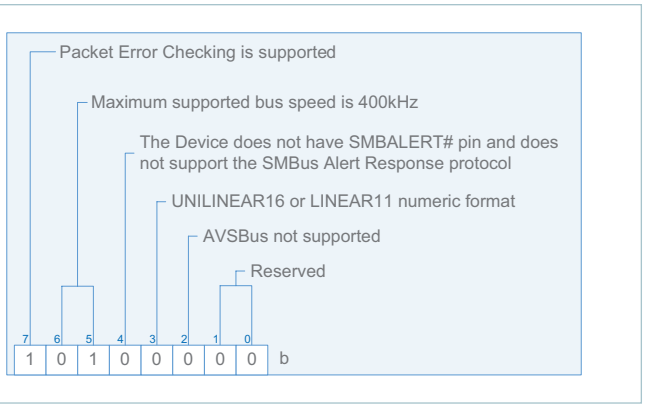
Supported Command List and Supported Commands Transaction Type

Command Name	Command Code	Function	Default Data Content	SMBus Write Transaction	SMBus Read Transaction	Number Data Bytes	Data Format
CLEAR_FAULTS	03h	Clear fault status register	n/a	Send Byte	n/a	0	bit
STORE_USER_CODE	17h	Can write VOUT_COMMAND to NV memory	n/a	Write Byte	n/a	1	bit
CAPABILITY	19h	DCM key capabilities set by factory	28h	n/a	Read Byte	1	bit
VOUT_MODE	20h	Format for VOUT_COMMAND	17h	n/a	Read Byte	1	bit
VOUT_COMMAND	21h	Set DCM output voltage	1866h	Write Word	Read Word	2	ULINEAR16
STATUS_BYTE	78h	Fault Readback	n/a	n/a	Read Byte	1	bit
STATUS_WORD	79h	Generic Fault Readback	n/a	n/a	Read Word	2	bit
READ_VIN	88h	DCM Input Voltage	n/a	n/a	Read Word	2	LINEAR11
READ_VOUT	8Bh	Regulator Output Voltage at +INV pin	n/a	n/a	Read Word	2	ULINEAR16
READ_TEMPERATURE_1	8Dh	DCM Temperature at Regulator Controller	n/a	n/a	Read Word	2	LINEAR11
MFR_ID	99h	Manufacturer ID	"VI"	n/a	Block Read	2	ASCII
MFR_VOUT_MIN	A4h	Minimum rated value for Vout set	0C00h	n/a	Read Word	2	ULINEAR16
MFR_VOUT_MAX	A5h	Maximum rated value for Vout set	1C19h	n/a	Read Word	2	ULINEAR16
MFR_STATUS_FAULTS	F0h	DCM Specific Faults	n/a	n/a	READ 32	4	bit



CAPABILITY Command (19h)

The DCM returns a default value of A0h. This value indicates that the Packet Error Checking (PEC) is supported, PMBus® frequency is up to 400kHz, the SMBALERT# bit is not supported and that the numeric data can be LINEAR11 or ULINEAR16. See supported data command table indicating each command respective data reporting format.



VOUT_MODE Command (20h)

The DCM VOUT_MODE command is read only. Set to a default value of 17h.

VOUT_COMMAND Command (21h)

VOUT_COMMAND causes the DCM to set the output voltage to the commanded value. Format is ULINEAR16 with –9 exponent, high byte, low byte. When multiple DCMs are used in parallel to create a high-power array, the group command protocol should be used when using VOUT_COMMAND to change the output voltage. The group command protocol will cause all DCMs in the array to wait until the last unit receives the VOUT_COMMAND before they all update their output voltage setting. Not using the group command protocol can lead to nuisance detection of $\%_{EAIN\_HI}$ faults for units which are programmed lower than the others in the array.

STATUS_BYTE (78h) and STATUS_WORD (79h)

Although the DCM powertrain will self-restart once fault conditions are cleared, all fault or warning flags, if set, will remain asserted until cleared by the host or once DCM input power is removed. This includes overtemperature warning and communication faults.

STATUS_WORD and STATUS_BYTE can be cleared by sending CLEAR_FAULTS (03h) command.

The TEMPERATURE FAULT but reflects that an overtemperature shut down of the Stage 1 ZVS buck-boost occurred.

The PMBus COMMUNICATION EVENT bit is set when a communication fault occurs. See the PMBus Communication Fault section for details.

READ_VIN Command (88h)

READ_VIN returns the input voltage telemetry in LINEAR11 format.

READ_VOUT Command (8Bh)

READ_VOUT returns the output voltage telemetry in ULINEAR16 format. Refer to the PMBus Power System Management Protocol Specification – Part II – Revision 1.3 for details on reported LINEAR11 and ULINEAR16 numeric format. READ_VOUT telemetry is taken from the +INV node, and so it will nominally read 4x the actual V_{OUT} during operation. Also note that there is a diode-clamp path from +OUT back to +INV, and so when the module is disabled or the stage 2 current multiplier is stopped, READ_VOUT will report a value equal to +OUT minus approximately 0.6V.

READ_TEMPERATURE_1 (8Dh)

READ_TEMPERATURE_1 returns the measured temperature at the stage 1 ZVS buck-boost controller. This temperature can be used as a relative gauge to the operating temperature of one internal area of the module.

READ_TEMPERATURE_1 is not sufficient to design or validate any module-level thermal solution. Thermal design must use the module power dissipation and thermal resistance model to ensure that all areas of the module internal circuitry are kept below the maximum operating temperature.

MFR_ID (99h)

This read-only command will return "VI" as two ASCII bytes, indicating the manufacturer Vicor Corporation.

MFR_VOUT_MIN (A4h), MFR_VOUT_MAX (A5h)

These read-only commands return the functional range of the VOUT_COMMAND. As with the VOUT_COMMAND, their format is ULINEAR16 with an exponent of –9. Note that the functional range guarantees that the module output voltage can be trimmed well beyond the rated V_{OUT} range.

MFR_STATUS_FAULTS (F0h)

This command returns four bytes; the first three are used and are defined in the table below.

Bit	Data Byte Readback Order			
	0	1	2	3
7	EN_LOW	unsupported	0	unsupported
6	VOUT_NEG	unsupported	0	unsupported
5	VOUT_OVP	EAIN_HI	0	unsupported
4	VIN_OVLO	Q1_FIL	0	unsupported
3	VIN_UVLO	Q3_SIL	0	unsupported
2	unsupported	Q3_FIL	unsupported	unsupported
1	unsupported	EAO_OVERLOAD	unsupported	unsupported
0	unsupported	$\overline{\text{FLT}}$_FALLING_EDGE [c]	OVERTEMPERATURE	unsupported

[c] Sets on the falling edge of the $\overline{\text{FLT}}$ pin. This occurs when any other fault type occurs. However, if this bit is set with no other fault type, then it indicates that a fault was detected by the current-multiplier stage, for example Overcurrent.

All fault or warning flags, if set, will remain asserted until cleared by the host using a CLEAR_FAULTS (03h) command. CLEAR_FAULTS should be issued after power is initially applied to clear any fault flags which are set during module initialization.

PMBus Communication Fault

Module Behavior

Corrupted data, unrecognized commands or other PMBus® protocol violations have no impact on powertrain functionality.

PMBus Reporting Characteristics

The below tables summarize data transmission and data content faults as implemented in the DCM.

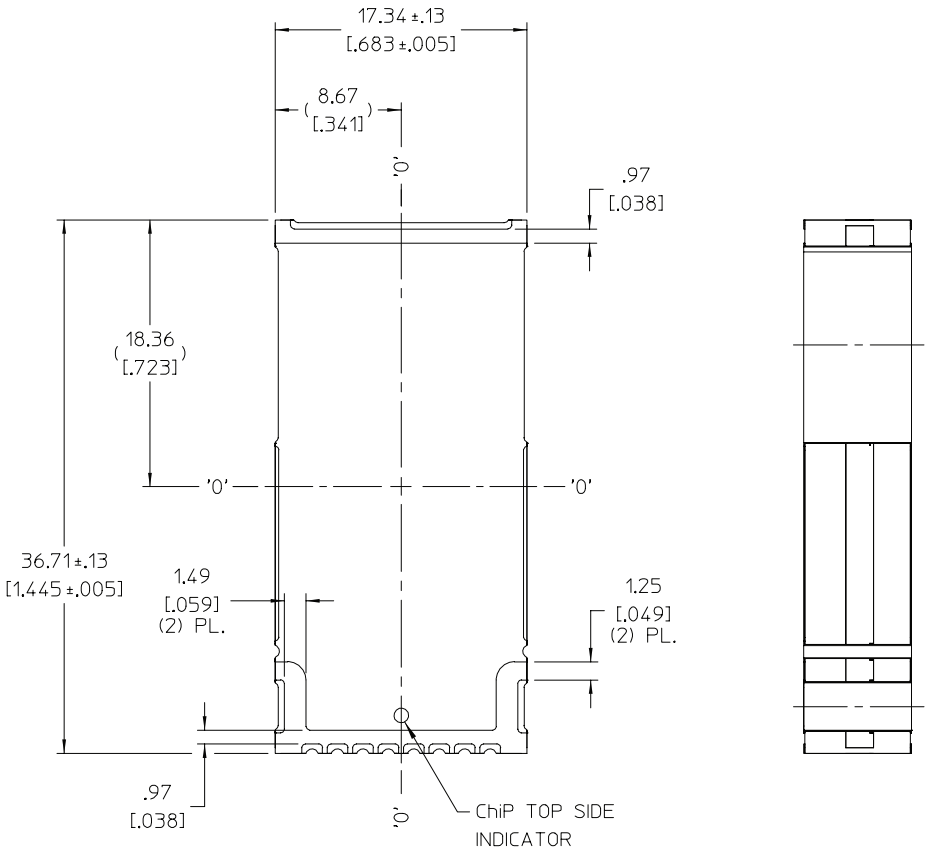
Section	Description	STATUS_BYTE	Notes
		CML	
10.8.1	Corrupted data	X	PEC failure
10.8.2	Sending too few bits		Device will ignore transmission
10.8.3	Reading too few bits		No response
10.8.4	Host sends or reads too few bytes	X	CML set on writes only
10.8.5	Host sends too many bytes	X	
10.8.6	Reading too many bytes		Read will report old data
10.8.7	Device busy		Clock stretch prior to ACK

Table 2 — *Data transmission faults*

Section	Description	STATUS_BYTE	Notes
		CML	
10.9.1	Improperly set read bit in the address byte		Not interpreted as a fault; Device will respond normally
10.9.2	Unsupported command code	X	
10.9.3	Invalid or unsupported data	X	
10.9.4	Data out of range		No response
10.9.5	Reserved bits		No response Not a fault

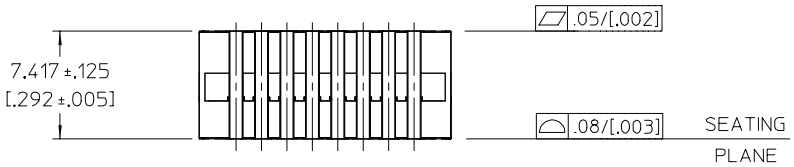
Table 3 — *Data content faults*

Product Outline Drawing – Top View



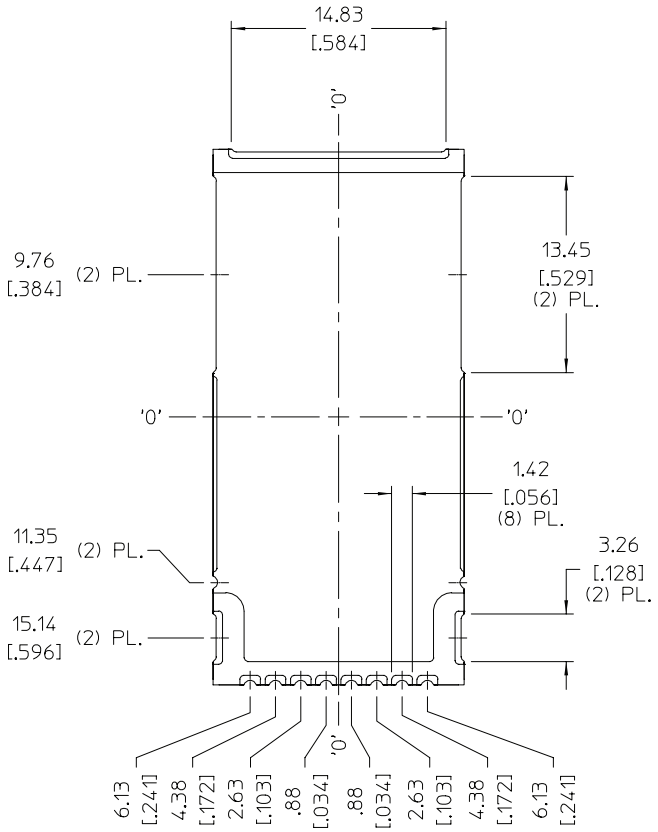
TOP VIEW (COMPONENT SIDE)

3717 DCM



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE MM [INCH]

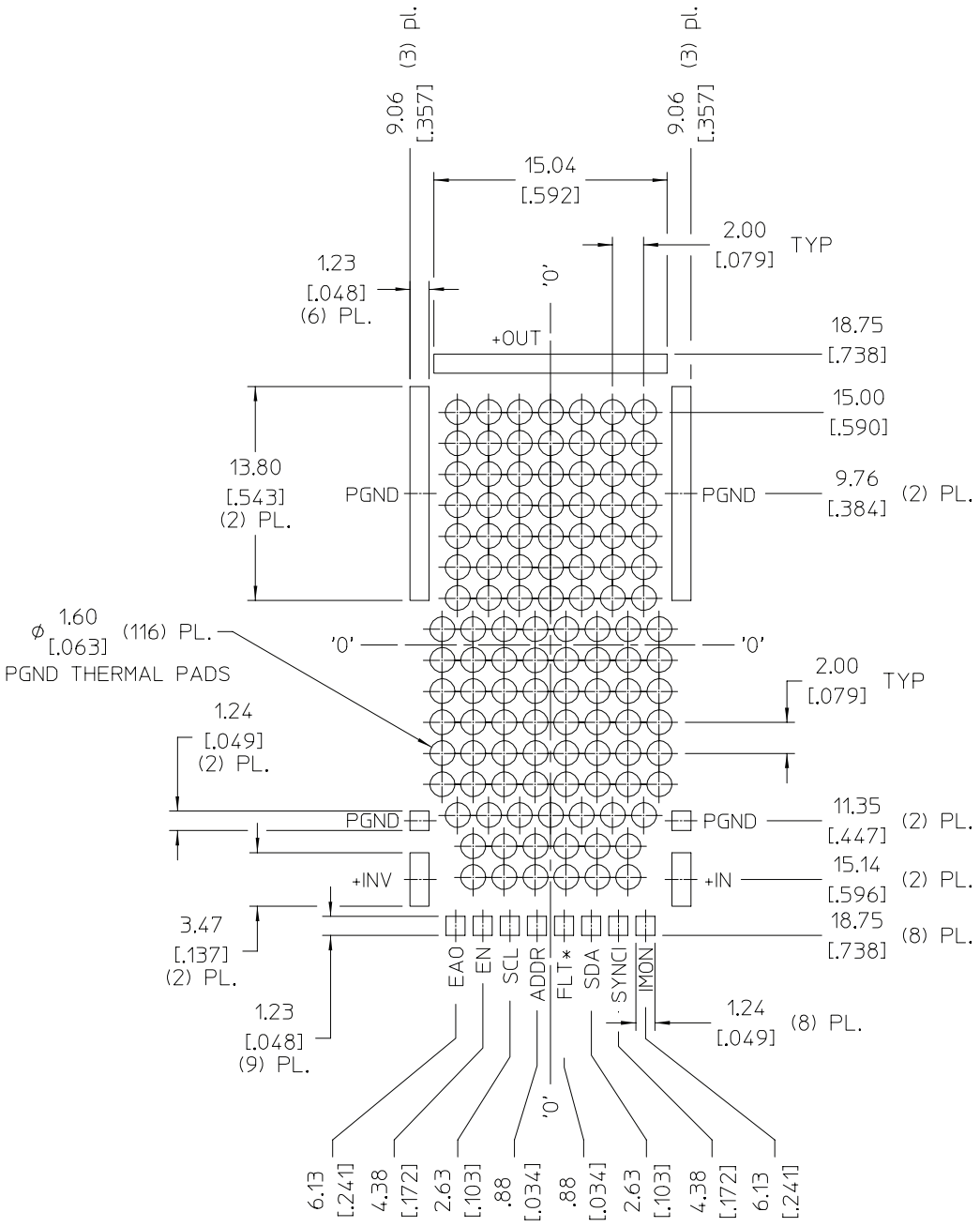
Product Outline Drawing – Bottom View



BOTTOM VIEW

3717 DCM

Recommended Land Pattern



RECOMMENDED LAND PATTERN,

3717 DCM

(COMPONENT SIDE)

Revision History

Revision	Date	Description	Page Number(s)
1.0	02/10/20	Initial release	n/a
1.1	04/23/20	Added typical applications diagrams Revised minimum temperature to –20°C Added functional block diagram Updated to add performance data Added state and timing diagrams Revised and reordered functional description and design guidelines	2 4, 6, 7, 8 5 10 – 12, 21 16 – 18 14, 15, 19
1.2	08/11/20	Updated terminology	8, 24
1.3	09/03/20	Updated typical application diagrams Updated electrical specifications Updated $\overline{FLT}$ signal characteristics	2 6 9
1.4	10/23/20	Modified short circuit shut down specification	8, 16, 17, 19, 26
1.5	02/02/21	Revised ESD charged device specification and MTBF values Bold type removed from T_{INT} = 25°C switching frequency spec Typo correction in input fuse recommendations	4 6 20

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