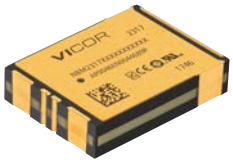
NBM™ Bus Converter
NBM2317S60D1565T0R



Non-Isolated, Fixed-Ratio Bidirectional DC-DC Converter

Features & Benefits

- 97.9% peak efficiency
- Bidirectional start up and steady-state operation
- Up to 6.4kW/in^3 power density
- Maximum continuous output power: 800W
  - Up to 1kW, 2ms peak power capability
- Rated output current, step-down operation
  - 65A continuous
  - 100A transient, up to 2ms
- Rated output current, step-up operation
  - 16.25A continuous
  - 25A transient, up to 2ms
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal shut down

Typical Applications

- DC Power Distribution
- High-Performance Computing Systems (HPC)
- Mild Hybrid and Autonomous Vehicles
- Automated Test Equipment (ATE)
- Industrial Systems
- High-Density Power Supplies
- Communications Systems
- Transportation
- Bidirectional DC Energy Storage

Product Ratings (Step-Down Operation)	
V_{HI} = 54V (40 – 60V)	I_{LO} = up to 65A
V_{LO} = 13.5V (10 – 15V) (NO LOAD)	K = 1/4

Product Description

The NBM2317S60D1565T0R is a high-efficiency Non-Isolated Bus Converter operating from a 40 to 60V_{DC} high-side voltage bus to deliver a ratiometric low-side voltage from 10 to 15V_{DC}.

The NBM2317S60D1565T0R offers low noise, fast transient response, and industry-leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a PoL regulator to be located at the high side of the NBM. With a high-side to low-side K factor of 1/4, that capacitance value can be reduced by a factor of 16x, resulting in savings of board area, material and total system cost.

Leveraging the thermal and density benefits of Vicor SM-ChiP packaging technology, the NBM offers flexible thermal management options with very low top- and bottom-side thermal impedances. Thermally-adept SM-ChiP-based power components enable customers to achieve low-cost power system solutions with previously unattainable system size, weight and efficiency attributes quickly and predictably.

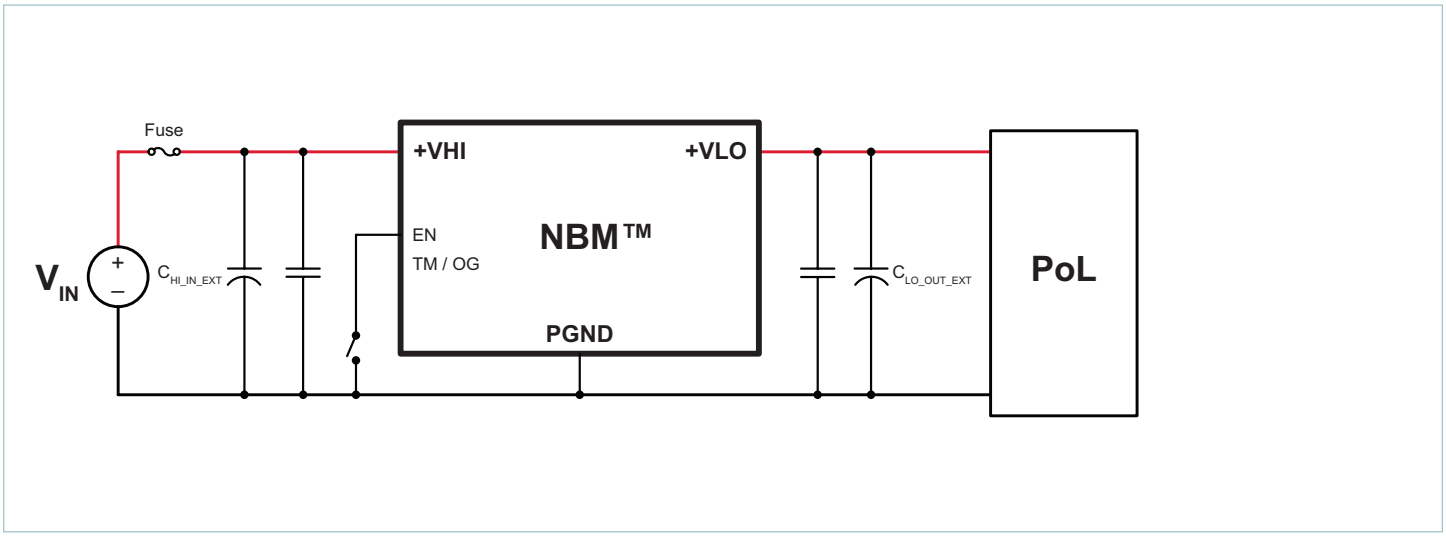
The NBM non-isolated topology allows bidirectional start up and steady-state operation and provides bidirectional fault detection and shut down.

Package Information

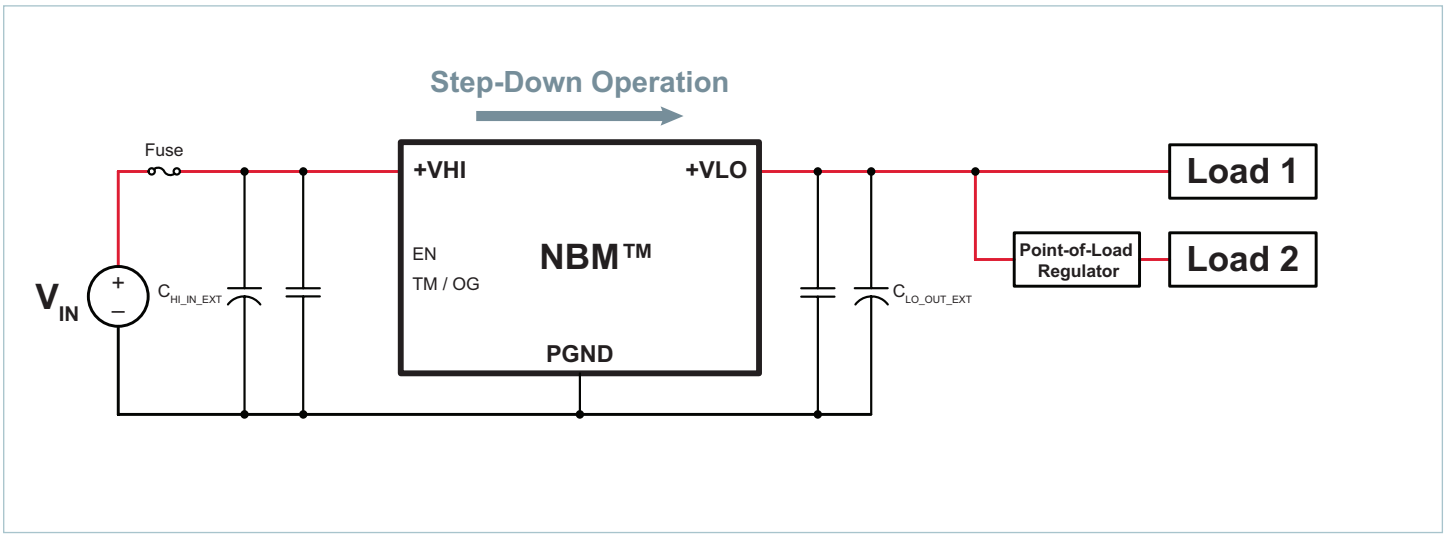
- Thermally-Adept SM-ChiP™
- 22.8 x 17.3 x 5.2mm
  [0.90 x 0.68 x 0.20in]
- Weight: 8.7g

Note: Product images may not highlight current product markings.

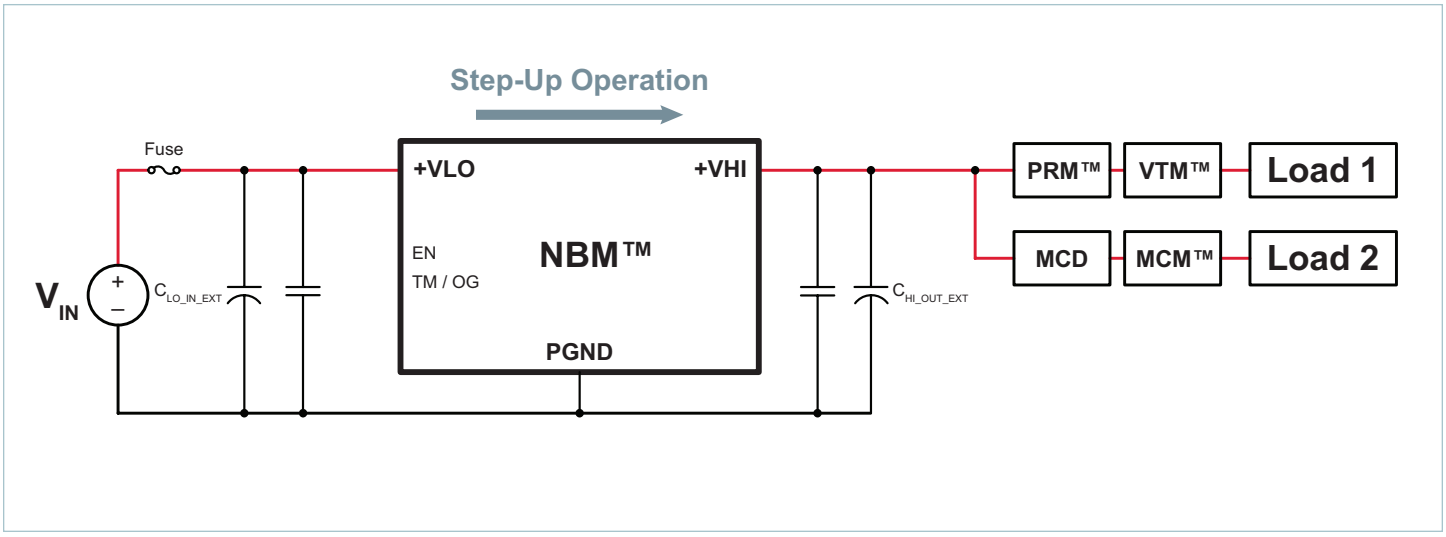
Typical Applications



NBM2317S60D1565T0R + point-of-load

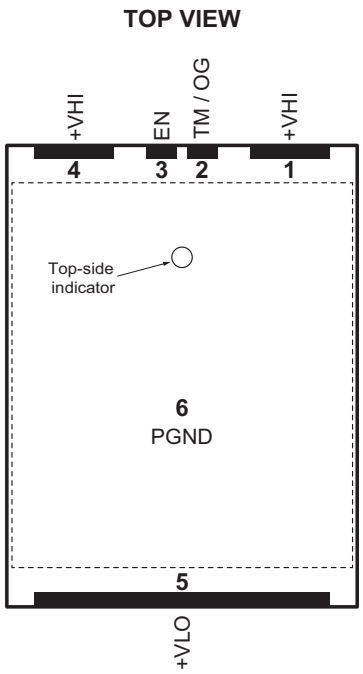


NBM2317S60D1565T0R in step-down operation powering point-of-load regulator and direct load



NBM2317S60D1565T0R in step-up operation powering PRM + VTM and MCD + MCM

Terminal Configuration



NBM2317 SM-ChiP™

Terminal Descriptions

Terminal Number	Signal Name	Type	Function
1, 4	+VHI	HIGH SIDE POWER	High-side power positive terminals
2	TM / OG	OUTPUT	Temperature Monitor and Output Good
3	EN	INPUT	NBM enable/disable control
5	+VLO	LOW SIDE POWER	Low-side power positive terminal
6	PGND	POWER RETURN	Common negative high-side and low-side power return terminal

Part Ordering Information

Part Number	Temperature Grade	Option	Tray Size
NBM2317S60D1565**T0R**	**T** = –40 to 125°C	**0R** = Reversible Analog Control	55 parts per tray

All products shipped in JEDEC standard high-profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

Storage and Handling Information

Note: For compressive loading refer to Application Note AN:036, "Recommendations for Maximum Compressive Force of Heat Sinks."

Attribute	Comments	Specification
Storage Temperature Range	T-Grade	–40 to 125°C
Operating Internal Temperature Range (T_{INT})	T-Grade	–40 to 125°C
Weight		8.67g
Package Plating		75µm copper with ENiG surface finish
MSL Rating		MSL4, 245°C maximum reflow temperature
ESD Rating	Human Body Model ESDA / JEDEC JDS-001-2012	Class 1C, 1kV to < 2kV
	Charged Device Model JESD22-C101-E	CLASS II, 200V to < 500V

Reliability and Agency Approvals

Attribute	Comments	Value	Unit
MTBF	Telcordia Issue 2, Method I Case 3; 25°C Ground Benign, Controlled	15	MHrs
	MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer	6.41	
Agency Approvals/Standards			
	cTÜVus EN 62368-1		
	CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable		

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+VHI to PGND		–1	70	V
VHI or VLO Slew Rate	Operational		1	V/µs
+VLO to PGND		–1	17.5	V
TM / OG to PGND		–0.3	5.7	V
EN to PGND			5.7	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Step-Down Operation (High-Voltage Side to Low-Voltage Side)						
High-Side Input Voltage Range	V_{HI_DC}	Continuous, operating	**40**	54	**60**	V
Controller Initialization	$V_{C\text{-}ACTIVE}$	V_{HI_DC} voltage where controller is initialized	5			V
High-Side Input Quiescent Current	I_{HI_Q}	Disabled, EN low, V_{HI_DC} = 54V		5.4		mA
		$T_{INTERNAL}$ ≤ 100°C			8	
No Load Power Dissipation	P_{HI_NL}	V_{HI_DC} = 54V		4.2	7	W
			2		**9.3**	
		V_{HI_DC} = 40 – 60V			9.3	
					12.5	
High-Side Input Inrush Current Peak	$I_{HI\_INR\_PK}$	V_{HI_DC} = 54V, C_{LO_EXT} = 3000µF, no load		2.1		A
		$T_{INTERNAL}$ ≤ 100°C			**5**	
DC High-Side Input Current	$I_{HI\_IN\_DC}$	At $I_{LO\_OUT\_DC}$ = 65A, $T_{INTERNAL}$ ≤ 100°C			17	A
Transformation Ratio	K	High voltage side to low voltage side, K = V_{LO_DC} / V_{HI_DC}, at no load		1/4		V/V
Low-Side Output Current	$I_{LO\_OUT\_DC}$	Continuous; 40V ≤ V_{HI_DC} ≤ 54V			65	A
	$I_{LO\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $I_{LO\_OUT\_AVG}$ ≤ 50% rated $I_{LO\_OUT\_DC}$			100	
Low-Side Output Power	$P_{LO\_OUT\_DC}$	Continuous; 54V < V_{HI_DC} ≤ 60V			800	W
	$P_{LO\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $P_{LO\_OUT\_AVG}$ ≤ 50% rated $P_{LO\_OUT\_DC}$			1000	
Efficiency (Ambient)	η_{AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 65A	96.6	97.3		%
		V_{HI_DC} = 40 – 54V, $I_{LO\_OUT\_DC}$ = 65A	95.6			
		V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 32.5A	97.3	97.8		
Efficiency (Hot)	η_{HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 65A	96.1	96.6		%
		V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 32.5A	97.3	97.7		
Efficiency (Over Load Range)	$\eta_{20\%}$	13A < $I_{LO\_OUT\_DC}$ < 65A	**94.8**			%
Low-Side Output Resistance	R_{LO_COLD}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 65A, $T_{INTERNAL}$ = –40°C	2.6	3.4	4.2	mΩ
	R_{LO_AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 65A	3.3	4.1	5.0	
	R_{LO_HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 65A, $T_{INTERNAL}$ = 100°C	4.1	5.0	5.9	
Switching Frequency	F_{SW}	Low-side voltage ripple frequency = 2x F_{SW}		1.74		MHz
Low-Side Output Voltage Ripple	$V_{LO\_OUT\_PP}$	$C_{LO\_OUT\_EXT}$ = 0µF, $I_{LO\_OUT\_DC}$ = 65A, V_{HI_DC} = 54V, 20MHz BW		170		mV
		$T_{INTERNAL}$ ≤ 100°C			270	
Effective High-Side Input Capacitance (Internal)	C_{HI_INT}	Effective value at 54V_{HI_DC}		2.9		µF
Effective Low-Side Output Capacitance (Internal)	C_{LO_INT}	Effective value at 13.5V_{LO_DC}		30		µF
Rated Low-Side Output Capacitance (External)	$C_{LO\_OUT\_EXT}$	Excessive capacitance may drive module into short circuit fault			**3000**	µF
	$C_{LO\_OUT\_AEXT}$	Parallel array operation; $C_{LO\_OUT\_AEXT}$ Max = N • 0.5 • $C_{LO\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				µF

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Fault Shut-Down Specification – Step-Down Operation (High-Voltage Side to Low-Voltage Side)						
Auto Restart Time	$t_{AUTO\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given $V_{HI\_DC} > V_{HI\_UVLO+}$	**904**	970	**1035**	ms
High-Side Input Overvoltage Lockout Threshold	V_{HI_OVLO+}			66.9	**68**	V
High-Side Input Overvoltage Recovery Threshold	$V_{HI\_OVLO–}$		**60**	65.5		V
High-Side Input Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			1.4		V
High-Side Input Overvoltage Lockout Response Time	t_{HI_OVLO}			1		µs
High-Side Input Undervoltage Lockout Threshold	$V_{HI\_UVLO–}$		**26**	28.7		V
High-Side Input Undervoltage Recovery Threshold	V_{HI_UVLO+}			30.5	**40**	V
High-Side Input Undervoltage Lockout Hysteresis	$V_{HI\_UVLO\_HYST}$			2.2		V
High-Side Input Undervoltage Lockout Response Time	t_{HI_UVLO}			1		µs
Input-to-Output Undervoltage Start-Up Delay	$t_{HI\_TO\_LO\_DELAY}$	From $V_{HI\_DC} = V_{HI\_UVLO+}$ to powertrain active, EN floating (i.e., one-time start-up delay from application of V_{HI_DC} to V_{LO_DC})		150	225	µs
Low-Side Output Soft-Start Ramp Time	$t_{LO\_SOFT\_START}$	$C_{LO\_OUT\_EXT}$ = 0µF, V_{HI_DC} = 54V, no load; from powertrain active; fast current limit fault detection disabled during soft-start		250		µs
		$C_{LO\_OUT\_EXT}$ = 3000µF, V_{HI_DC} = 54V, no load; from powertrain active; fast current limit fault detection disabled during soft-start			**13**	ms
Low-Side Output Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**66**	75	**95**	A
Low-Side Output Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$		2		4.3	ms
Low-Side Output Short Circuit Fault Trip Threshold	$I_{LO\_OUT\_SCP}$		**110**			A
Low-Side Output Short Circuit Fault Response Time	$t_{LO\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC	**125**			°C
Overtemperature Recovery Threshold	$t_{OTP–}$		105	110	115	°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Step-Up Operation (Low-Voltage Side to High-Voltage Side)						
Low-Side Input Voltage Range	V_{LO_DC}	Continuous, operating	**10**	13.5	**15**	V
Controller Initialization	$V_{C\text{-}ACTIVE}$	V_{LO_DC} voltage where controller is initialized	5			V
Low-Side Input Quiescent Current	I_{LO_Q}	Disabled, EN low, V_{LO_DC} = 13.5V		19		mA
		$T_{INTERNAL}$ ≤ 100°C			25	
No-Load Power Dissipation	P_{LO_NL}	V_{LO_DC} = 13.5V		4.2	7	W
			3		**11**	
		V_{LO_DC} = 10 – 15V			8	
					14	
Low-Side Input Inrush Current Peak	$I_{LO\_INR\_PK}$	V_{LO_DC} = 15V, C_{HI_EXT} = 187.5µF, no load		8.4		A
		$T_{INTERNAL}$ ≤ 100°C			**20**	
DC Low-Side Input Current	$I_{LO\_IN\_DC}$	At $I_{HI\_OUT\_DC}$ = 16.25A, $T_{INTERNAL}$ ≤ 100°C			67	A
Transformation Ratio	K	Low-voltage side to high-voltage side, K = V_{HI_DC} / V_{LO_DC}, at no load		4		V/V
High-Side Output Current	$I_{HI\_OUT\_DC}$	Continuous; 10V ≤ V_{LO_DC} ≤ 13.5V			16.25	A
	$I_{HI\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $I_{HI\_OUT\_AVG}$ ≤ 50% rated $I_{HI\_OUT\_DC}$			25	
High-Side Output Power	$P_{HI\_OUT\_DC}$	Continuous; 13.5V < V_{LO_DC} ≤ 15V			800	W
	$P_{HI\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $P_{HI\_OUT\_AVG}$ ≤ 50% rated $P_{HI\_OUT\_DC}$			1000	
Efficiency (Ambient)	η_{AMB}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 16.25A	96.5	97.3		%
		V_{LO_DC} = 10 – 15V, $I_{HI\_OUT\_DC}$ = 16.25A	95.5			
		V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 8.125A	97.3	97.8		
Efficiency (Hot)	η_{HOT}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 16.25A	96.0	96.5		%
		V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 8.125A	97.3	97.7		
Efficiency (Over Load Range)	$\eta_{20\%}$	3.25A < $I_{HI\_OUT\_DC}$ < 16.25A	**94.8**			%
High-Side Output Resistance	R_{HI_COLD}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 16.25A, $T_{INTERNAL}$ = –40°C	50	65	80	mΩ
	R_{HI_AMB}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 16.25A	62	80	98	
	R_{HI_HOT}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 16.25A, $T_{INTERNAL}$ = 100°C	75	91	118	
Switching Frequency	F_{SW}	High-side output voltage ripple frequency = 2x F_{SW}		1.74		MHz
High-Side Output Voltage Ripple	$V_{HI\_OUT\_PP}$	$C_{HI\_OUT\_EXT}$ = 0µF, $I_{HI\_OUT\_DC}$ = 16.25A, V_{LO_DC} = 13.5V, 20MHz BW		370		mV
		$T_{INTERNAL}$ ≤ 100°C			**570**	
Effective Low-Side Input Capacitance (Internal)	C_{LO_INT}	Effective value at 13.5V_{LO_DC}		30		µF
Effective High-Side Output Capacitance (Internal)	C_{HI_INT}	Effective value at 54V_{HI_DC}		2.9		µF
Rated High-Side Output Capacitance (External)	$C_{HI\_OUT\_EXT}$	At start up with no load; excessive capacitance may prevent module start up			**187.5**	µF
	$C_{HI\_OUT\_AEXT}$	Parallel array operation; $C_{HI\_OUT\_AEXT}$ Max = N • 0.5 • $C_{HI\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				µF

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Fault Shut-Down Specification – Step-Up Operation (Low-Voltage Side to High-Voltage Side)						
Auto Restart Time	$t_{AUTO\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given $V_{LO\_DC} > V_{LO\_UVLO+}$	**904**	970	**1035**	ms
Low-Side Input Overvoltage Lockout Threshold	V_{LO_OVLO+}			16.7	**17.2**	V
Low-Side Input Overvoltage Recovery Threshold	$V_{LO\_OVLO–}$		**15.4**	15.8		V
Low-Side Input Overvoltage Lockout Hysteresis	$V_{LO\_OVLO\_HYST}$			0.4		V
Low-Side Input Overvoltage Lockout Response Time	t_{LO_OVLO}			1		µs
Low-Side Input Undervoltage Lockout Threshold	$V_{LO\_UVLO–}$		**7.5**	8.0		V
Low-Side Input Undervoltage Recovery Threshold	V_{LO_UVLO+}			9	**10**	V
Low-Side Input Undervoltage Lockout Hysteresis	$V_{LO\_UVLO\_HYST}$			0.1		V
Low-Side Input Undervoltage Lockout Response Time	t_{LO_UVLO}			1		µs
Input-to-Output Start-Up Delay	$t_{LO\_TO\_HI\_DELAY}$	From $V_{LO\_DC} = V_{LO\_UVLO+}$ to powertrain active, EN floating (i.e., one-time start-up delay from application of V_{LO_DC} to V_{HI_DC})		150	225	µs
High-Side Output Soft-Start Ramp Time	$t_{HI\_SOFT\_START}$	$C_{HI\_OUT\_EXT}$ = 0µF, V_{LO_DC} = 13.5V, no load; from powertrain active		400		µs
		$C_{HI\_OUT\_EXT}$ = 187.5µF, V_{HI_DC} = 13.5V, no load; from powertrain active			**13**	ms
High-Side Output Overcurrent Trip Threshold	$I_{HI\_OUT\_OCP}$	Powertrain stops switching; conduction path from low side to high side still exists through body diodes of powertrain MOSFETs [a]	**16.5**	18.75	**23.75**	A
High-Side Output Overcurrent Response Time Constant	$t_{HI\_OUT\_OCP}$		2		4.3	ms
Overtemperature Shut-Down Threshold	t_{OTP+}	Temperature sensor located inside controller IC	**125**			°C
Overtemperature Recovery Threshold	$t_{OTP–}$		105	110	115	°C
Undertemperature Shut-Down Threshold	t_{UTP}	Temperature sensor located inside controller IC			–45	°C

[a] Sustained current through body diodes can cause powertrain damage. See "start up and bidirectional operation" on page 15.

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Temperature Monitor / Output Good (TM / OG) [b]						
Powertrain active to TM / OG time	$t_{TM/OG}$	Powertrain active to TM / OG high, start up into 3000µF low-side output capacitance			**13**	ms
TM / OG Voltage Range	$V_{TM/OG}$		**1.60**		**2.82**	V
TM / OG Voltage Reference	V_{TM/OG_AMB}	T_J controller = 27°C	2.06	2.1	2.14	V
TM / OG Source Current	$I_{TM/OG}$	TM accuracy = ±5°C			**200**	µA
TM / OG Short Circuit Current	$I_{SC\_TM/OG}$	Maximum source current when pulled to ground externally			**2**	mA
TM / OG Gain	$A_{TM/OG}$			7		mV / °C
TM / OG Voltage Ripple	V_{TM/OG_PP}	$C_{TM/OG}$ = 0pF, V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 65A		100	**150**	mV
TM / OG Fault Response Time	$T_{FR\_TM/OG}$	From fault to TM / OG low		2		µs
TM / OG Voltage	V_{TM/OG_DIS}	TM/OG held low by internal controller		0.2		V
TM / OG Sinking Current	$I_{SINK\_TM/OG}$	Maximum current TM/OG can sink when pulled low by internal controller			**4**	mA
Enable / Disable Control (EN) [b]						
Enable Pull-Up Voltage	V_{EN}		**4.9**	5.1	**5.5**	V
EN Source (Current)	I_{EN_EN}		**20**	50		µA
Enable High Threshold	$V_{EN\_HIGH\_TH}$		**0.9**	1	**1.1**	V
Enable Low Threshold	$V_{EN\_LOW\_TH}$		0.7	0.8	**0.9**	V
EN Disable Duration	$t_{EN\_DIS\_t}$	Minimum time before attempting re-enable	**1**			s
Enable Threshold Hysteresis	$V_{EN\_HYST\_TH}$			200		mV
Enable to Powertrain Active Time	t_{EN_START}	V_{HI_DC} > V_{HI_UVLO+}, EN held low. Both conditions satisfied for time > $t_{HI\_TO\_LO\_DELAY}$			200	µs
EN Disable to V_{OUT} Time	t_{EN_DIS}			1.6	**3**	µs

[b] See signal terminal description section on page 15.

Operating Area

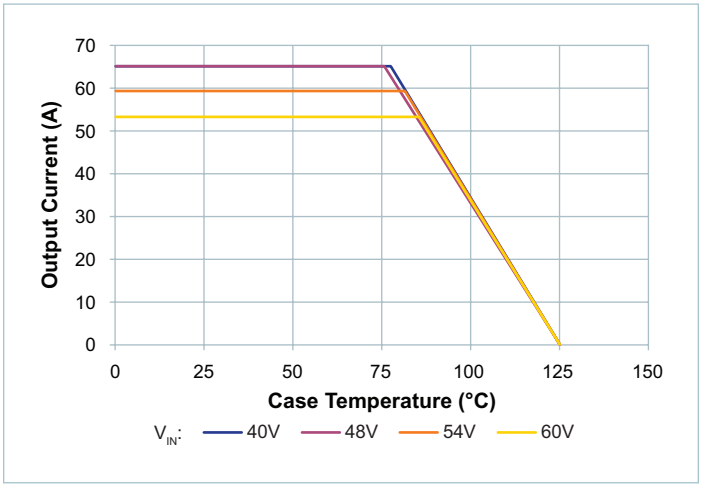


Figure 1 — *Thermal specified operating area; bottom-side cooling, output power vs. case temperature*

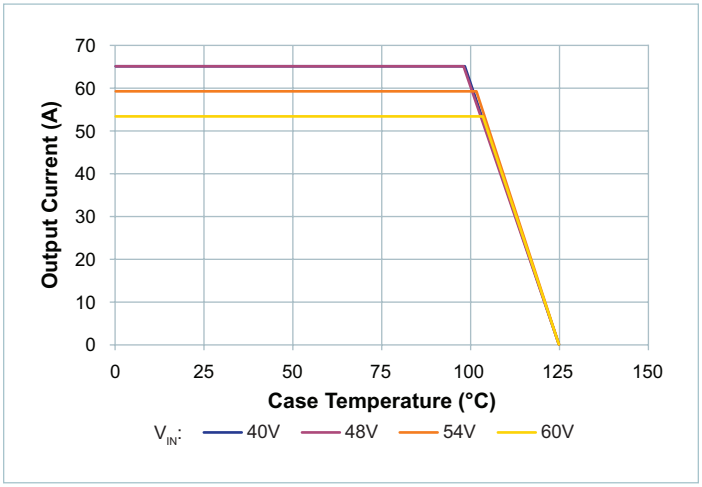


Figure 2 — *Thermal specified operating area; double-sided cooling, output power vs. case temperature*

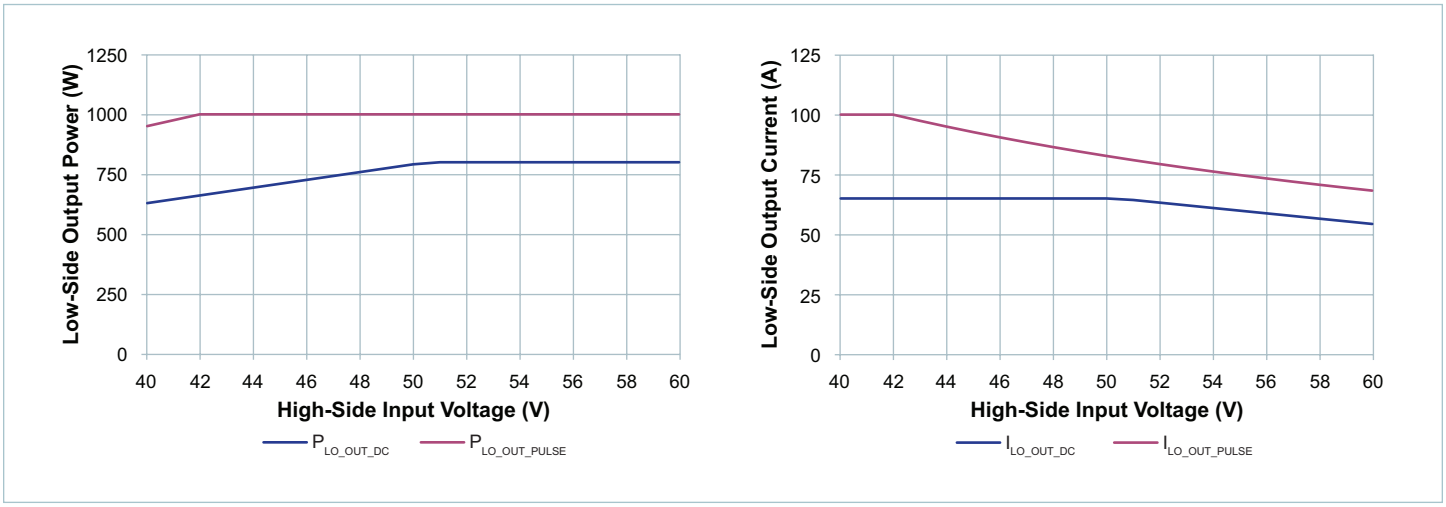


Figure 3 — *Specified electrical operating area, step-down operation*

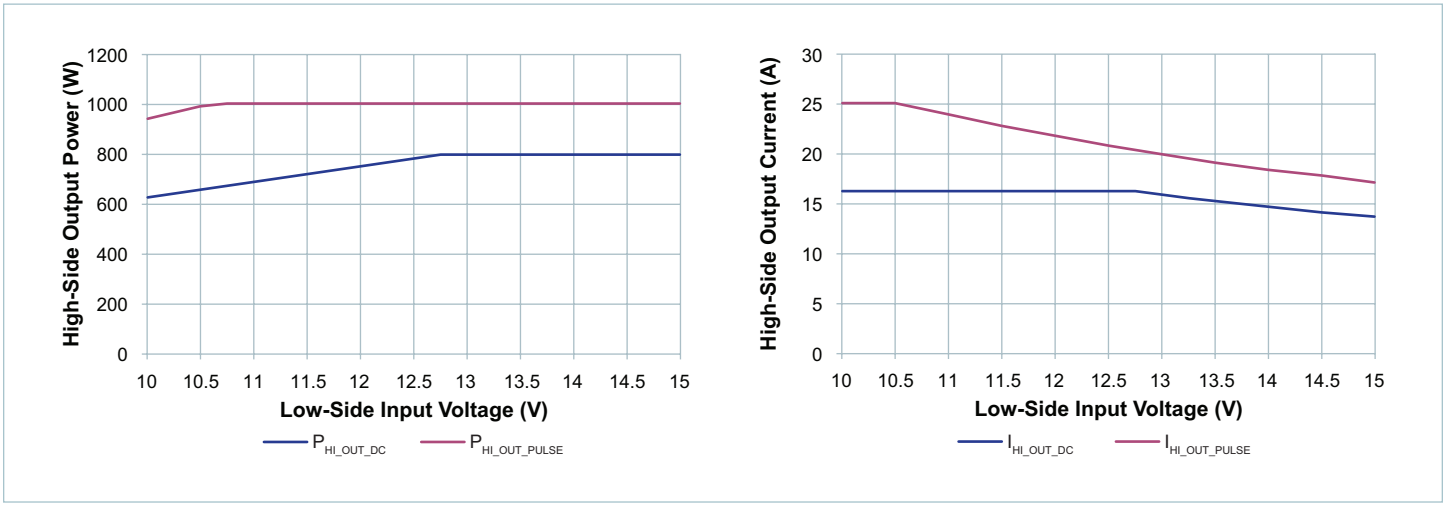


Figure 4 — *Specified electrical operating area, step-up operation*

Application Characteristics, Step-Down Operation

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-down mode, processing power from high-voltage side to low-voltage side. See associated figures for general trend data.

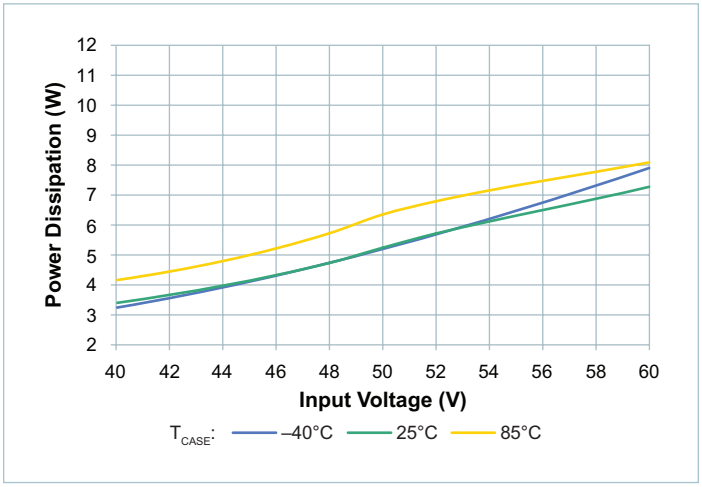


Figure 5 — *No-load power dissipation vs. V_{HI_DC}*

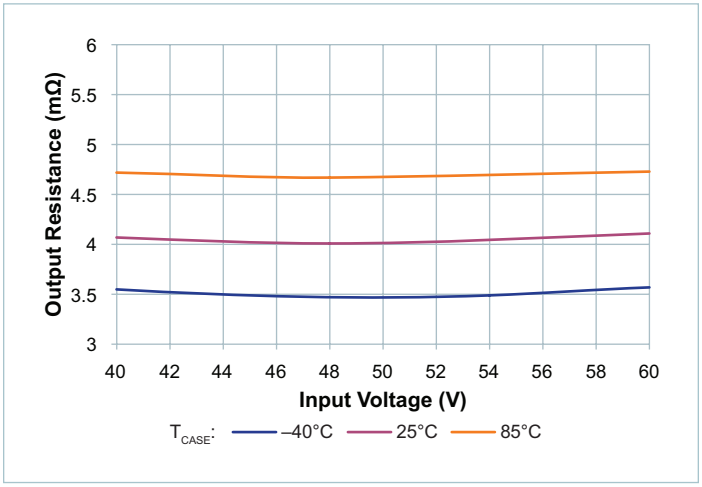


Figure 6 — *R_{LO} vs. input voltage, I_{LO_DC} = 80A*

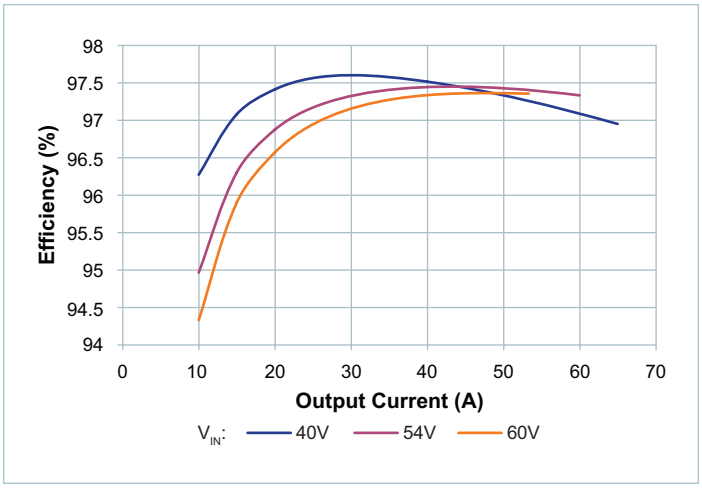


Figure 7 — *Efficiency at T_{CASE} = –40°C*

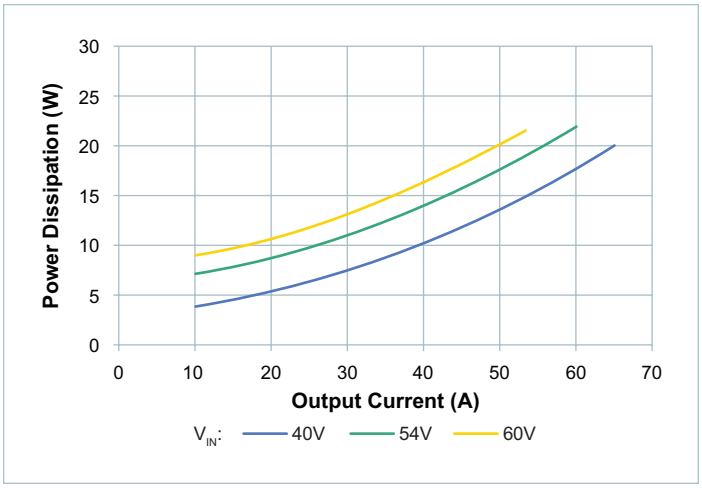


Figure 8 — *Power dissipation at T_{CASE} = –40°C*

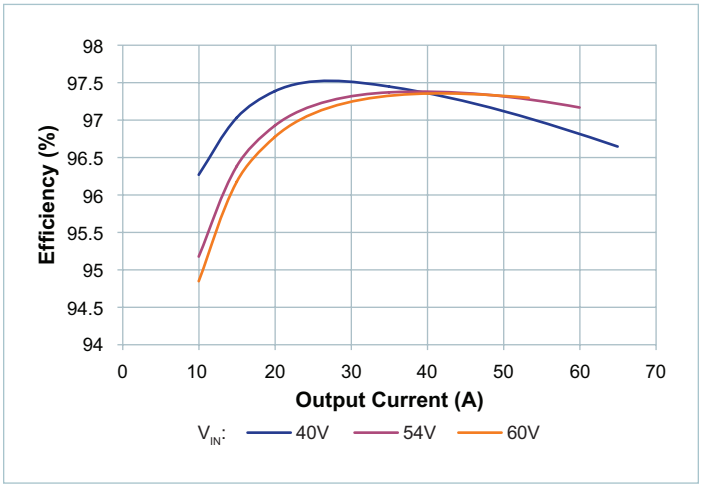


Figure 9 — *Efficiency at T_{CASE} = 25°C*

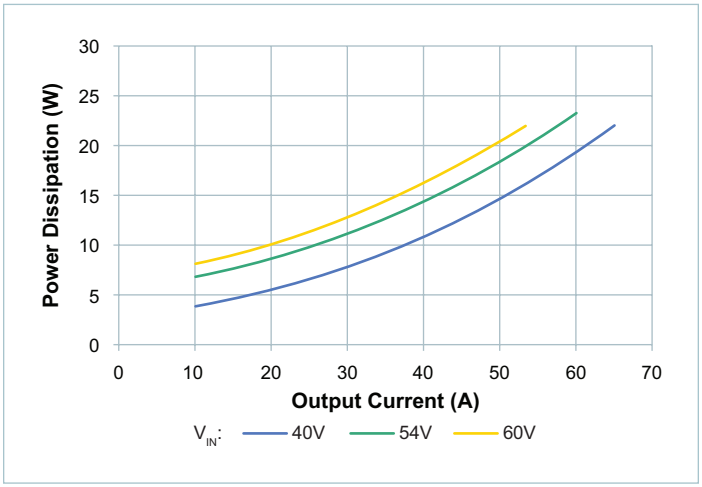


Figure 10 — *Power dissipation at T_{CASE} = 25°C*

Application Characteristics, Step-Down Operation (Cont.)

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-down mode, processing power from high-voltage side to low-voltage side. See associated figures for general trend data.

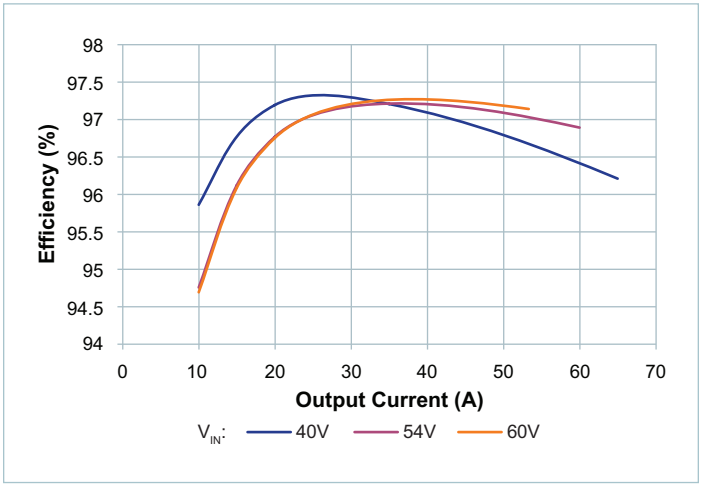


Figure 11 *— Efficiency at T_{CASE} = 85°C*

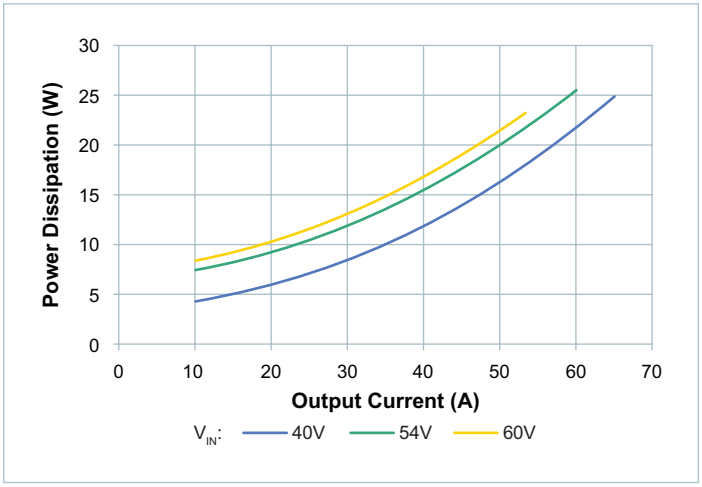


Figure 12 *— Power dissipation at T_{CASE} = 85°C*

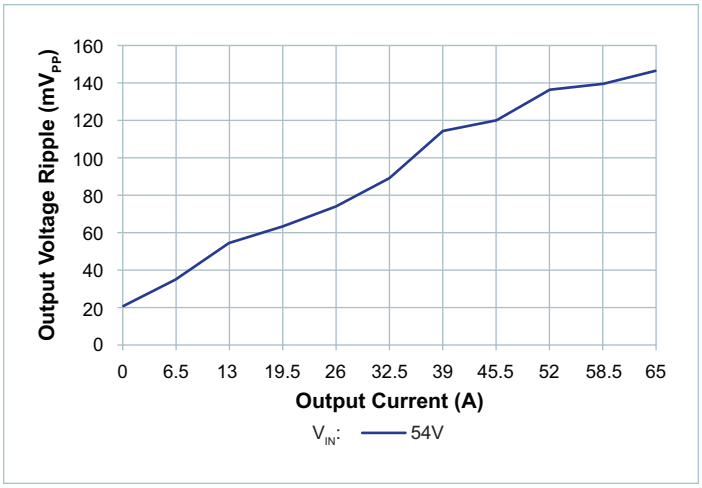


Figure 13 *— $V_{LO\_OUT\_PP}$ vs. I_{LO_DC} ; no external $C_{LO\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

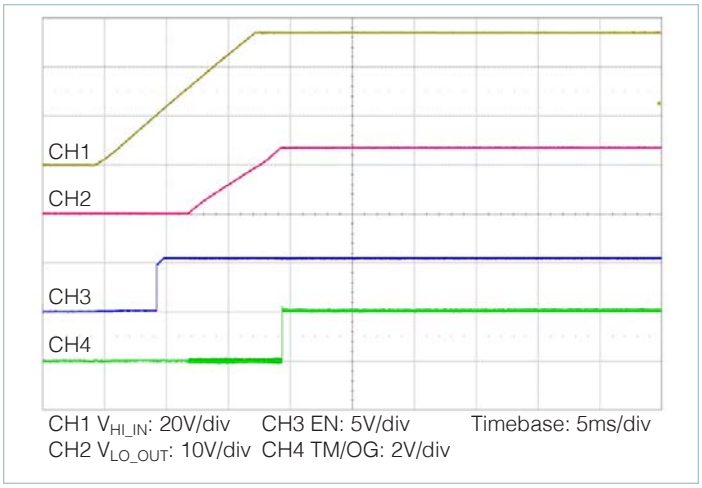


Figure 14 *— Start up from application of V_{HI_DC} = 54V, $C_{LO\_OUT\_EXT}$ = 3000µF, no load; see start up description*

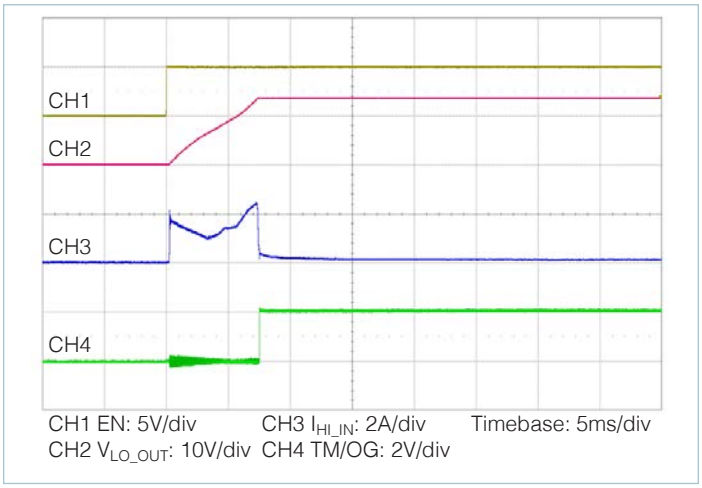


Figure 15 *— Start up from application of EN with pre-applied V_{HI_DC} = 54V, $C_{LO\_OUT\_EXT}$ = 3000µF, no load*

Application Characteristics, Step-Up Operation

Temperature controlled via top-side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-up mode, processing power from low-volage side to high-voltage side. See associated figures for general trend data.

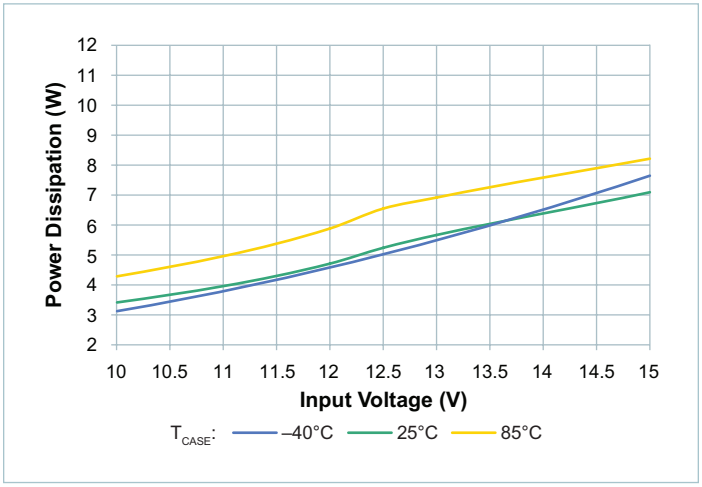


Figure 16 — *No-load power dissipation vs. V_{LO_DC}*

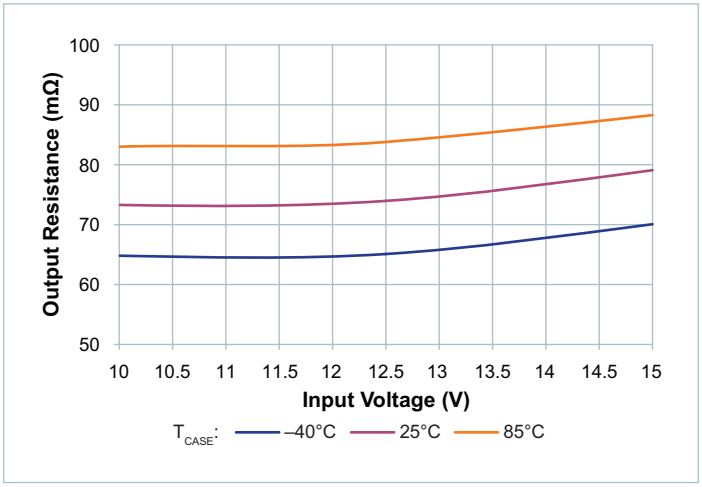


Figure 17 — *R_{HI} vs. input voltage, I_{HI_DC} = 20A*

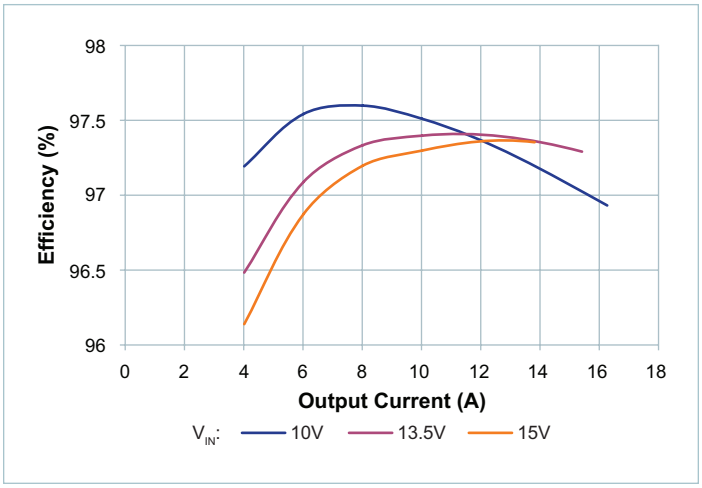


Figure 18 — *Efficiency at T_{CASE} = –40°C*

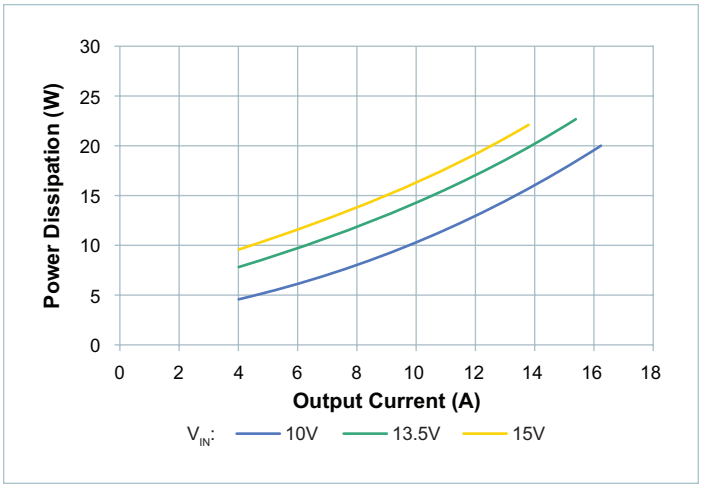


Figure 19 — *Power dissipation at T_{CASE} = –40°C*

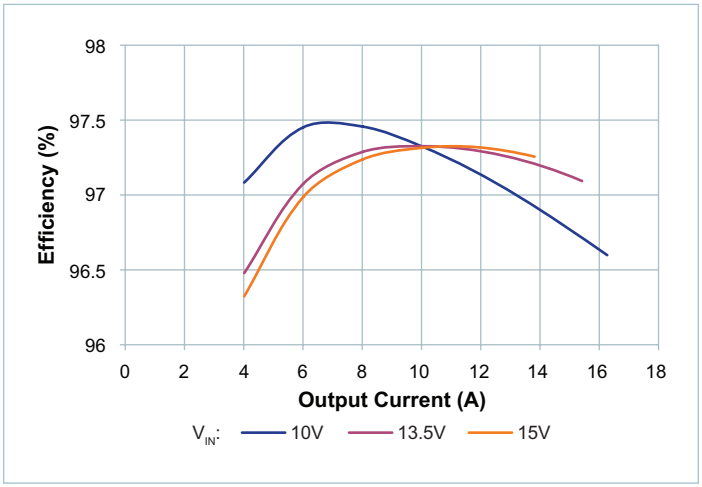


Figure 20 — *Efficiency at T_{CASE} = 25°C*

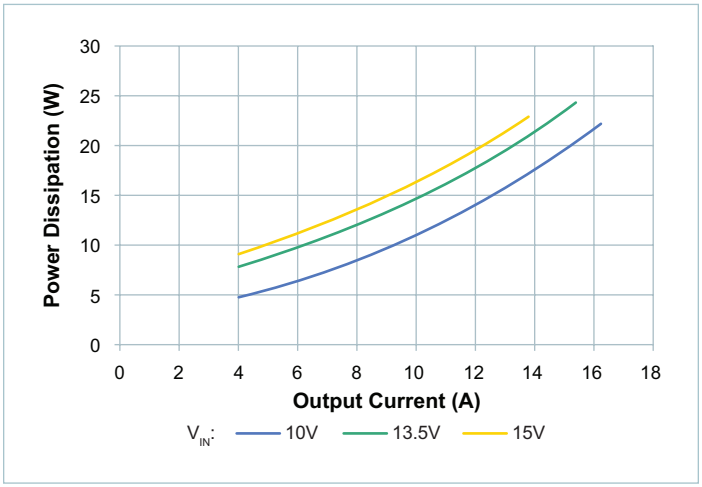


Figure 21 — *Power dissipation at T_{CASE} = 25°C*

Application Characteristics, Step-Up Operation (Cont.)

Temperature controlled via top-side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-up mode, processing power from low-volage side to high-voltage side. See associated figures for general trend data.

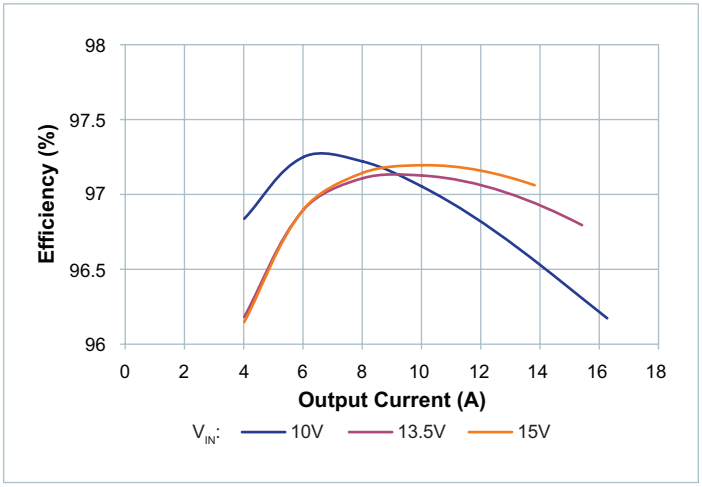


Figure 22 — *Efficiency at T_{CASE} = 85°C*

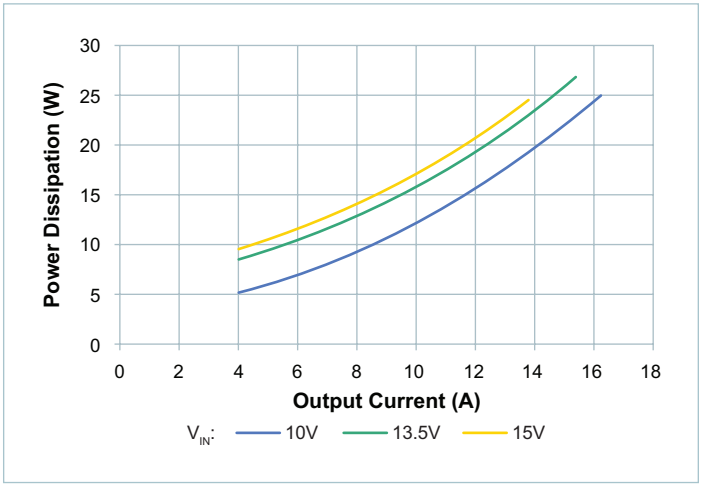


Figure 23 — *Power dissipation at T_{CASE} = 85°C*

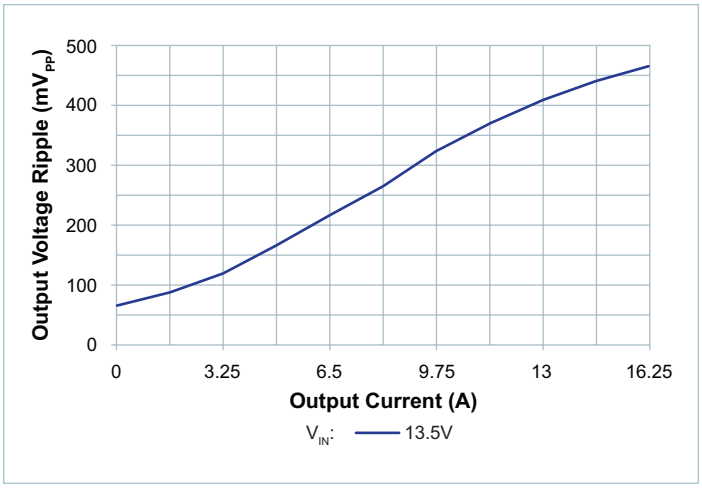


Figure 24 — *$V_{HI\_OUT\_PP}$ vs. I_{HI_DC} ; no external $C_{HI\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

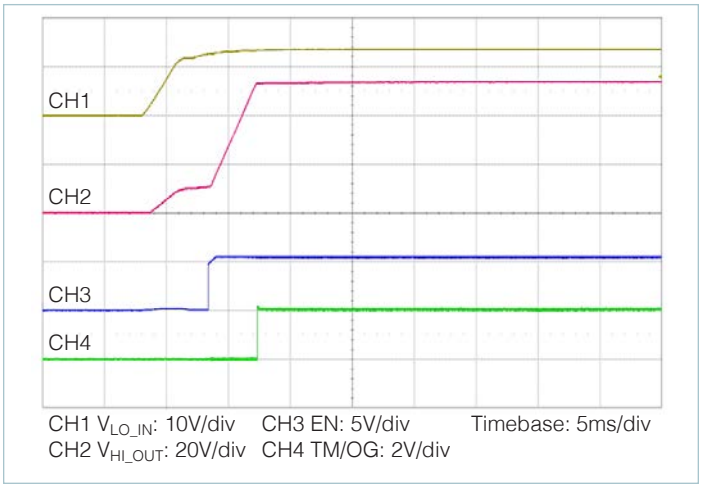


Figure 25 — *Start up from application of V_{LO_DC} = 13.5V, $C_{HI\_OUT\_EXT}$ = 187.5µF, no load*

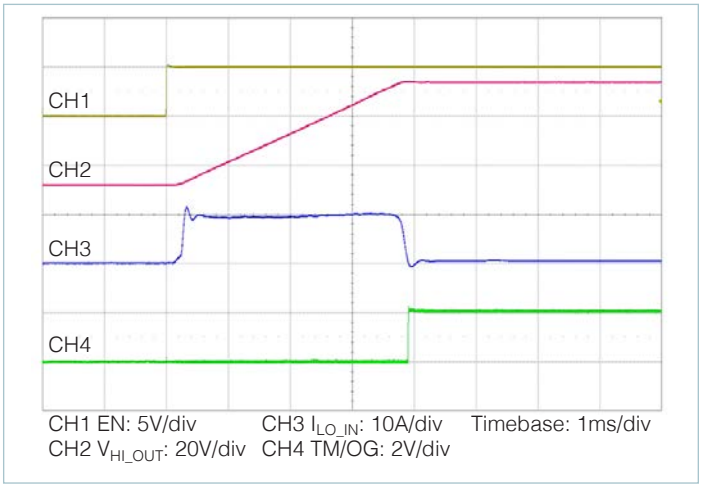


Figure 26 — *Start up from application of EN with pre-applied V_{LO_DC} = 13.5V, $C_{HI\_OUT\_EXT}$ = 187.5µF, no load*

Signal Terminal Descriptions

Enable Control (EN)

The EN terminal enables and disables the NBM. When held low, the NBM is disabled. When allowed to float, the module will start and the EN terminal is pulled up to internally generated V_{EN} (or V_{CC}).

The EN terminal is capable of being either driven high by an external open-collector or open-drain logic signal. During normal operation, EN terminal output is V_{EN}.

In an array of NBM modules, EN terminals should be interconnected to synchronize start up. The NBM modules will start simultaneously when enabled.

Note that NBM must not be disabled if a load is present on the high side while operating in step-up mode to avoid load current conduction through the powertrain MOSFET body diodes.

Temperature Monitor and Output Good (TM / OG)

The TM / OG terminal provides temperature monitoring and power good functionalities. It can be used to accomplish the following two functions:

- *Output Good flag*

  This terminal will be internally held low until the start up has completed. When the output voltage is in a steady-state condition after the completion of the soft start, it will internally be released and can be used as a "Ready to process full load current" flag.

  This signal can be used to drive logic circuit downstream for delayed enable or connection of the load. It can also be used as "Fault flag", as the terminal is pulled low internally when a fault is detected.

- *Monitor the control IC temperature*

  After start up, this terminal provides a voltage proportional to the absolute temperature of the converter control IC. It monitors the internal junction temperature of the controller IC within an accuracy of ±5°C, with an approximate gain of 7mV/°C.

  The following equation can be used to get the equivalent TM voltage in volts for a given junction temperature (T_J) in °C.

$$TM(V) = T_J(°C) \bullet 0.007 + 1.911$$

  The following equation can be used to get the junction temperature (T_J) in °C for a given TM voltage in volts.

$$T_J(°C) = \frac{TM(V) - 1.911}{0.007}$$

Start Up and Bidirectional Operation

The NBM2317S60D1565T0R is capable of start up in both directions (step-up and step-down) once the applied voltage is greater than the undervoltage lockout threshold.

Start Up

- *Start up from application of input voltage*

  When the input voltage is applied, the internal bias supply comes up and powers the internal controller. The controller handles the powertrain switching and fault management. The typical start-up time of bias supply is 3ms from when the input voltage is reached to the controller initialization voltage ($V_{C\text{-}ACTIVE}$).

  When the input voltage slew rate is slower and does not reach to the input undervoltage recovery threshold (UVLO+) within the start-up time of the bias supply, the controller registers the UVLO fault and delays the start-up by the amount of auto restart time ($t_{AUTO\_RESTART}$). However, if the input voltage slew rate is faster and reaches to the input UVLO+ within the start-up time of the bias supply, the output voltage starts after the input-to-output undervoltage start-up delay ($t_{HI\_TO\_LO\_DELAY}$ or $t_{LO\_TO\_HI\_DELAY}$) depending on the mode of operation. Refer to the electrical specifications table for timings.

- *Start up from application of EN with pre-applied input voltage*

  When the input voltage is pre-applied and the start-up is from application of EN signal, the output voltage starts after finishing the enable to powertrain active time (t_{EN_START}).

Bidirectional Operation

The non-isolated bus converter module is fully bidirectional. Once the unit is enabled, the NBM2317S60D1565T0R will operate in step-up mode, transferring energy from low side to the high side, whenever the low-side voltage exceeds $V_{HI} \bullet K$. The NBM2317S60D1565T0R module will operate in step-down mode, transferring energy from high side to the low side, whenever the high-side voltage exceeds V_{LO} / K.

Loading must be delayed until completion of start up. The output good (TM / OG) signal terminal voltage can be used to determine when the start-up has completed and the load can be safely enabled. A load must not be present on the HI-side (+VHI terminal) if the powertrain is not actively switching and LO-side voltage ($+V_{LO}$) is present: remove any HI-side load prior to disabling the module.

Conduction from LO to HI side through powertrain MOSFET body diodes will occur if the unit stops switching while a load is present on the HI side and LO-side voltage ($+V_{LO}$) is present. In other words, if the powertrain is disabled through EN terminal or by any fault detection and LO-side voltage ($+V_{LO}$) is present, then a voltage equal to $+V_{LO}$ minus the body diode drops will appear on the HI side, see Figure 27. Note that in this condition the NBM does not have a current-limiting mechanism from +VLO to +VHI. The built-in short-circuit fault shut down will stop the powertrain switching in case of a fault on the HI side; however external circuitry will be needed to limit the fault current and remove faults.

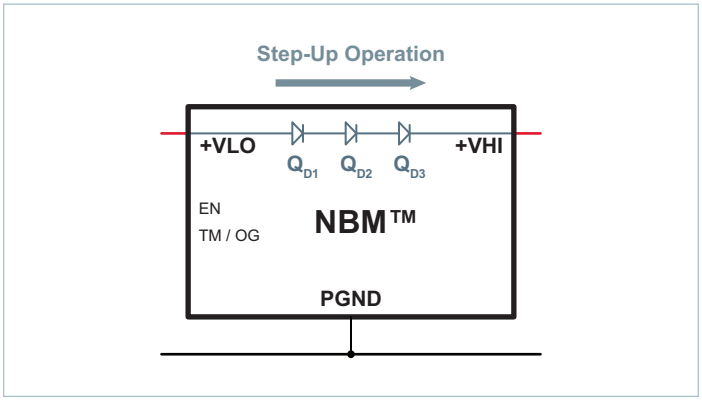


Figure 27 — *Conduction path through MOSFET body diodes under disabled or fault conditions*

Q_{D1}, Q_{D2}, Q_{D3} are the internal power MOSFET drain-source body diodes. The voltage drop across each diode is 1.1V, and any current conduction through the diodes is not recommended.

SM-ChiP™ NBM

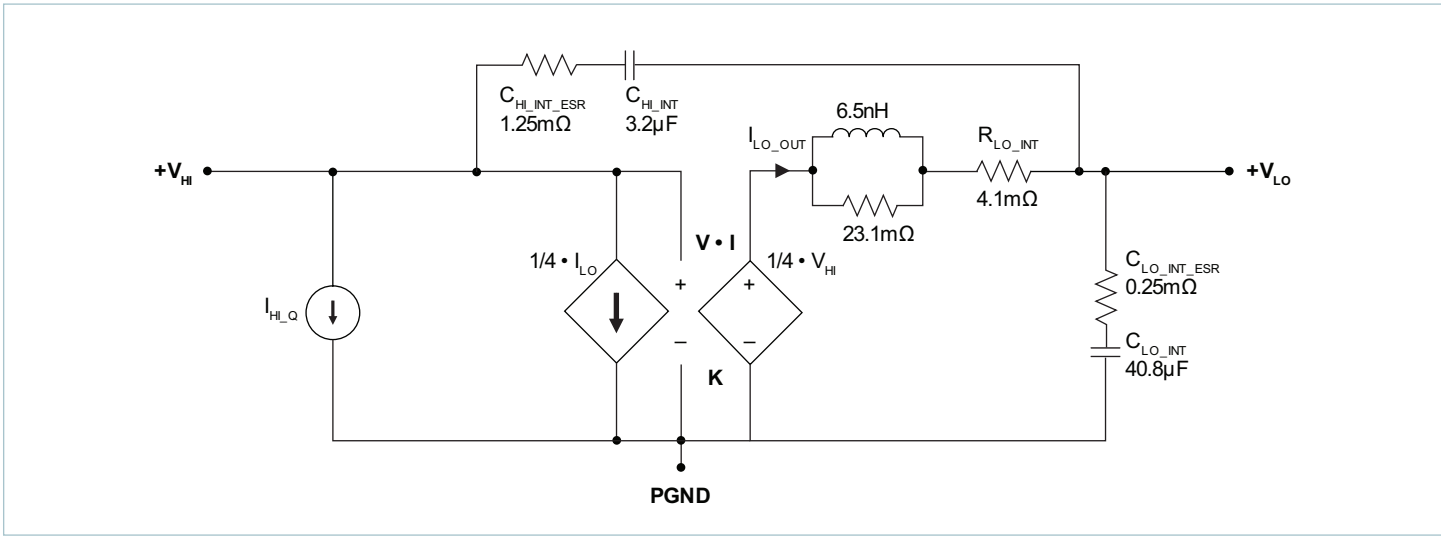


Figure 28 — *NBM AC model*

The NBM uses a high-frequency resonant tank to move energy from high-voltage side to low-voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the high-side voltage and the low-side current. A small amount of capacitance embedded in the high-voltage side and low-voltage side stages of the module is sufficient for full functionality and is key to achieving high power density.

The NBM2317S60D1565T0R can be simplified into the model shown in Figure 28.

At no load:

$$V_{LO} = V_{HI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the NBM.
Rearranging Equation 1:

$$K = \frac{V_{LO}}{V_{HI}} \qquad (2)$$

In the presence of a load, V_{LO} is represented by:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R_{LO} \qquad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI\_Q}}{K} \qquad (4)$$

R_{LO} represents the impedance of the NBM, and is a function of the R_{DS_ON} of the high-side and low-side MOSFETs and the winding resistance of the power transformer. I_{HI_Q} represents the quiescent current of the NBM controller, gate drive circuitry and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that R_{LO} = 0Ω and I_{HI_Q} = 0A, Equation 3 now becomes Equation 1 and is essentially load independent, resistor R is now placed in series with V_{HI}.

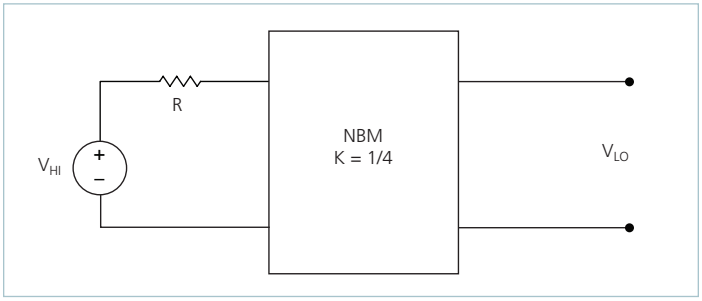


Figure 29 — *K = 1/4 NBM with series high-side resistor*

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = \left(V_{HI} - I_{HI} \bullet R\right) \bullet K \qquad (5)$$

Substituting the simplified version of Equation 4 (I_{HI_Q} is assumed = 0A) into Equation 5 yields:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Equation 3, where R_{LO} is used to represent the characteristic impedance of the NBM. However, in this case a real resistor, R, on the high side of the NBM is effectively scaled by K^2 with respect to the low side.

Assuming that R = 1Ω, the effective R as seen from the low side is 62.5mΩ, with K = 1/4.

A similar exercise can be performed with the additon of a capacitor or shunt impedance at the high-voltage side of the NBM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 30.

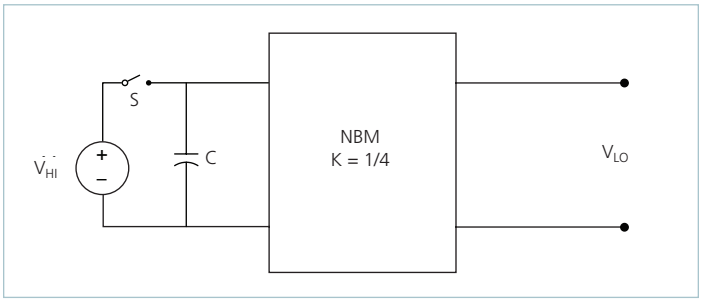


Figure 30 — *NBM with high-side capacitor*

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\,\frac{dV_{HI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{HI}, the switch is opened and the capacitor is discharged through the idealized NBM. In this case,

$$I_C = I_{LO} \bullet K \qquad (8)$$

substituting Equation 1 and 8 into Equation 7 reveals:

$$I_{LO}(t) = \frac{C}{K^2} \bullet \frac{dV_{LO}}{dt} \qquad (9)$$

The equation in terms of the low side has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low side when expressed in terms of the high side. With K = 1/4 as shown in Figure 30, C = 1µF would appear as C = 16µF when viewed from the low side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a NBM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the NBM is too high. The impedance of the NBM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the NBM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the NBM are:

- No load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the NBM modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{HI\_NL} + P_{R_{LO}} \qquad (10)$$

Therefore,

$$P_{LO\_OUT} = P_{HI\_IN} - P_{DISSIPATED} = P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}} \qquad (11)$$

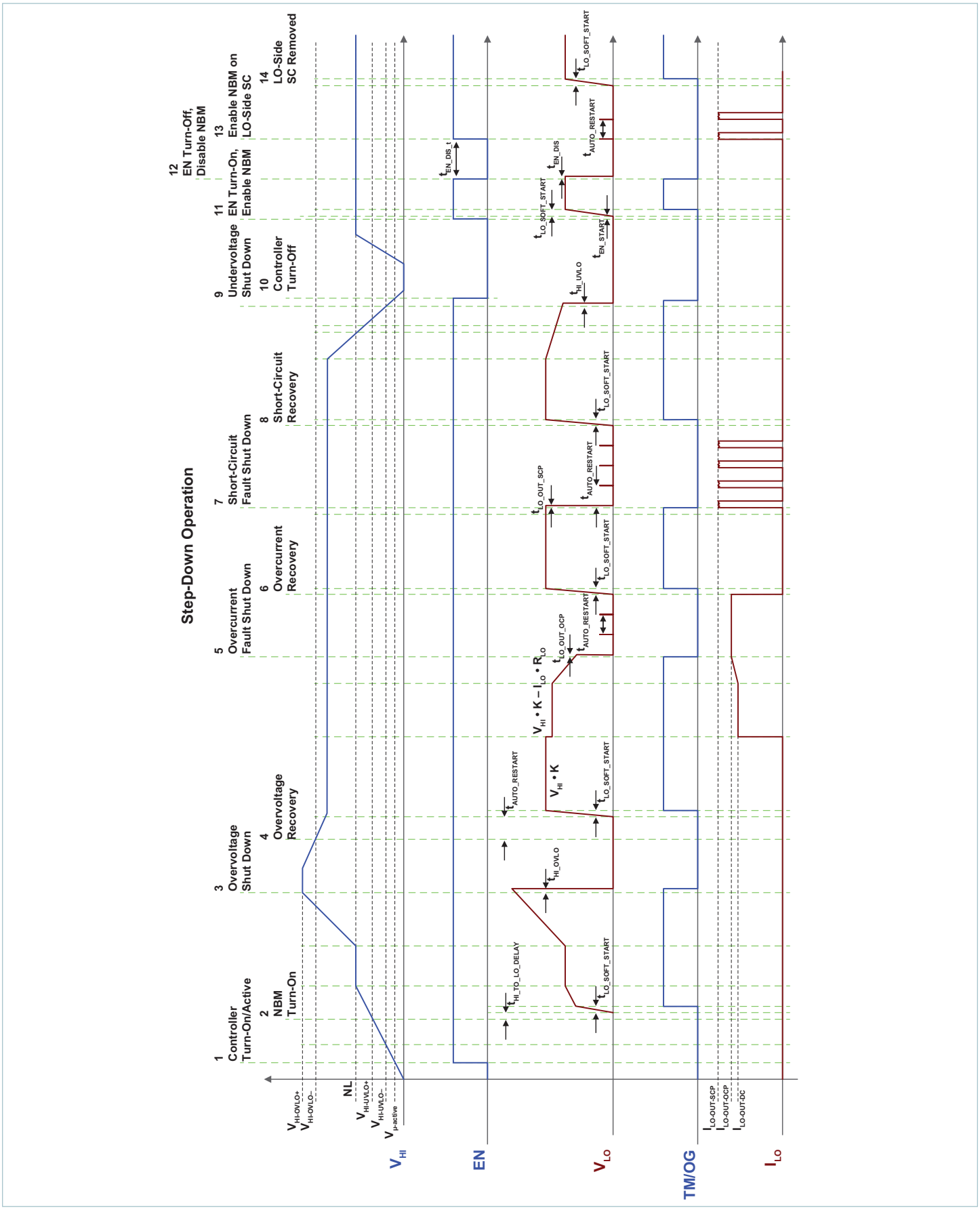
The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{LO\_OUT}}{P_{HI\_IN}} = \frac{P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}}}{P_{HI\_IN}} \qquad (12)$$

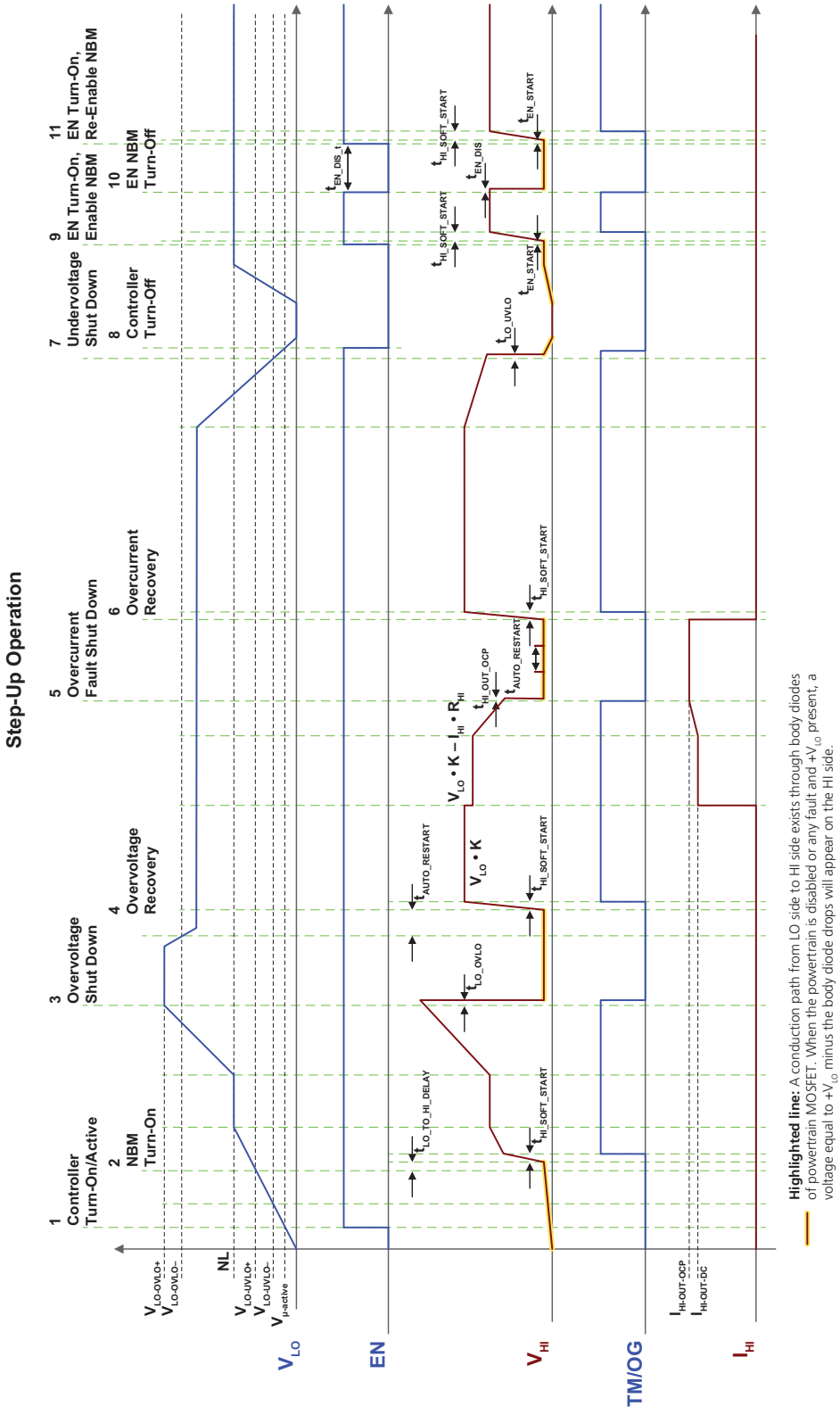
$$= \frac{V_{HI} \bullet I_{HI} - P_{HI\_NL} - (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}$$

$$= 1 - \left(\frac{P_{HI\_NL} + (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}\right)$$

NBM Step-Down Operation Timing Diagram



NBM Step-Up Operation Timing Diagram



Input and Output Filter Design

A major advantage of NBM systems versus conventional PWM converters is that the auto-transformer based NBM does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of high-side voltage and low-side current and efficiently transfers charge through the auto-transformer. A small amount of capacitance embedded in the high-side and low-side stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- *Guarantee low source impedance:*

  To take full advantage of the NBM's dynamic response, the impedance presented to its high-side terminals must be low from DC to approximately 5MHz. The connection of the non-isolated bus converter module to its power source should be implemented with minimal distribution inductance. In step-down operation, the interconnect inductance on the high side should not exceed 300nH; in step-up operation, the interconnect inductance on the low side should not exceed 20nH. If the interconnect inductance exceed these limits, the input side of the NBM should be bypassed with a RC damper or electrolytic capacitor to retain low source impedance and stable operation.

- *Further reduce high-side and/or low-side voltage ripple without sacrificing dynamic response:*

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the high-side source will appear at the low side of the module multiplied by its K factor.

- *Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:*

  The module high-side/low-side voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating range.

Total load capacitance of the NBM module shall not exceed the specified maximum. Owing to the wide bandwidth and low low-side impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the high side of the module. At frequencies <500kHz the module appears as an impedance of R_{LO} between the source and load.

Within this frequency range, capacitance at the high side appears as effective capacitance on the low side per the relationship defined in Equation 13.

$$C_{LO\_EXT} = \frac{C_{HI\_EXT}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Current Sharing

The performance of the NBM topology is based on efficient transfer of energy through a auto-transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal auto-transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple NBMs of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load. Ensuring equal current sharing among modules requires that NBM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- A dedicated input filter for each NBM in an array is recommended to prevent circulating currents.

For further details see:
AN:016 Using BCM Bus Converters in High Power Arrays

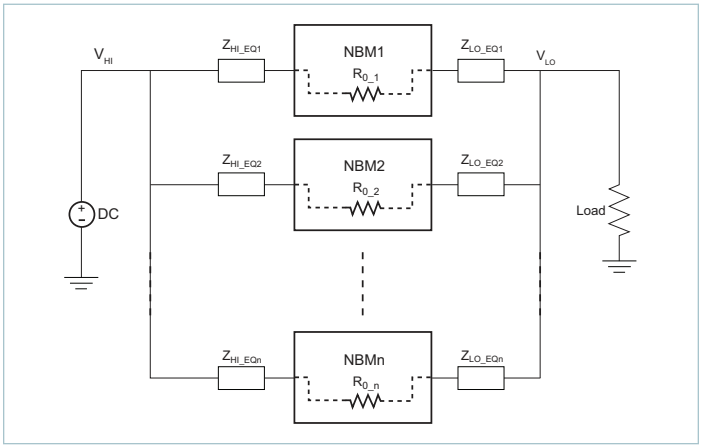


Figure 31 — *NBM parallel array*

Input Fuse Selection

In order to provide flexibility in configuring power systems, SM-ChiP™ modules are not internally fused. Input line fusing of SM-ChiP products is recommended at the system level to provide thermal protection in case of catastrophic failure.

An input fuse is required to meet safety agency conditions of acceptability. A 25A input fuse (Littelfuse® Nano2® 456 Series) is required in step-down operation to comply with safety agency conditions of acceptability. An e-fuse or a disconnect is required on the input in step-up mode. Always ascertain and observe the safety, regulatory or other agency specifications that apply to your specific application.

Thermal Considerations

The SM-ChiP™ module provides a high degree of flexibility in that it presents several pathways to remove heat from the internal power dissipating components. Heat may be removed from the top surface, the bottom surface, the power terminals and the signal terminals. The extent to which these surfaces are cooled is a key component in determining the maximum current that is available from an SM-ChiP, as can be seen from Figure 1.

Since the SM-ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. Given that there are many pathways to remove heat from the SM-ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors.

Figure 32(a) shows the "thermal circuit" for a NBM2317 SM-ChiP in two-sided cooling application, where the product is cooled through the PCB at the bottom and a heat sink at the top. In this case, the NBM power dissipation is $P_{DISSIPATION}$ and the top and bottom (heat sink and PCB) surface temperatures are represented as $T_{TOP\_HEAT\_SINK}$ and T_{PCB}. This thermal system can now be very easily analyzed as an electrical network with simple resistors, voltage sources, and a current source. The results of the simulation provide an estimate of heat flow through the various dissipation pathways as well as internal temperature.

Figure 32(b) shows the thermal model for an application with single-side cooling, where the heat is dissipated through the PCB only.

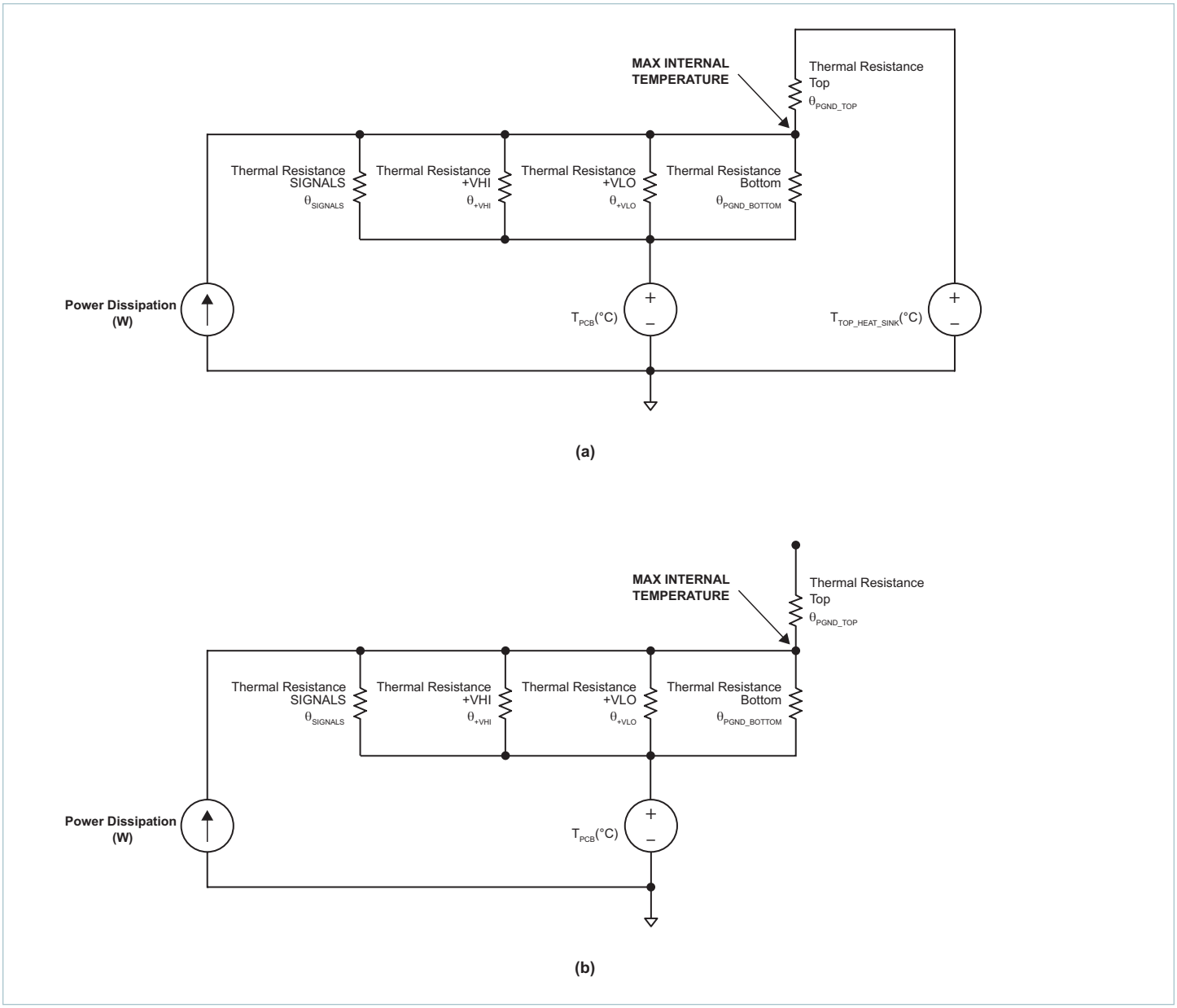


Figure 32 — *NBM2317S60D1565T0R two-sided cooling thermal model (a) and bottom-side cooling only (through PCB) thermal model (b).*

Thermal Considerations (Cont.)

Symbol	Thermal Impedance (°C / W)	Definition of Estimated Thermal Resistance
θ_{PGND_TOP}	1.6	from the hottest component junction inside the NBM to PGND_TOP
$\theta_{SIGNALS}$	55	from the hottest component junction inside the NBM to the circuit board it is mounted on at SIGNALS
θ_{+VHI}	17	from the hottest component junction inside the NBM to the circuit board it is mounted on at +VHI
θ_{+VLO}	7.1	from the hottest component junction inside the NBM to the circuit board it is mounted on at +VLO
θ_{PGND_BOTTOM}	1.9	from the hottest component junction inside the NBM to the circuit board it is mounted on at PGND_BOTTOM

Table 1 — *Thermal impedance*

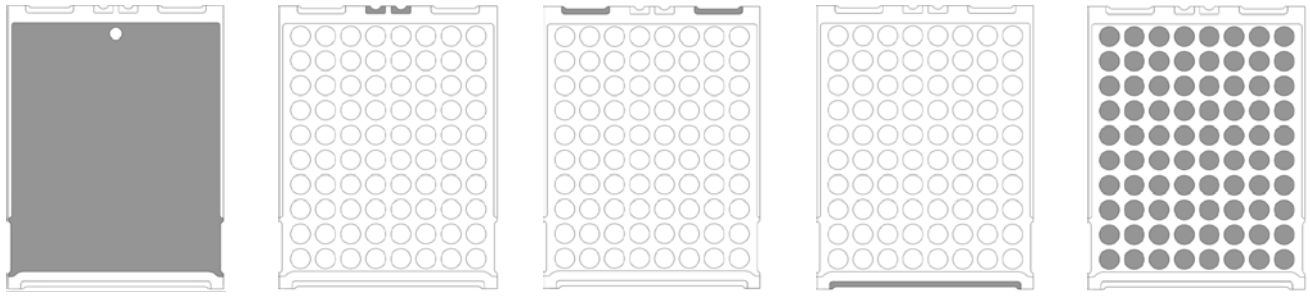
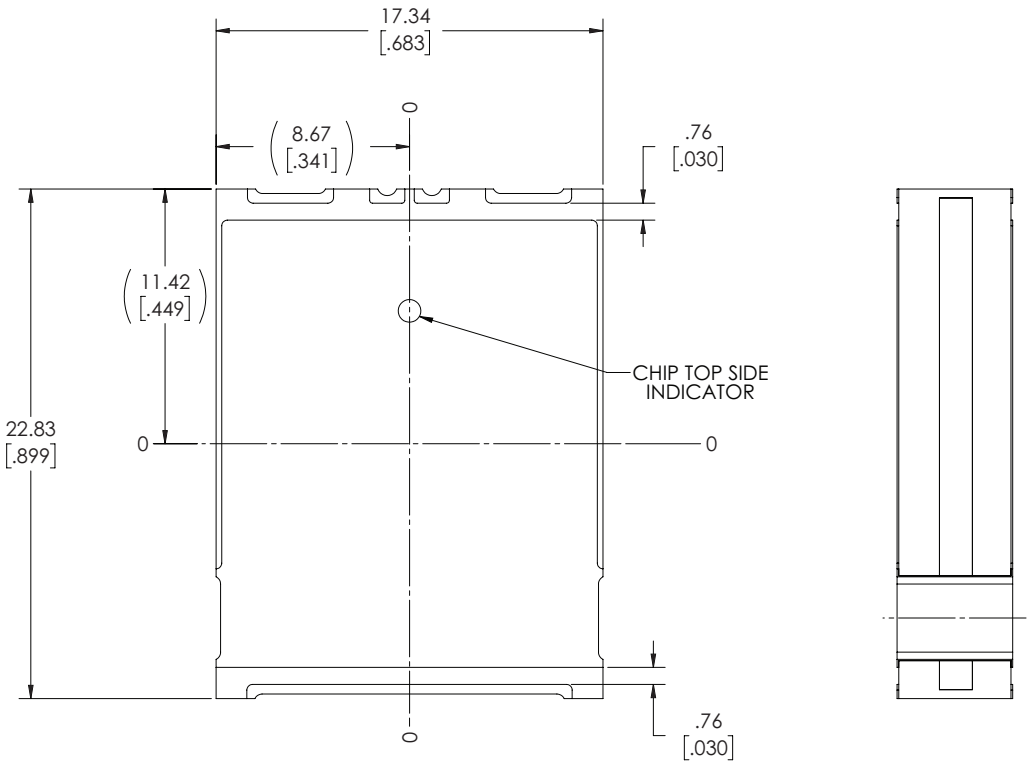


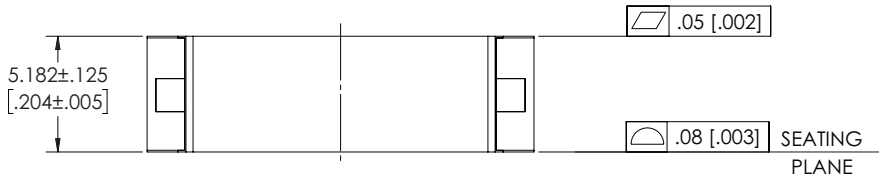
Figure 33 — *Thermal model boundary conditions; area defined as shaded*

NBM Package Drawing Top & Side View

2317 NBMTC6
(Reference DWG # 49373 Rev 2)



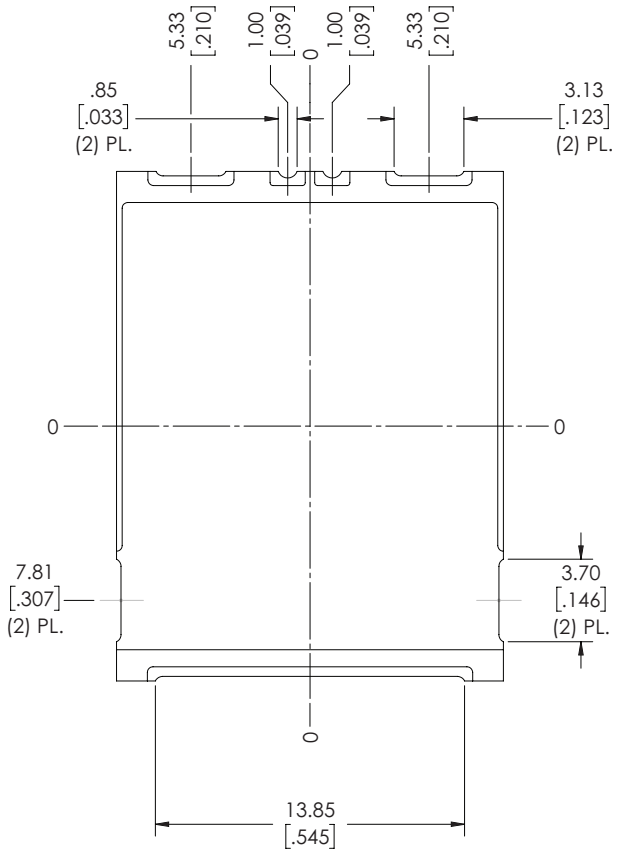
TOP VIEW
(COMPONENT SIDE)



NOTES:
1- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM [INCH]
2- TOLERANCES ARE:
DECIMALS
X.XX [X.XX] = ±0.25 [0.01]
X.XXX [X.XXX] = ±0.127 [0.005]
ANGLES = ±1°

NBM Package Drawing Bottom View

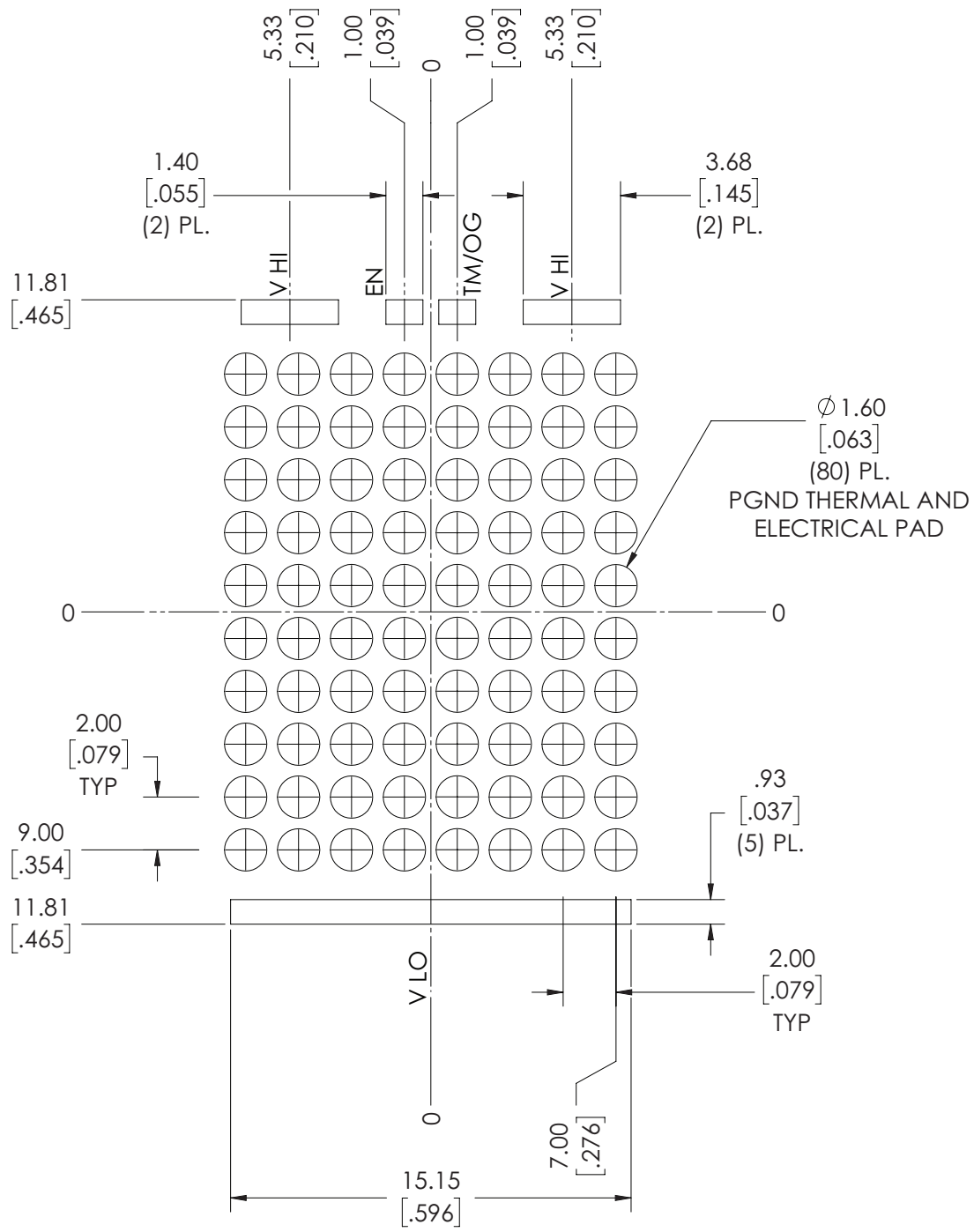
2317 NBMTC6
(Reference DWG # 49373 Rev 2)



BOTTOM VIEW

NBM Recommended Land Pattern (Component Side)

2317 NBMTC6
(Reference DWG # 49373 Rev 2)



RECOMMENDED LAND PATTERN

Revision History

Revision	Date	Description	Page Number(s)
1.0	07/07/21	Initial release	n/a

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