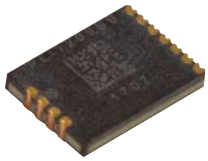
Point-of-Load Isolator

PLI1209BCxyzz



Digital Supervisor with Isolation for use with BCM® Bus Converter Modules

Features & Benefits

- PMBus-compatible host interface for enhanced monitoring and control of ChiP and SM-ChiP BCM modules
- Interfaces with primary-referenced ChiP modules through dedicated, isolated UART channels, enabling secondary-referenced control and telemetry
- Overvoltage, overcurrent and overtemperature protection and monitoring
- Three isolated digital channels (one receive, two transmit)
- DC Isolation Voltage = 4242V_{DC}
- AC Isolation Voltage = 3000V_{RMS}
- 12 x 9mm SM-ChiP package
- Safety Regulatory Approvals: IEC 60950-1, EN 60950-1, UL 60950-1

Typical Applications

- 380V_{DC} Power Distribution
- High-End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High-Density Power Supplies
- Communications Systems
- Transportation

Product Description

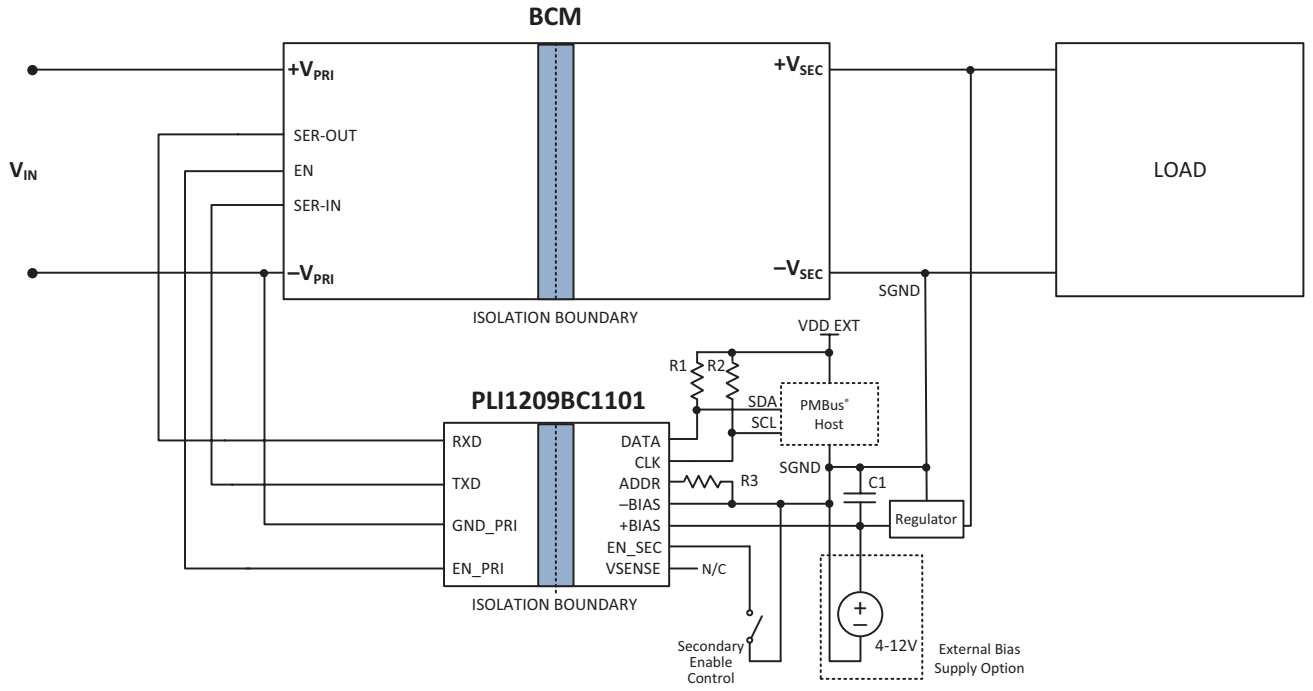
The PLI1209BCxyzz is an isolated digital power system supervisor that provides a communication interface between a host processor and a ChiP™ or SM-ChiP™ BCM.

The PLI communicates with a system controller via a PMBus® compatible interface over an isolated UART interface. Through the PLI, the host processor can configure, set protection limits, and monitor the BCM.

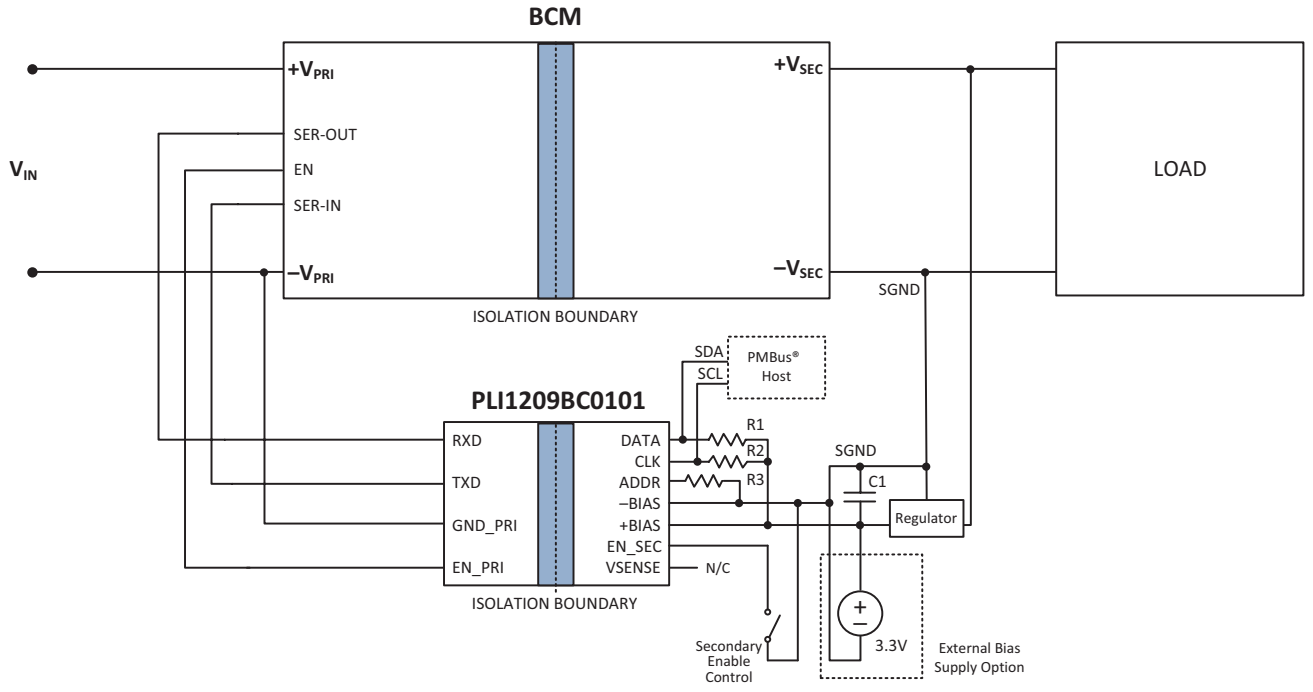
Standard Models

Product Function	Package Size	Compatible ChiP	Bias Supply	Interface Type	Unique Version Identifier
PLI	1209	BC	0	1	01
PLI	1209	BC	1	1	01

Typical Applications

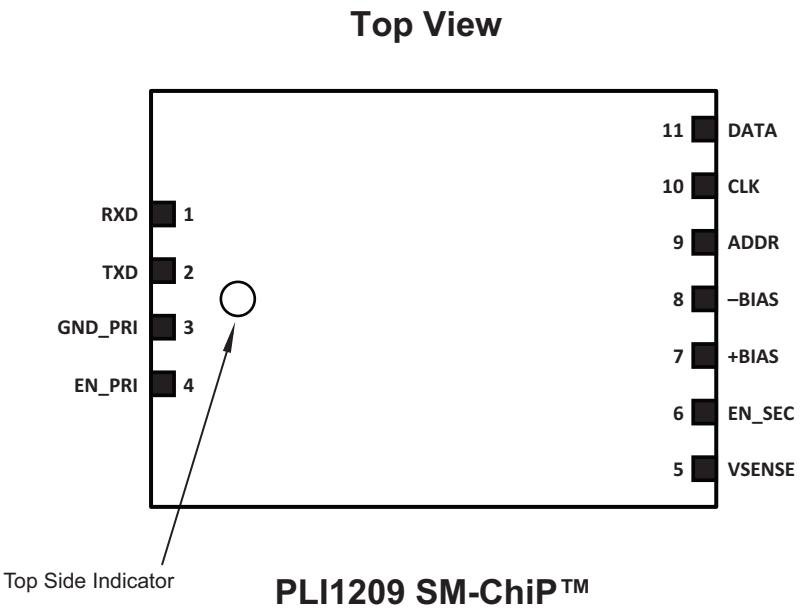


Typical Application: BCM ChiP with PLI1209BC1101, connection to PMBus® Host
(Pull-up resistors R1 and R2 to VDD_EXT required if not implemented by PMBus Host)



Typical Application: BCM ChiP with PLI1209BC0101, connection to PMBus Host
(Pull-up resistors R1 and R2 to +BIAS required if not implemented by PMBus Host)

Pin Configuration



Pin Descriptions

Signal Name	Pin Number	Type	Description
Primary-Side Referenced Signals			
RXD	1	INPUT	UART receive channel, receive data from BCM
TXD	2	OUTPUT	UART transmit channel, send data to BCM
GND_PRI	3	SIGNAL GROUND	Primary-side signal ground reference
EN_PRI	4	OUTPUT	Primary-side referenced enable/disable signal to BCM
Secondary-Side Referenced Signals			
VSENSE	5	INPUT	Not used, no connection
EN_SEC	6	INPUT	Secondary-side referenced enable/disable signal. Connect to LV secondary-side enable control signal.
+BIAS	7	INPUT POWER	Positive input power terminal
–BIAS	8	INPUT POWER RETURN	Negative input power terminal
ADDR	9	INPUT	Address assignment – resistor-based
CLK	10	OUTPUT	I^2C Clock, PMBus®-Compatible
DATA	11	INPUT/OUTPUT	I^2C Data, PMBus-Compatible

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+BIAS to –BIAS	PLI1209BC0yzz	–0.3	3.6	V
	PLI1209BC1yzz	–0.3	16	
I_{+BIAS}			75	mA
RXD to GND_PRI		–0.5	4.6	V
TXD, EN_PRI to GND_PRI		–0.3	20	V
DATA, CLK to –BIAS		–0.3	5.5	V
ADDR, EN_SEC, VSENSE to –BIAS		–0.3	3.6	V
Isolation Voltage / Dielectric Withstand	Reinforced insulation	4242		V_{DC}
		3000		V_{RMS}
Operating Temperature	Internal	–40	125	°C
Storage Temperature	Internal	–55	125	°C

Primary-Side Referenced Signal Characteristics

Specifications apply over the rated supply range (V_{+BIAS}), unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

UART Pins: TXD & RXD

- Universal Asynchronous Receiver/Transmitter (UART) pins.
- Provide intrasystem communication to a ChiP Bus Converter Module (BCM).
- The Point-of-Load Isolator incorporates an isolated interface for communication to a BCM using the UART pins.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General I/O	Regular Operation	Baud Rate	BR_{UART}			**750**		kbits/s
Digital Input		**RX Receive Pin**						
		RX Input Voltage Threshold	V_{RX_IH}		2.6			V
			V_{RX_IL}				0.8	
		RX Rise Time	t_{RX_RISE}	10 – 90%		150		ns
		RX Fall Time	t_{RX_FALL}	10 – 90%		30		ns
		RX External Capacitance	C_{RX-EXT}				120	pF
Digital Output		**TX Transmit Pin**						
		TX Output Voltage Threshold	V_{TX_OH}		2.9			V
			V_{TX_OL}				0.1	V
		TX Rise Time	t_{TX_RISE}	10 – 90%		150		ns
		TX Fall Time	t_{TX_FALL}	10 – 90%		30		ns
		TX Sink Current	I_{TX}				24	mA
		TX Output Impedance	Z_{TX}			**0.75**		Ω

Primary-Side Enable Pin: EN_PRI

- The EN_PRI pin is used to drive the primary-side referenced BCM EN pin.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Output	Regular Operation	Voltage Level	$V_{EN\_PRI\_OH}$		2.9			V
			$V_{EN\_PRI\_OL}$				0.1	V
		Leakage Current	$I_{EN\_PRI\_LEAKAGE}$				50	nA
		Rise Time	$t_{EN\_PRI\_RISE}$	10 – 90%		150		ns
		Fall Time	$t_{EN\_PRI\_FALL}$	10 – 90%		30		ns
		Sink Current	I_{EN_PRI}				24	mA
		Output Impedance	Z_{EN_PRI}			**0.75**		Ω

Signal Ground Pin: GND_PRI

- Signal return and reference for all primary-side Point-of-Load Isolator signal input/output.

Secondary-Side Referenced Signal Characteristics

Specifications apply over the rated supply range (V_{+BIAS}), unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Bias Pin: +BIAS

- +BIAS powers the internal controller.
- +BIAS must be applied to enable and disable the BCM through PMBus® control (using OPERATION COMMAND) or through EN_SEC pin and to adjust warning and protection thresholds.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Input	Regular Operation	+BIAS Voltage	V_{+BIAS}	PLI1209BC0yzz	3	3.3	3.6	V
				PLI1209BC1yzz	4	5	12	
		Internally Generated V_{CC}	V_{CC}	PLI1209BC1yzz	3.23	3.3	3.37	V
		+BIAS Current Consumption	I_{+BIAS}				50	mA
	Start Up	Inrush Current Peak	I_{+BIAS_INR}	PLI1209BC0yzz, +BIAS slew rate 1V/µs		60		mA
		Turn-On time	t_{VDD_ON}	From V_{+BIAS_MIN} to PMBus active		1.5		ms

Bias Return Pin: –BIAS

- +BIAS power supply return pin and reference for all Point-of-Load Isolator secondary-side signals.

Address Pin: ADDR

- This pin programs the address using a resistor between ADDR pin and –BIAS.
- The address is sampled during start up and is stored until power is reset. This pin programs only a fixed and persistent address.
- This pin has an internal 10kΩ pull-up resistor to V_{+BIAS} (PLI1209BC0yzz) or 3.3V (PLI1209BC1yzz).
- 16 addresses are available. The range of each address nominally 206.25mV (total range for all 16 addresses is 0 – 3.3V).

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Multi-Level Input	Regular Operation	ADDR Input Voltage	V_{ADDR}	At typical V_{+BIAS}	0		3.3	V
		ADDR Leakage Current	I_{ADDR}	Leakage current			1	µA
	Start Up	ADDR Registration Time	t_{ADDR}	From V_{+BIAS_MIN}		1		ms

Secondary-Side Enable Pin: EN_SEC

- +BIAS powers the internal controller.
- The EN_SEC pin is a standard analog I/O configured as an input to an internal µC.
- The EN_SEC pin is an active-high logic input and is internally pulled up to V_{CC} (See Bias Pin: +BIAS description).
- Use an open-collector or open-drain connection to actively pull down on the EN_SEC pin to disable the BCM. Allow the EN-SEC pin to float to enable connected BCM.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Input	Any	EN_SEC Enable Threshold	$V_{EN\_SEC\_EN}$	At typical V_{+BIAS}	2.31			V
		EN_SEC Disable Threshold	$V_{EN\_SEC\_DIS}$	At typical V_{+BIAS}			0.99	V
		EN_SEC Internal Pull-Up Resistance to V_{CC}	$R_{EN\_SEC\_INT}$		31.9	32.2	32.5	kΩ

Voltage Sense Pin: VSENSE

- No connection. Voltage Sense pin is unused in BCM applications.

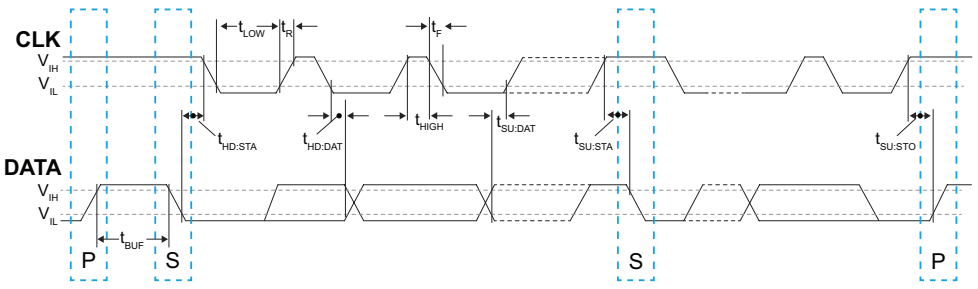
Secondary-Side Referenced Signal Characteristics (Cont.)

Specifications apply over the rated supply range (V_{+BIAS}), unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Serial Clock Input and Serial Data Pins: CLK & DATA

- High-power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is signal not supported.
- PMBus® command compatible.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input/Output	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}	At typical V_{+BIAS}	2.31			V
			V_{IL}	At typical V_{+BIAS}			0.99	V
		Output Voltage Threshold	V_{OH}	At typical V_{+BIAS}	3			V
			V_{OL}	At typical V_{+BIAS}			0.4	V
		Leakage Current	$I_{LEAK-PIN}$	Unpowered device	–10		10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10 – 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	kHz
		Free Time Between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold Time After Start or Repeated Start Condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Setup Time	$t_{SU:STA}$		0.6			µs
		Stop Condition Set-Up Time	$t_{SU:STO}$		0.6			µs
		Data Hold Time	$t_{HD:DAT}$		300			ns
		Data Setup Time	$t_{SU:DAT}$		100			ns
		Clock Low Time Out	$t_{TIMEOUT}$		25		35	ms
		Clock Low Period	t_{LOW}		1.3			µs
		Clock High Period	t_{HIGH}		0.6		50	µs
		Cumulative Clock Low Extend Time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall Time	t_F	Measured from (V_{IL_MAX} – 0.15) to (V_{IH_MIN} + 0.15)	20		300	ns
		Clock or Data Rise Time	t_R	0.9 • $V_{VDD\_IN\_MAX}$ to (V_{IL_MAX} – 0.15)	20		300	ns

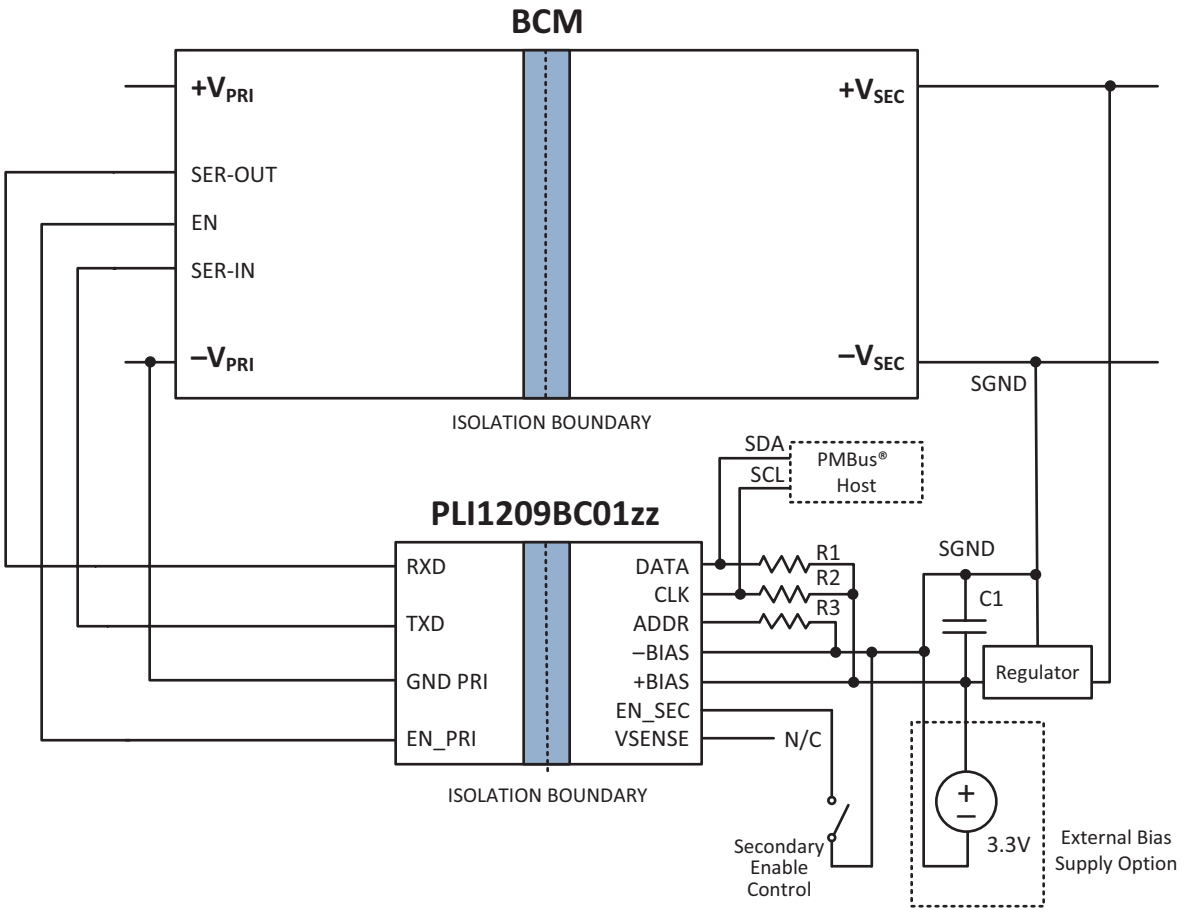


General Characteristics

Specifications apply over the rated supply range (V_{+BIAS}), unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		12.35 [0.486]	12.48 [0.491]	12.61 [0.496]	mm [in]
Width	W		9.06 [0.357]	9.19 [0.362]	9.32 [0.367]	mm [in]
Height	H		1.678 [0.066]	1.803 [0.071]	2.053 [0.081]	mm [in]
Weight	W			0.5 [0.017]		g [oz]
Thermal						
Operating Temperature	T_{INT}	PLI1209BCxyzz, T-Grade	–40		125	°C
Assembly						
Storage Temperature	T_{ST}	PLI1209BCxyzz, T-Grade	–55		125	°C
Moisture Sensitivity Level	MSL	MSL4, 72 hours of out bag				
ESD Withstand	ESD_{HBM}	Human Body Model, (JEDEC JS-001-2012) Class 2, ≥ 2000V to < 8000V				
	ESD_{CDM}	Charge Device Model, (JESD22-C101-E) Class 2, ≥ 200V to < 500V				
Soldering						
Peak Temperature During Reflow		Under MSL 4 conditions listed above, up to three reflows			245	°C
Peak Time above 217°C				60	90	s
Safety						
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer		11.0		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		25.4		MHrs
Agency Approvals / Standards		cTÜVus EN 60950-1				
		cURus UL 60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

System Functional Description



The Point-of-Load Isolator provides the host system telemetry access to a single Bus Converter Module (BCM). The PLI1209BCxyzz is a PMBus® child and will respond only to host commands listed in subsequent sections. The PLI enables the PMBus-compatible host interface with an operating bus speed of up to 400kHz.

The Point-of-Load Isolator is a self-powered device as defined by the SMBus specification and has a single secondary-side referenced power input pin. For model PLI1209BC0yzz, +BIAS directly supplies internal circuitry. For model PLI1209BC1yzz, +BIAS is a wide-range input that powers an internal regulator.

The Point-of-Load Isolator allows UART communication over an isolated interface between the host system and the associated primary-referenced BCM UART pins. The PLI1209BCxyzz UART interface operates at a typical speed of 750kHz across the isolation barrier. Each PLI provides enough signal channels for operation with one BCM.

The Point-of-Load Isolator regularly polls the UART interface and stores the BCM's telemetry, faults and warnings. This updated data is then available for access by the host processor via the PMBus interface. Direct communication to the individual BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the PLI data and page (0x01) prior to a telemetry inquiry points to the connected BCM data. BCM reported parameters calibration coefficient and calibration gain are factory set and are stored in individual BCMs ensuring specified telemetry accuracy is met. Refer to the respective BCM datasheet for more details.

A startup order of the Point-of-Load Isolator or the BCM array is not required. The PLI is constantly probing all UART pins to discover connected BCMs.

The PMBus output voltage level setting commands and faults do not apply to the BCM. The BCM during normal operation will provide an output voltage proportional to its transfer ratio referred to as BCM K Factor.

Any available communication enabled BCM may be used with a Point-of-Load Isolator.

PMBus® Interface

Refer to "PMBus Power System Management Protocol SpecificationRevision 1.2, Part I and II" for complete PMBus specifications details visit http://pmbus.org.

Device Address

The PMBus address (ADDR Pin) should be set to one of a predetermined 16 possible addresses shown in the table below using a voltage divider from ADDR to –BIAS.

The BCM and PLI accept only a fixed and persistent address and do not support SMBus address resolution protocol. At initial power-up, the PLI will sample the address pin voltage and will hold this address until device power is removed.

ID	Child Address	HEX	Recommended Resistor R_{ADDR} (Ω)
1	1010 000b	50h	487
2	1010 001b	51h	1050
3	1010 010b	52h	1870
4	1010 011b	53h	2800
5	1010 100b	54h	3920
6	1010 101b	55h	5230
7	1010 110b	56h	6810
8	1010 111b	57h	8870
9	1011 000b	58h	11300
10	1011 001b	59h	14700
11	1011 010b	5Ah	19100
12	1011 011b	5Bh	25500
13	1011 100b	5Ch	35700
14	1011 101b	5Dh	53600
15	1011 110b	5Eh	97600
16	1011 111b	5Fh	316000

Reported DATA Formats

The PLI employs a direct data format where all reported PLI measurements are in Volts, Amperes, Degrees Celsius, or Seconds. The host uses the following PMBus specification to interpret received values metric prefixes. Note that the Coefficients command is not supported:

$$X = \left(\frac{1}{m}\right) \bullet \left(Y \bullet 10^{-R} - b\right)$$

Where:

X, is a "real world" value in units (A, V, °C, s)

Y, is a two's complement integer received from the PLI

m, b and R are two's complement integers defined as follows:

Command	Code	m	R	b
TON_DELAY	60h	1	3	0
READ_VIN	88h	1	1	0
READ_IIN [a]	89h	1	3	0
READ_VOUT [b]	8Bh	1	1	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1 [c]	8Dh	1	0	0
READ_POUT	96h	1	0	0
READ_PIN	97h	1	1	0
MFR_VIN_MIN	A0h	1	0	0
MFR_VIN_MAX	A1h	1	0	0
MFR_VOUT_MIN	A4h	1	0	0
MFR_VOUT_MAX	A5h	1	0	0
MFR_IOUT_MAX	A6h	1	0	0
MFR_POUT_MAX	A7h	1	0	0
READ_K_FACTOR	D1h	65536	0	0
READ_BCM_ROUT	D4h	1	5	0

[a] READ_IIN command listed value valid for HV BCM products. Use R = 2 for LV BCM products.
[b] Default READ Output Voltage returned when BCM unit is disabled = –300V.
[c] Default READ Temperature returned when BCM unit is disabled = –273°C.

READ_IIN command listed value valid for HV BCM products. Use R = 2 for LV BCM products.

Supported Command List

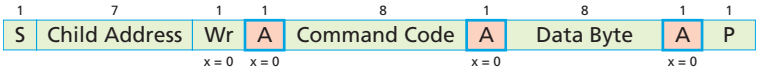
Command	Code	Function	Default Data Content	Data Bytes
PAGE	00h	Access PLI stored information	00h	1
OPERATION	01h	Turn BCM on or off	80h	1
ON_OFF_CONFIG	02h	Defines startup when power is applied as well as immediate on/off control over the BCM	1Dh	1
CLEAR_FAULTS	03h	Clear all faults	N/A	None
CAPABILITY	19h	PMBus® key capabilities set by factory	20h	1
OT_FAULT_LIMIT	4Fh [d]	Overtemperature protection	64h	2
OT_WARN_LIMIT	51h [d]	Overtemperature warning	64h	2
VIN_OV_FAULT_LIMIT	55h [d]	High-voltage-side overvoltage protection	64h	2
VIN_OV_WARN_LIMIT	57h [d]	High-voltage-side overvoltage warning	64h	2
IIN_OC_FAULT_LIMIT	5Bh [d]	High-voltage-side overcurrent protection	64h	2
IIN_OC_WARN_LIMIT	5Dh [d]	High-voltage-side overcurrent warning	64h	2
TON_DELAY	60h [d]	Startup delay in addition to fixed delay	00h	2
STATUS_BYTE	78h	Summary of faults	00h	1
STATUS_WORD	79h	Summary of fault conditions	00h	2
STATUS_IOUT	7Bh	Overcurrent fault status	00h	1
STATUS_INPUT	7Ch	Overvoltage and undervoltage fault status	00h	1
STATUS_TEMPERATURE	7Dh	Overtemperature and undertemperature fault status	00h	1
STATUS_CML	7Eh	PMBus communication fault	00h	1
STATUS_MFR_SPECIFIC	80h	Other BCM status indicator	00h	1
READ_VIN	88h	Reads high-side voltage	FFFFh	2
READ_IIN	89h	Reads high-side current	FFFFh	2
READ_VOUT	8Bh	Reads low-side voltage	FFFFh	2
READ_IOUT	8Ch	Reads low-side current	FFFFh	2
READ_TEMPERATURE_1	8Dh	Reads internal temperature	FFFFh	2
READ_POUT	96h	Reads low-side power	FFFFh	2
READ_PIN	97h	Reads high-side power	FFFFh	2
PMBUS_REVISION	98h	PMBus compatible revision	22h	1
MFR_ID	99h	PLI ID	"VI"	2
MFR_MODEL	9Ah	PLI or BCM model	Part Number	18
MFR_REVISION	9Bh	PLI or BCM revision	FW and HW revision	18
MFR_LOCATION	9Ch	PLI or BCM factory location	"AP"	2
MFR_DATE	9Dh	PLI or BCM manufacturing date	"YYWW"	4
MFR_SERIAL	9Eh	PLI or BCM serial number	Serial Number	16
MFR_VIN_MIN	A0h	Minimum rated high-side voltage	Varies per BCM	2
MFR_VIN_MAX	A1h	Maximum rated high-side voltage	Varies per BCM	2
MFR_VOUT_MIN	A4h	Minimum rated low-side voltage	Varies per BCM	2
MFR_VOUT_MAX	A5h	Maximum rated low-side voltage	Varies per BCM	2
MFR_IOUT_MAX	A6h	Maximum rated low-side current	Varies per BCM	2
MFR_POUT_MAX	A7h	Maximum rated low-side power	Varies per BCM	2
USER_DATA_0	B0h	Custom user data space	00h	29
USER_DATA_1	B1h	Custom user data space	00h	29
BCM_EN_POLARITY	D0h [d]	Set BCM EN pin polarity	02h	1
READ_K_FACTOR	D1h	Reads K factor	Varies per BCM	2
READ_BCM_ROUT	D4h	Reads low-voltage-side output resistance	Varies per BCM	2
SET_ALL_THRESHOLDS	D5h [d]	Set supervisory warning and protection thresholds	646464646464h	6
DISABLE_FAULT	D7h [d]	Disable overvoltage, overcurrent or undervoltage supervisory faults	00h	2

[d] The BCM must be in a disabled state with $V_{IN} < V_{IN\_UVLO-}$ and +BIAS applied to the PLI during a write message.

Command Structure Overview

Write Byte protocol:

The Host always initiates PMBus® communication with a START bit. All messages are terminated by the Host with a STOP bit. In a write message, the parent sends the child device address followed by a write bit. Once the child acknowledges, the parent proceeds with the command code and then similarly the data byte.



S Start Condition

Sr Repeated start Condition

Rd Read

Wr Write

X Indicated that field is required to have the value of x

A Acknowledge (bit may be 0 for an ACK or 1 for a NACK)

P Stop Condition

From Parent to Child

From Child to Parent

... Continued next line

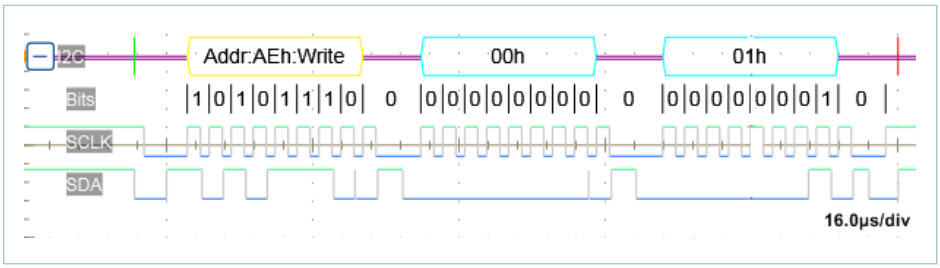
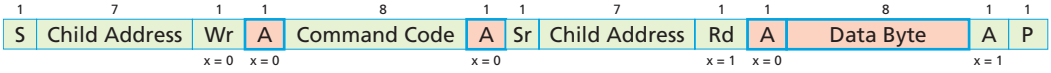


Figure 1 — *PAGE COMMAND (00h), WRITE BYTE PROTOCOL*

Read Byte protocol:

A Read message begins by first sending a Write Command, followed by a REPEATED START Bit and a child Address. After receiving the READ bit, the PLI begins transmission of the Data responding to the Command. Once the Host receives the requested Data, it terminates the message with a NACK preceding a stop condition signifying the end of a read transfer.



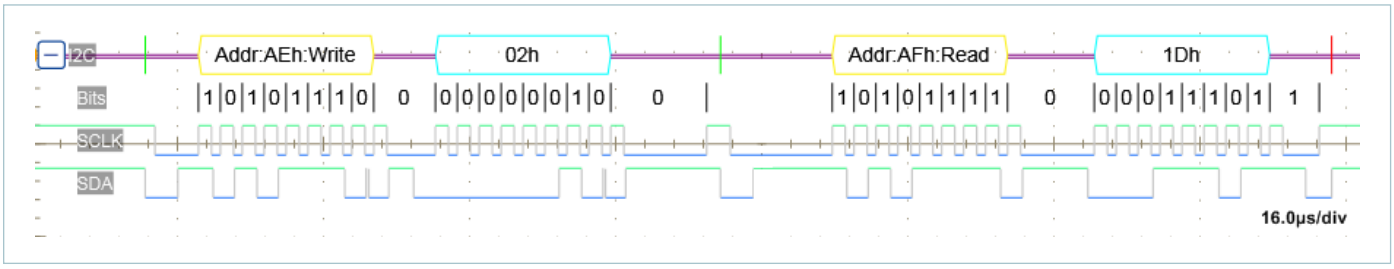
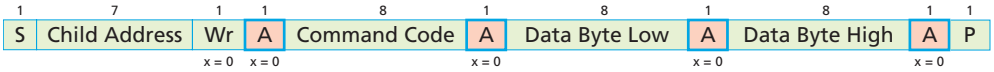


Figure 2 — *ON_OFF_CONFIG COMMAND (02h), READ BYTE PROTOCOL*

Write Word protocol:

When transmitting a word, the lowest order byte leads the highest order byte. Furthermore, when transmitting a Byte, the least significant bit (LSB) is sent last. Refer to System Management Bus (SMBus) specification version 2.0 for more details.

Note: Extended command and Packet Error Checking Protocols are not supported.



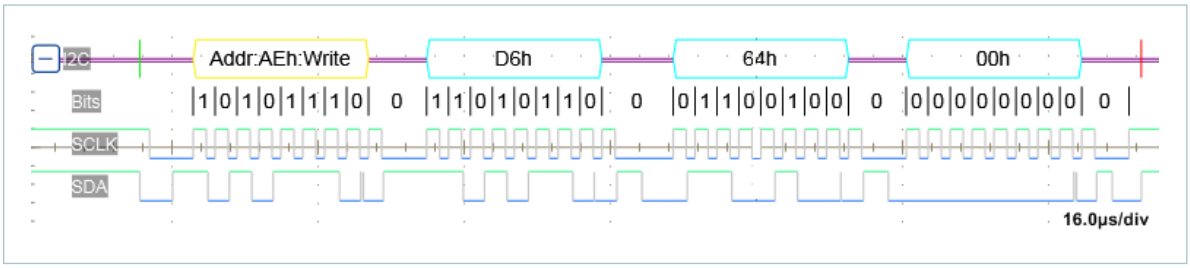
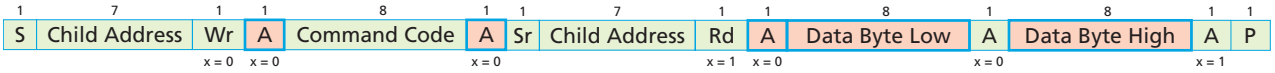


Figure 3 — *TON_DELAY COMMAND (D6h)_WRITE WORD PROTOCOL*

Read Word protocol:



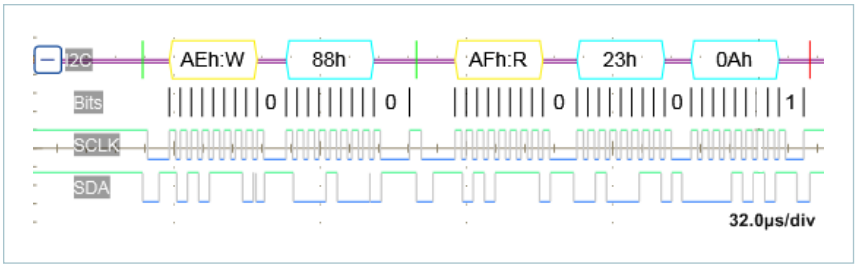
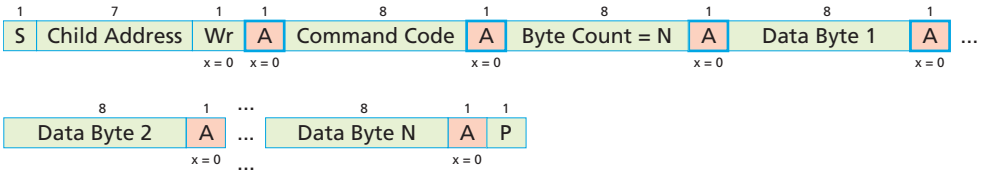


Figure 4 — *MFR_VIN_MIN COMMAND (88h)_READ WORD PROTOCOL*

Write Block protocol:



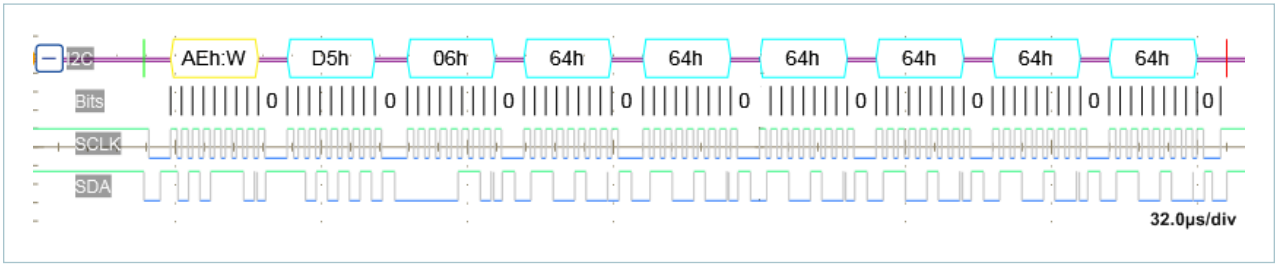
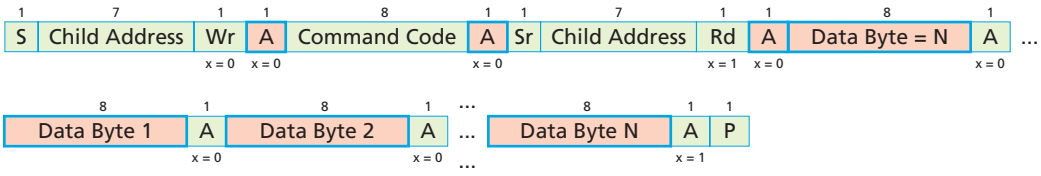


Figure 5 — *SET_ALL_THRESHOLDS COMMAND (D5h)_WRITE BLOCK PROTOCOL*

Read Block protocol:



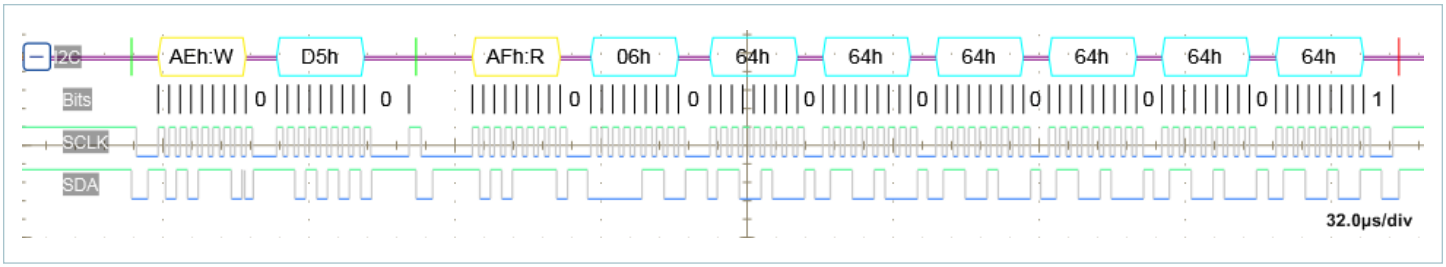
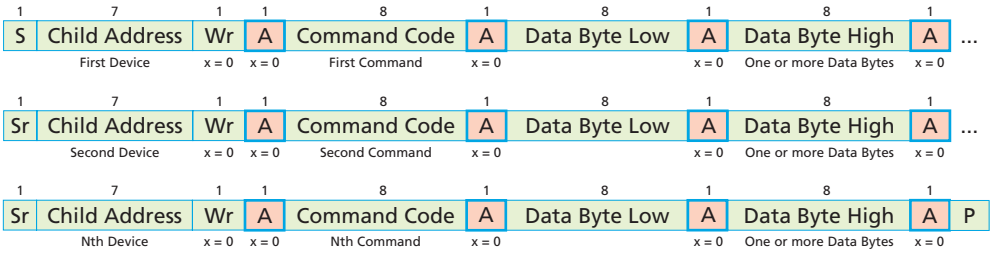


Figure 6 — *SET_ALL_THRESHOLDS COMMAND (D5h)_READ BLOCK PROTOCOL*

Write Group Command protocol:



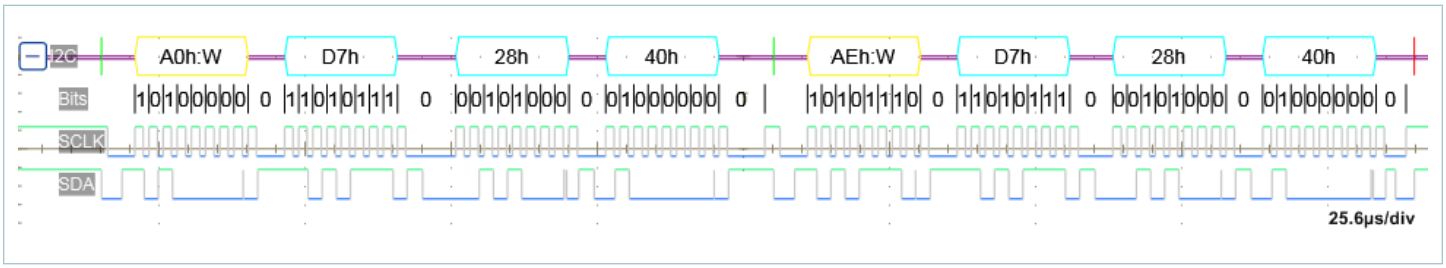


Figure 7 — *DISABLE_FAULT COMMAND (D7h)_WRITE*

Note that only one command per device is allowed in a group command.

Supported Commands Transaction Type

A direct communication to the PLI and a simulated communication to non-PMBus® devices is enabled by a page command. Supported command access privileges with a pre-selected PAGE are defined in the following table. Deviation from this table generates a communication error in STATUS_CML register.

Command	Code	PAGE Data Byte Access Type	
		00h	01h
PAGE	00h	R/W	R/W
OPERATION	01h	R	R/W
ON_OFF_CONFIG	02h		R
CLEAR_FAULTS	03h	W	W
CAPABILITY	19h	R	
OT_FAULT_LIMIT	4Fh		R/W
OT_WARN_LIMIT	51h		R/W
VIN_OV_FAULT_LIMIT	55h		R/W
VIN_OV_WARN_LIMIT	57h		R/W
IIN_OC_FAULT_LIMIT	5Bh		R/W
IIN_OC_WARN_LIMIT	5Dh		R/W
TON_DELAY	60h		R/W
STATUS_BYTE	78h	R/W	R
STATUS_WORD	79h	R	R
STATUS_IOUT	7Bh	R	R/W
STATUS_INPUT	7Ch	R	R/W
STATUS_TEMPERATURE	7Dh	R	R/W
STATUS_CML	7Eh	R/W	
STATUS_MFR_SPECIFIC	80h	R[	R/W
READ_VIN	88h		R
READ_IIN	89h	R	R
READ_VOUT	8Bh		R
READ_IOUT	8Ch	R	R
READ_TEMPERATURE_1	8Dh	R	R
READ_POUT	96h	R	R
READ_PIN	97h	R	R
PMBUS_REVISION	98h	R	
MFR_ID	99h	R	
MFR_MODEL	9Ah	R	R
MFR_REVISION	9Bh	R	R
MFR_LOCATION	9Ch	R	R
MFR_DATE	9Dh	R	R
MFR_SERIAL	9Eh	R	R
MFR_VIN_MIN	A0h	R	R
MFR_VIN_MAX	A1h	R	R
MFR_VOUT_MIN	A4h	R	R
MFR_VOUT_MAX	A5h	R	R
MFR_IOUT_MAX	A6h	R	R
MFR_POUT_MAX	A7h	R	R
USER_DATA_0	B0h	R/W	
USER_DATA_1	B1h	R/W	
BCM_EN_POLARITY	D0h		R/W
READ_K_FACTOR	D1h		R
READ_BCM_ROUT	D4h		R
SET_ALL_THRESHOLDS	D5h		R/W
DISABLE_FAULT	D7h		R/W

Page Command (00h)

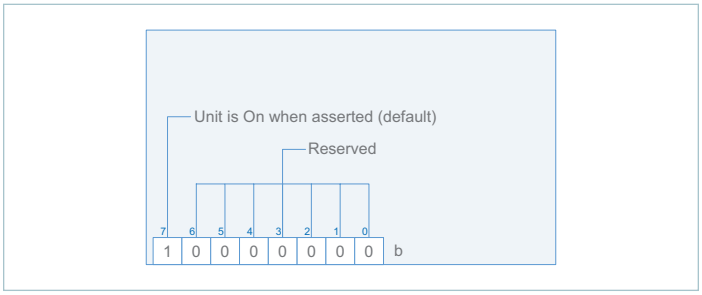
The page command data byte of 00h prior to a command call will address the PLI-specific data and a page data byte of 01h would broadcast to the BCM. The value of the Data Byte corresponds to the pin name trailing number with the exception of 00h and FFh.

Data Byte	Description
00h	PLI
01h	BCM

OPERATION Command (01h)

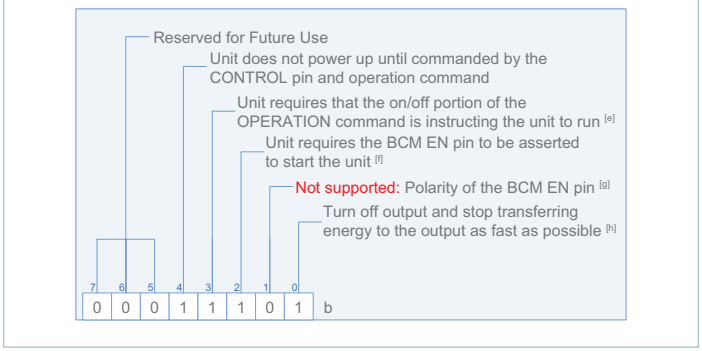
The OPERATION command and the BCM EN pin can both be used to turn on and off the connected BCM. Note that the host OPERATION command will not enable the BCM if the BCM EN pin is disabled in hardware with respect to the pre-set pin polarity. The OPERATION command provides ON/OFF control only with the BCM EN pin active.

If synchronous startup is required in the system, it is recommended to use the command from host PMBus or the BCM EN pin in order to achieve simultaneous array startup.



This command accepts only two data values: 00h and 80h. If any other value is sent the command will be rejected and a CML Data error will result.

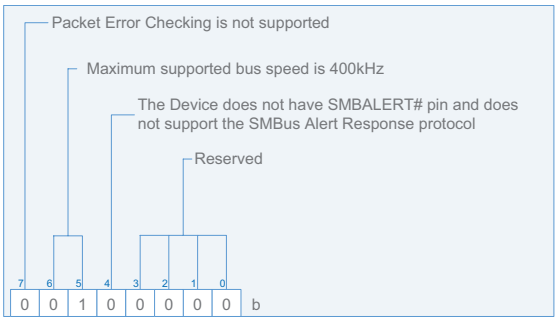
ON_OFF_CONFIG Command (02h)



[e] The BCM EN pin is ALWAYS to be asserted for powerup. The BCM_EN_POLARITY command (D0h) bit[1] defines the logic level required for the control pin (i.e BCM Enable pin) to be asserted.
[f] With respect to the BCM EN pin if used in system.
[g] See MFR_SPECIFIC_00 / BCM_EN_POLARITY to change the Polarity of the BCM Enable Pin.
[h] The BCM powertrain once disabled cannot sink current.

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted again once cleared. All faults are latched once asserted in the PLI. Registered faults will not be cleared when shutting down the BCM powertrain by recycling the BCM high side voltage or sending the OPERATION command.



CAPABILITY Command (19h)

The PLI returns a default value of 20h. This value indicates that the PMBus® frequency supported is up to 400kHz and that both Packet Error Checking (PEC) and SMBALERT# are not supported.

OT_FAULT_LIMIT Command (4Fh), OT_WARN_ LIMIT Command (51h), VIN_OV_FAULT_ LIMIT Command (55h), VIN_OV_WARN_ LIMIT Command (57h), IIN_OC_FAULT_ LIMIT Command (5Bh), IIN_OC_WARN_ LIMIT Command (5Dh)

The values of these registers are set in non-volatile memory and can only be written when the BCM is disabled.

The values of the above mentioned faults and warnings are set by default to 100% of the respective BCM model supervisory limits. However, these limits can be set to a lower value. For example: In order for a limit percentage to be set to 80%, one would send a write command with a (50h) Data Word.

Any values outside the range of (00h – 64h) sent by a host will be rejected, will not override the currently stored value and will set the Unsupported Data bit in STATUS_CML.

The SET_ALL_THRESHOLDS COMMAND (D5h) combines in one block overtemperature fault and warning limits, V_{IN} overvoltage fault and warning limits as well as I_{OUT} overcurrent fault and warning limits. A delay prior to a read command of up to 200ms following a write of new value is required.

All FAULT_RESPONSE commands are unsupported. The BCM powertrain supervisory limits and powertrain protection will behave as described in the BCM datasheet. In general, once a fault is detected, the BCM powertrain will shut down and attempt to auto-restart after a predetermined delay.

The VIN_UV_WARN_LIMIT (58h) and VIN_UV_FAULT_LIMIT (59h) are set by the factory and cannot be changed by the host. However, a host can disable the undervoltage setting using the DISABLE_FAULT COMMAND (D7h).

All FAULT_RESPONSE commands are unsupported. The BCM powertrain supervisory limits and powertrain protection will behave as described in the Electrical Specifications. In general, once a fault is detected, the BCM powertrain will shut down and attempt to auto-restart after a predetermined delay.

TON_DELAY Command (60h)

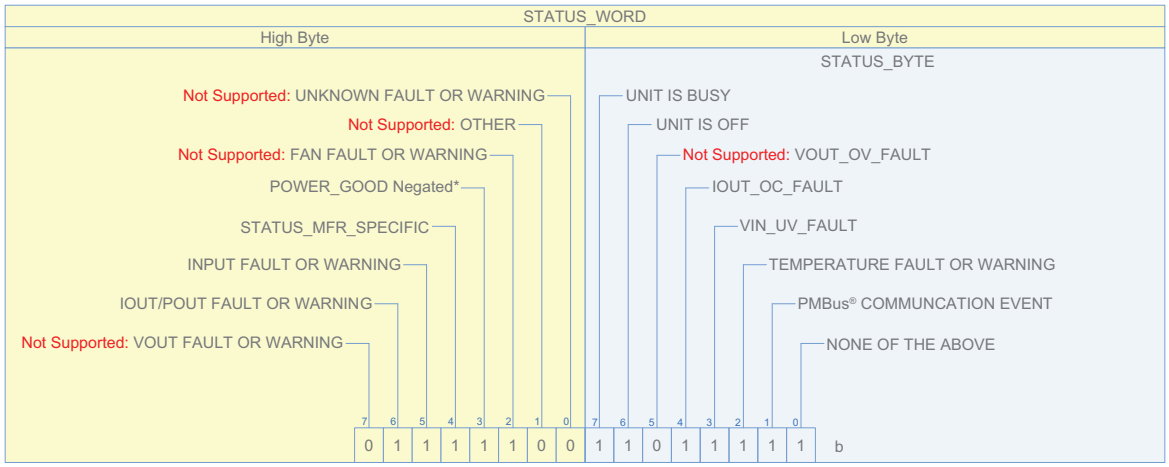
The value of this register word is set in non-volatile memory and can only be written when the BCM is disabled.

The maximum possible delay is 100ms. Default value is set to (00h). The reported value can be interpreted using the following equation.

$$TON\_DELAY_{ACTUAL} = t_{REPORTED} \bullet 10^{-3} \ (s)$$

Staggering startup in an array is possible with the TON_DELAY Command. This delay will be in addition to any startup delay inherent in the BCM module. For example: startup delay from application of V_{IN} is typically 20ms. When TON_DELAY is greater than zero, the set delay will be added to it.

STATUS_BYTE (78h) and STATUS_WORD (79h)



* equal to POWER_GOOD#

All fault or warning flags, if set, will remain asserted until cleared by the host or once the BCM and PLI +BIAS power is removed. This includes undervoltage fault, overvoltage fault, overvoltage warning, overcurrent warning, overtemperature fault, overtemperature warning, undertemperature fault, reverse operation, communication faults and analog controller shutdown fault.

Asserted status bits in all status registers, with the exception of STATUS_WORD and STATUS_BYTE, can be individually cleared. This is done by sending a data byte with one in the bit position corresponding to the intended warning or fault to be cleared. Refer to the PMBus® Power System Management Protocol Specification – Part II – Revision 1.2 for details.

The POWER_GOOD# bit reflects the state of the device and does not reflect the state of the POWER_GOOD# signal limits. The POWER_GOOD_ON COMMAND (5Eh) and POWER_GOOD_OFF COMMAND (5Fh) are not supported. The POWER_GOOD# bit is set, when the BCM is not in the active state, to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared, when the BCM is in the active state, 5ms after the powertrain is activated allowing for soft-start to elapse. POWER_GOOD# and OFF bits cannot be cleared as they always reflect the current state of the device.

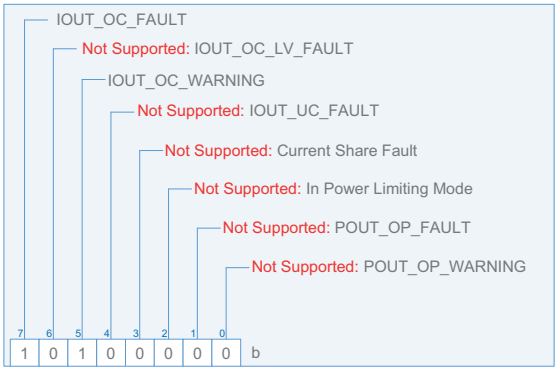
The Busy bit can be cleared using CLEAR_ALL Command (03h) or by writing either data value (40h, 80h) to PAGE (00h) using the STATUS_BYTE (78h).

Fault reporting, such as SMBALERT# signal output, and host notification by temporarily acquiring bus parent status is not supported.

If the PLI is powered through +BIAS, it will retain the last telemetry data and this information will be available to the user via a PMBus Status request. This is in agreement with the PMBus standard, which requires that status bits remain set until specifically cleared. Note that in the case where the BCM V_{IN} is lost, the status will always indicate an undervoltage fault, in addition to any other fault that occurred.

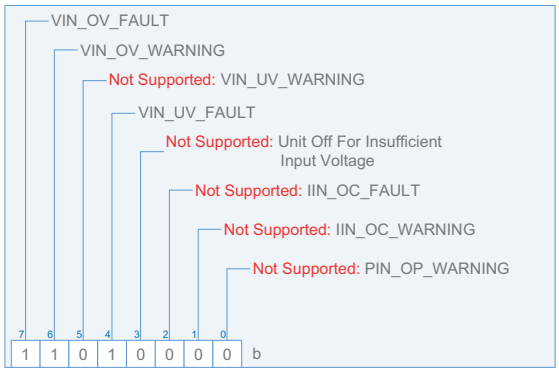
NONE OF THE ABOVE bit will be asserted if either the STATUS_MFR_SPECIFIC (80h) or the High Byte of the STATUS WORD is set.

STATUS_IOUT (7Bh)



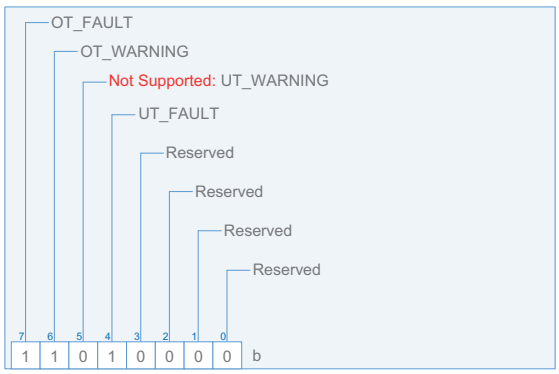
Unsupported bits are indicated above. A one indicates a fault.

STATUS_INPUT (7Ch)



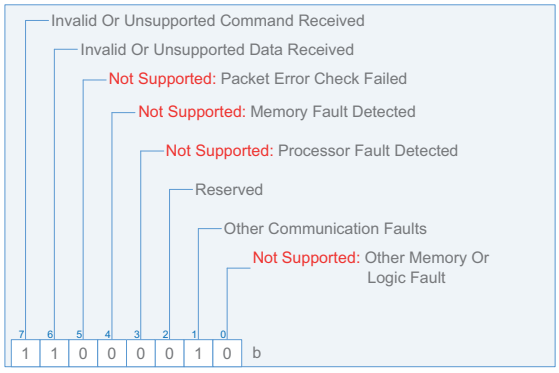
Unsupported bits are indicated above. A one indicates a fault.

STATUS_TEMPERATURE (7Dh)



Unsupported bits are indicated above. A one indicates a fault.

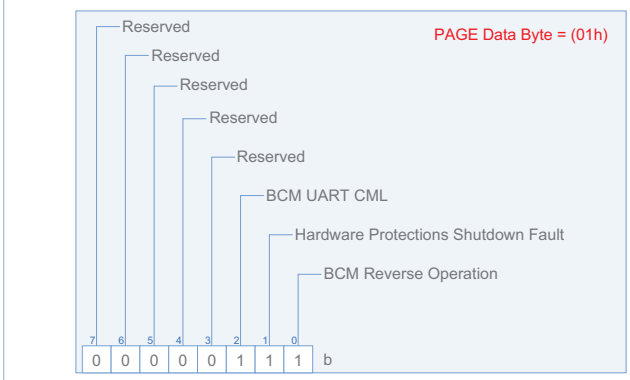
STATUS_CML (7Eh)



Unsupported bits are indicated above. A one indicates a fault.

The STATUS_CML data byte will be asserted when an unsupported PMBus® command or data or other communication fault occured.

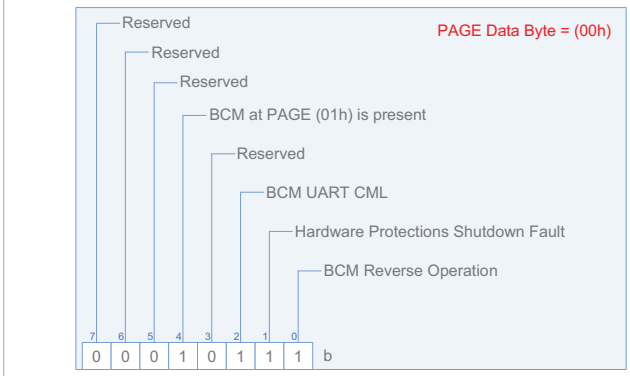
STATUS_MFR_SPECIFIC (80h)



The reverse operation bit, if asserted, indicates that the BCM is processing current in reverse. Reverse current reported value is not supported.

The BCM has hardware protections and supervisory limits. The hardware protections provide an additional layer of protection and have the fastest response time. The Hardware Protections Shutdown Fault, when asserted, indicates that at least one of the powertrain protection faults is triggered. This fault will also be asserted if a disabled fault event occurs after asserting any bit using the DISABLE_FAULTS COMMAND.

The BCM communicates with the PLI via UART communication. If the BCM UART CML bit is asserted, it may indicate a hardware or connection issue between the BCM and the PLI.



When the PAGE COMMAND (00h) data byte is equal to (00h), the BCM Reverse operation, Analog Controller Shutdown Fault, and BCM UART CML bit will return the result of the active BCM. The BCM UART CML will also be asserted if the active BCM stops responding. The BCM must communicate at least once to the internal controller in order to trigger this FAULT. The BCM UART CML can be cleared using the PAGE (00h) CLEAR_FAULTS (03h) Command.

READ_VIN Command (88h)

If PAGE data byte is equal to (01h), command will return the BCM's input-side voltage in the following format:

$$V_{IN\_ACTUAL} = V_{IN\_REPORTED} \bullet 10^{-1} \ (V)$$

READ_IIN Command (89h)

If PAGE data byte is equal to (01h), command will return the BCM's input-side current in the following format:

$$I_{IN\_ACTUAL} = I_{IN\_REPORTED} \bullet 10^{-3} \ (A)$$

If PAGE data byte is equal (00h), command will also return the BCM's input-side current.

READ_VOUT Command (8Bh)

If PAGE data byte is equal to (01h), command will return the BCM's output-side voltage in the following format:

$$V_{OUT\_ACTUAL} = V_{OUT\_REPORTED} \bullet 10^{-1} \ (V)$$

READ_IOUT Command (8Ch)

If PAGE data byte is equal to (01h), command will return the BCM's output-side current in the following format:

$$I_{OUT\_ACTUAL} = I_{OUT\_REPORTED} \bullet 10^{-2} \ (A)$$

If PAGE data byte is equal (00h), command will also return the BCM's output-side current.

READ_TEMPERATURE_1 Command (8Dh)

If PAGE data byte is equal to (01h), command will return the BCM's temperature in the following format:

$$T_{ACTUAL} = \pm T_{REPORTED} \ (^{o}C)$$

If PAGE data byte is equal (00h), command will also return the BCM's temperature.

READ_POUT Command (96h)

If PAGE data byte is equal to (01h), command will return the BCM's output-side power in the following format:

$$P_{OUT\_ACTUAL} = P_{OUT\_REPORTED} \ (W)$$

If PAGE data byte is equal to (00h), command will also return the BCM's output-side power.

READ_PIN Command (97h)

If PAGE data byte is equal to (01h), command will return the BCM's input-side power in the following format:

$$P_{IN\_ACTUAL} = P_{IN\_REPORTED} \bullet 10^{-1} \ (W)$$

If PAGE data byte is equal to (00h), command will also return the BCM's input-side power.

MFR_VIN_MIN Command (A0h), MFR_VIN_MAX Command (A1h), MFR_VOUT_MIN Command (A4h), MFR_VOUT_MAX Command (A5h), MFR_IOUT_MAX Command (A6h), MFR_POUT_MAX Command (A7h)

These values are set by the factory and indicate the device input-side/output-side voltage and output-side current range and output-side power capacity.

If the PAGE data byte is equal to (00h – 01h), commands report the rated BCM input-side voltage minimum and maximum in Volts, output-side voltage minimum and maximum in Volts, output-side current maximum in Amperes and output-side power maximum in Watts.

USER_DATA_0 (B0h) and USER_DATA_1 (B1h) Command

A direct communication to the PLI controller for access of User Data by the B0h and B1h command is supported only for PAGE (00h). The supported command accesses 28 bytes of user data defined in the following table. Deviation from this table generates a communication error in STATUS_CML register. This command allows write and read of 28 bytes of data to and from non-volatile memory. A write stores a fixed length data payload of 28 bytes in EEPROM. A read will return the same 28 byte fixed length payload. The user shall use the BLOCK READ/WRITE command structure specified in SMBus™ specification also listed as example in this document.

USER_DATA_0 Command (B0h)

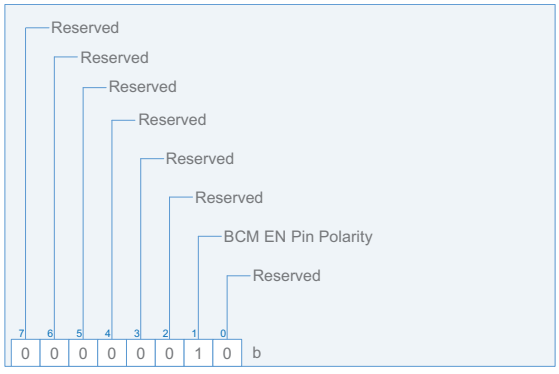
Byte	Values	Description
0	See table below	Action Description Byte
1:25	Data_1, Data_2, ..., Data_25	Data (28 user-programmable bytes)
26.0	0 or 1	Overtemperature Fault
26.1	0 or 1	Overcurrent Fault
26.2	0 or 1	UART BCM Fault, sets when PLI is not able to receive any data from connected BCM
26.3	0 or 1	UART PLI Fault, sets when PLI is unable to transmit any data to connected BCM
27:28		Reserved

Byte	Values	Description
0	0	Reserved
	1	**Write**: Write the 28-byte user data, in which the first 25 bytes is password protected and the last 3 bytes are readable and only reset to ZERO. The 25 bytes are write-protected by default when powered on.
	2	Reserved
	3	**Set WR Protection:** Byte 1:28 – 0xff **Remove WR Protection:** Byte 1:28 – 0x00
	4	**Write 3-byte unprotected data**: Each of the 3 bytes can only be reset to ZERO. All other values will be rejected. Byte 1:25 – xx (Don't Care) Byte 26:28 – Data_0, …, Data_2

USER_DATA_1 Command (B1h)

Byte	Values	Description
0	1: Write	Write
1:28	Data_1, Data_2, ..., Data_28	Data (28 user-programmable bytes)

BCM_EN_POLARITY Command (D0h)



The value of this register is set in non-volatile memory and can only be written when the BCM is disabled. When PAGE COMMAND (00h) data byte is equal to (01h), this command defines the polarity of the BCM EN pin. If BCM_EN_POLARITY is set, the BCM will start up once V_{IN} is greater than the under voltage threshold. The BCM EN PIN is internally pulled-up to 3.3V. If the BCM_EN_POLARITY is cleared, an external pull down is then required. Applying V_{IN} greater than the undervoltage threshold will not suffice to start the BCM.

READ_K_FACTOR Command (D1h)

If PAGE data byte is equal to (01h), command will return the BCM's K factor in the following format:

$$K\_FACTOR_{ACTUAL} = K\_FACTOR_{REPORTED} \bullet 2^{-16} \ (V/V)$$

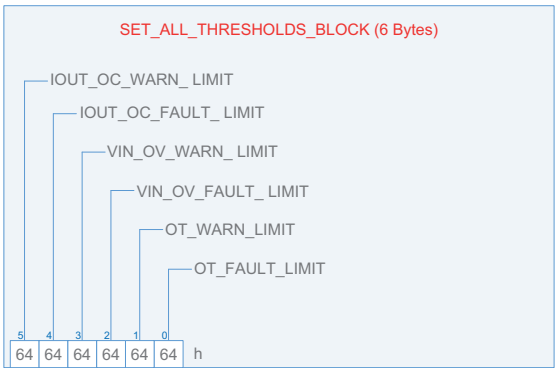
The K factor is defined in the BCM to represent the ratio of the transformer winding and hence is equal to V_{OUT} / V_{IN}.

READ_BCM_ROUT Command (D4h)

If PAGE data byte is equal to (01h), command will return the BCM's

$$BCM\_ROUT_{ACTUAL} = BCM\_ROUT_{REPORTED} \bullet 10^{-5} \ (\Omega)$$

output-side resistance in the following format:



SET_ALL_THRESHOLDS Command (D5h)

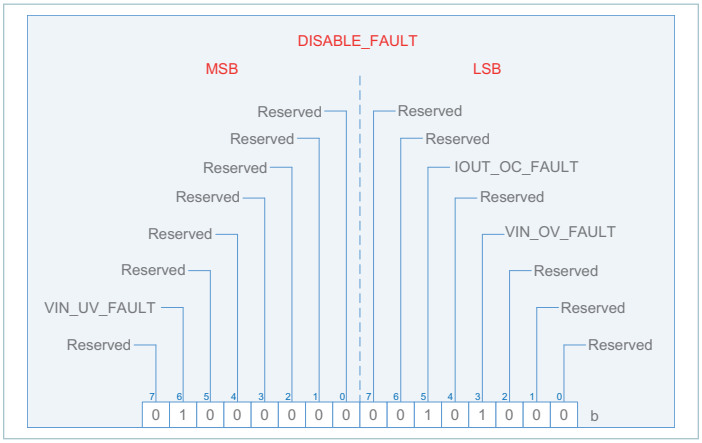
The values of this register block are set in non-volatile memory and can only be written when the BCM is disabled.

This command provides a convenient way to configure all of the limits, or any combination of limits described previously using one command.

V_{IN} overvoltage, overcurrent and overtemperature values are all set to 100% of the specified supervisory limits by default and can only be set to a lower percentage.

To leave a particular threshold unchanged, set the corresponding threshold data byte to a value greater than (64h).

DISABLE_FAULT Command (D7h)



Unsupported bits are indicated above. A one indicates that the supervisory fault associated with the asserted bit is disabled.

The values of this register block are set in non-volatile memory and can only be written when the BCM is disabled.

This command allows the host to disable the supervisory faults and respective statuses. It does not disable the powertrain analog protections or warnings with respect to the set limits in the SET_ALL_THRESHOLDS Command.

The input-side undervoltage can only be disabled to a pre-set low limit as specified in the monitored Telemetry Functional Reporting Range.

Data Transmission Faults Implementation

This section describes data transmission faults as implemented in the PLI.

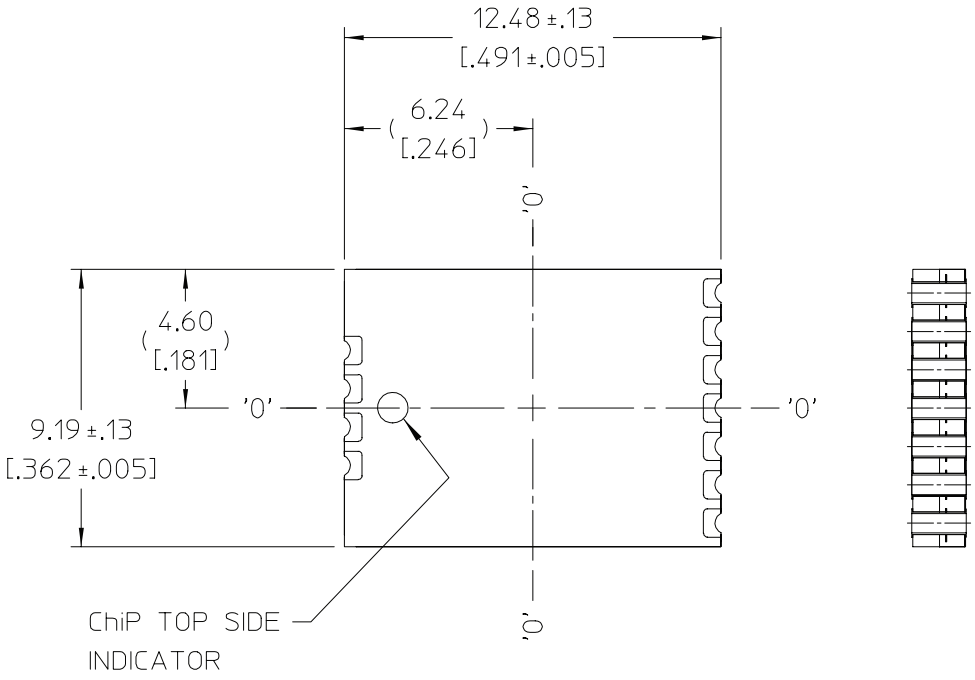
Section	Description	Responsible to Host		Status Byte	Status CML		Notes
		NAK	FFh	CML	Other Fault	Unsupported Data	
10.8.1	Corrupted Data						No response; PEC not supported
10.8.2	Sending too few bits			X	X		
10.8.3	Reading too few bits			X	X		
10.8.4	Host sends or reads too few bytes			X	X		
10.8.5	Host sends too many tytes	X		X		X	
10.8.6	Reading too many bytes		X	X	X		
10.8.7	Device busy	X	X				Device will ACK own address BUSY bit in STATUS_BYTE even if STATUS_WORD is set

Data Content Faults Implementation

This section describes data content faults as implemented in the PLI.

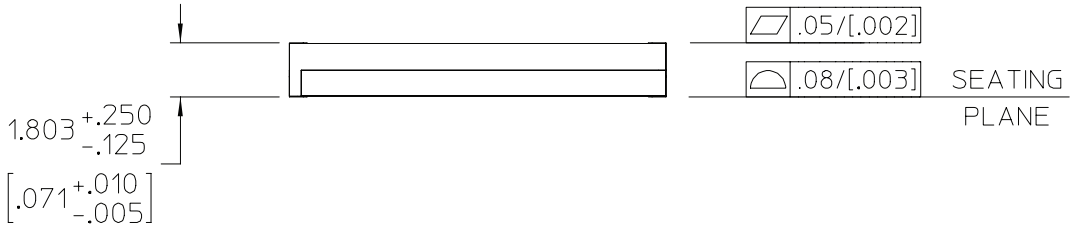
Section	Description	Responsible to Host	Status Byte	Status CML			Notes
		NAK	CML	Other Fault	Unsupported Command	Unsupported Data	
10.9.1	Inproperly set read bit in the address byte	X	X	X			
10.9.2	Unsupported command code	X	X		X		
10.9.3	Invalid or unsupported data		X			X	
10.9.4	Data out of range		X			X	
10.9.5	Reserved bits						No response; not a fault

Product Outline Drawing – Top View



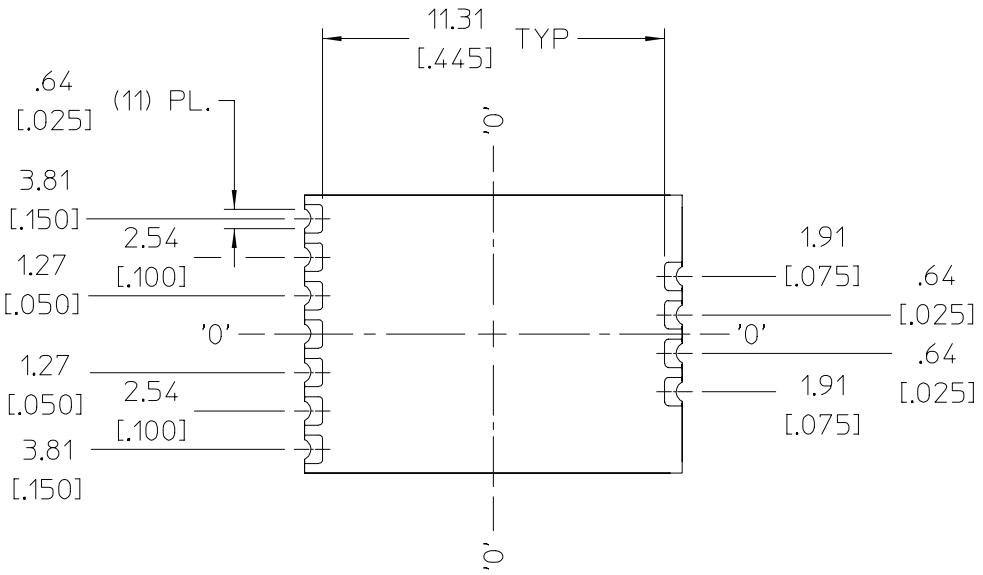
TOP VIEW
(COMPONENT SIDE)

1209 PLI



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE MM [INCH]

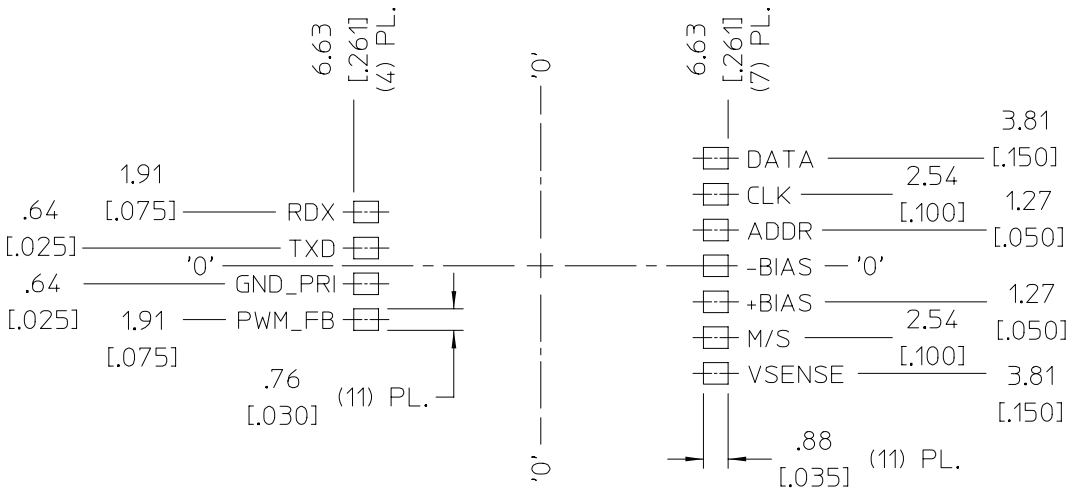
Product Outline Drawing – Bottom View



BOTTOM VIEW

1209 PLI

Recommended Land Pattern



RECOMMENDED LAND PATTERN,
1209 PLI
(COMPONENT SIDE)

Revision History

Revision	Date	Description	Page Number(s)
1.0	10/29/18	Initial release	n/a
1.1	02/27/19	Updated EN pin reference for secondary side Reorganized signal tables Updated EN_SEC signal characteristics Updated supported command list function descriptions Updated 80h description	2, 3, 4, 9 5 – 7 6 11 18
1.2	08/11/20	Updated terminology	9, 10, 12, 13, 17

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