SOSA™ Aligned Power Supply

SOS028H3U480N000

SOSA-Aligned DC-DC Converter with NED

Features & Benefits

- Open VPX – VITA 62
- 18 – 45V input voltage range
- Nuclear event detect (NED) signal input per VITA 62.0, 350µs response
- 480W output power
- 3U Open VPX power supply
- Conduction cooled
- IPMI 46.11 monitoring and control
- Input voltage reverse-polarity protection
- Remote voltage sensing for +12V and +3.3V auxiliary
- Overcurrent, overvoltage and overtemperature protections
- IPC-A-610 class 3
- No aluminum electrolytic capacitors
- Enable, inhibit, system reset and power fail controls
- Designed to meet military standard compliance: [a]
  - MIL-STD-704F
  - MIL-STD-461G
  - MIL-STD-810G
  - MIL-STD-1275E
  - RTCA/DO-160G

Typical Applications

- VPX power modules
- Avionics
- Shipborne electronics

Product Description

The Vicor SOSA-aligned power supply is a COTS power supply that is designed for 3U Open VPX systems that are developed to the SOSA standard. The module utilizes Vicor proprietary technology to enable high efficiency and power density for this highly rugged, conduction-cooled model.

[a] See detailed specifications; contact Vicor Applications Engineering for report details.

Note: Product images may not highlight current product markings and cosmetic features.

Connector Pin Configuration

ROWS	POWER			SIGNAL								POWER				
				1	2	3	4	5	6	7	8					
D	P1	P2	LP1									P3	P4	P5	LP2	P6
C																
B																
A																

3U P0 Connector

Note: See mechanical drawing on page 30 for connector information.

Connector Pin Descriptions

Pin	Function / Name	Description
P1	–DC_IN	V_{IN-}
P2	+DC_IN	V_{IN+}
LP1	CHASSIS	Chassis
A1, B1, C1, D1	No Connection	
A2	No Connection	
B2	FAIL*	When any of the output is not within specification, FAIL* signal will be driven low to indicate a failure
C2	INHIBIT*	Input control signal as defined in VITA 62, referenced to SIGNAL_RETURN
D2	ENABLE*	Input control signal as defined in VITA 62, referenced to SIGNAL_RETURN
C3	NED	Input as defined by VITA 62, referenced to NED_RETURN
D3	NED_RETURN	Return for NED signal
A3, B3, C3, D3	No Connection	
A4, B4, C4, D4	No Connection	
A5	*GA0	Geographical address defined by VITA 46.11
B5	*GA1	Geographical address defined by VITA 46.11
C5	SM0 (I^2C Clock)	Primary I^2C communication bus
D5	SM1 (I^2C Data)	
A6	I^2C Clock	Redundant I^2C communication bus
B6	I^2C Data	
C6	No Connection	
D6	SYS_RESET*	System Reset is actively low
A7, B7, C7	No Connection	
D7	SIGNAL_RETURN	Ground pin for control and communication signals; internally Kelvin-connected to POWER_RETURN; should be connected to POWER_RETURN on the backplane
A8	$+12V_{SENSE}$	VS1 sense; shall be connected at point-of-load or on the backplane to corresponding voltage output
B8	$+3.3V_{SENSE}$	VAUX sense; shall be connected at point-of-load or on the backplane to corresponding voltage output
C8	No Connection	
D8	SENSE_RETURN	Shall be connected to POWER_RETURN either remotely or at the connector
P3	VS1	+12V main output
P4, P5	POWER_RETURN	Common output voltage return pin
LP2	VAUX	+3.3V auxiliary output
P6	VS1	+12V main output

Part Ordering Information

Part Number	Product Grade	Special Feature	Factory-Configured Options
SOS028**H**3U480**N000**	**H** = –40 to 85°C	**N** = NED	**000** = Programmable, SOSA standard keying [b]

[b] Refer to connector components table, page 21. For custom keying, please contact Vicor Applications Engineering.

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
Total Output Power	Combined outputs for all rails		480	W
Operational Input Voltage	+IN to –IN, 100V 50ms operation MIL-STD-1275E surge only	–0.5	100	V
Operating Temperature	Measured at card edge	–40	85 [c]	°C
Storage Temperature		–40	125	
Isolation Voltage IN to OUT			500	V_{DC}
Isolation Voltage IN to CASE			500	V_{DC}
Isolation Voltage OUT to CASE			100	V

[c] Operating temperature is at nominal line in and aggregate maximum load. See de-rating curve below. See also overtemperature protection, page 11.

Caution

An external NED-activated disconnect function on power input is required, between this power supply and its power source, either at the source or on the backplane, where the disconnect response is within ~10µs from the NED signal going high. Failure to do so will cause damage to this power supply and to the power source.

Specified Operating Area

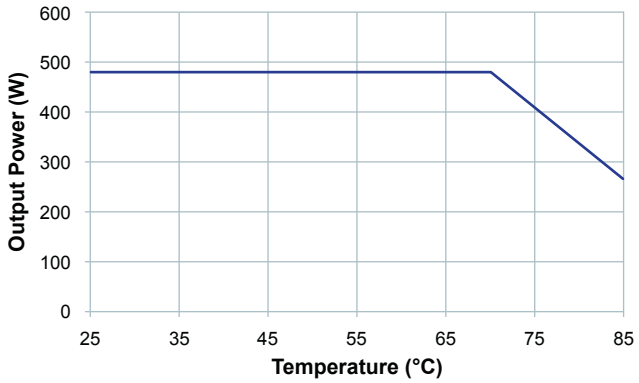


Figure 1 — *Thermal specified operating area, aggregate load at nominal line*

Electrical Characteristics

All data at nominal line and nominal load unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Overall System Characteristics						
System Efficiency		Nominal line, 25% aggregate loads		83		%
		Nominal line, 50% aggregate loads		87.0		
		Nominal line, 100% aggregate loads		87.5		
Power Input Characteristics						
Operating Input Voltage Range	V_{IN}		18	28	45	V
Input Current (No Load)	I_{IN-NL}	28V Input, enable asserted, inhibit de-asserted		0.50	1.0	A
Inrush Current	I_{INRUSH}	Peak no load, nominal line, high line; see Figure 5		70	120	A
Power On to +3.3V Auxiliary Output Delay		If ENABLE* is tied to signal ground	100	150	200	ms
Input Undervoltage Lockout					11.9	V
Input Undervoltage Lockout Recovery					17.8	V
MIL-STD-1275E Operational Characteristics						
Initial Engagement Surge (IES) Low Line Limit					11.9	V
Minimum Sustained IES Time Limit			5			s
Minimum Sustained Cranking Disturbance Time Limit		$12V < V_{IN} < 16V$	30			s
Minimum Sustained Cranking Disturbance Output Power				510		W
VS1: +12V Output						
Output Voltage Set Point	V_{VS1}		11.85	12.1	12.15	V
Output Regulation Over Line & Load				200		mV
Output Voltage Ripple / Noise		Nominal line from 4A load to full load		50	120	mV_{P-P}
Rated Output Current	I_{R-VS1}	VS1 total			40	A
Maximum Operating Transmission Voltage Drop	V_{TD-VS1}				0.5	V
Maximum Output Capacitance	C_{O-VS1}				9	mF
Soft-Start Ramp Time	t_{SS-VS1}	All full load with max C_{O-VS1}		10		ms
VAUX: +3.3V Output						
Output Voltage Set Point	V_{VAUX}		3.25	3.35	3.45	V
Output Regulation Over Line & Load				100	150	mV
Output Voltage Ripple / Noise		Nominal line over load range, 20MHz BW; measured with 1µF and 10µF ceramic capacitor			50	mV_{P-P}
Rated Output Current	I_{R-VAUX}				15	A
Soft-Start Ramp Time	$t_{SS-VAUX}$	All full load with max C_{O-VAUX}			5	ms
Overcurrent Trip Threshold	I_{OCP_VAUX}		18			A

Signal Characteristics

All of the following plots are at nominal line and 480W aggregate load unless otherwise noted.

ENABLE*: Enable*

- The ENABLE* pin or control register bit enables and disables the +3.3V AUX output of the power supply.
- The ENABLE* pin has an internal pull-up to VCC and is referenced to the Signal Return pin of the power supply.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input	Any	ENABLE* Enable Threshold	$V_{ENABLE-EN}$				0.8	V
		ENABLE* Disable Threshold	$V_{ENABLE-DIS}$		2.0			V
		Internally Generated V_{CC}	V_{CC}		3.21	3.30	3.39	V
		ENABLE* Internal Pull-Up Resistance to V_{CC}	$R_{ENABLE-INT}$		49	51	52	kΩ
		ENABLE* Enable Debounce Delay	t_{D-EN-E}		3	5		ms
		ENABLE* Disable Debounce Delay	t_{D-EN-D}		3	5		ms

INHIBIT*: Inhibit*

- The INHIBIT* pin enables and disables all outputs except +3.3V_{AUX} if $V_{ENABLE-EN}$ threshold has been met.
- The INHIBIT* pin has an internal pull up to V_{CC} and is referenced to the Signal Return pin of the power supply.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input	Any	INHIBIT* Enable Threshold	$V_{INHIBIT-EN}$	Status register bit 4 should be 0 (default) for digital input control line to have priority	2.0			V
		INHIBIT* Disable Threshold	$V_{INHIBIT-DIS}$				0.8	V
		Internally Generated V_{CC}	V_{CC}		3.21	3.30	3.39	V
		INHIBIT* Internal Pull-Up Resistance to V_{CC}	$R_{DISABLE-INT}$		49	51	52	kΩ
		INHIBIT* Enable Debounce Delay after ENABLE*	t_{D-IN-E}		3	5		ms
		INHIBIT* Disable Debounce Delay	t_{D-IN-D}		3	5		ms
		Lockout Delay Between Consecutive INHIBIT* Enables	t_{D-IN-L}		3	5		ms

Signal Characteristics (Cont.)

All of the following plots are at nominal line and 480W aggregate load unless otherwise noted.

GA0*, GA1*: Geographical Address

- The GA0* and GA1* pins sets the I^2C address of the power supply. Geographical address is set at start up and cannot be changed without a power cycle.
- The GA0* and GA1* pins have an internal pull-up to V_{CC} and is referenced to the Signal Return pin of the power supply.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input	Start Up	Address Pins Low Threshold	V_{ADDR-L}				0.8	V
		Address Pins High Threshold	V_{ADDR-H}		2.0			V
		Internally Generated V_{CC}	V_{CC}		3.21	3.30	3.39	V
		ENABLE* Internal Pull-Up Resistance to V_{CC}	$R_{ADDR-INT}$		49	51	52	kΩ
		Address Pins Debounce Delay	t_{D-ADDR}		5			ms

FAIL*, SYSRESET* & LED

- The power supply has one two color LED located on the ejector edge of the power supply.
- The LED is either GREEN or RED depending on the state of operation. FAIL* and SYSRESET* lines are set with the LED.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Outputs	Steady RED	SYSRESET*	V_{SYSRST}	Start up: input voltage operating threshold $V_{UV-IN} < V_{IN} < V_{OV-IN}$ has been met; if steady RED persists for >100ms, a critical system fault has been detected during start up	0.0		0.8	V
		FAIL*	V_{FAIL}		0.0		0.8	V
	Blinking GREEN	SYSRESET*	V_{SYSRST}	>100ms after $V_{UV-IN} < V_{IN} < V_{OV-IN}$ has been met; power supply is ready for use	2.0		3.5	V
		FAIL*	V_{FAIL}		2.0		3.5	V
	Steady GREEN	SYSRESET*	V_{SYSRST}	All outputs are OK and ENABLE* is pulled low	2.0		3.5	V
		FAIL*	V_{FAIL}		2.0		3.5	V
	Blinking RED	SYSRESET*	V_{SYSRST}	Power supply has encountered a OT, OV, UV, OC or critical system failure during operating	2.0		3.5	V
		FAIL*	V_{FAIL}		0.0		0.8	V
	Fast Blinking GREEN	None	-	SW priority is set by 0x55 status command	-	-	-	-
	Blinking Alternate GREEN/RED	None	-	Battle Override mode is enabled successfully by 0x55 status command	-	-	-	-

NED

- Isolated input to the processor, which then delivers timed controls to crowbar circuits across the capacitance of the various housekeeping circuits, power supply outputs, and input power circuits (input capacitance, EMI filter, 1275E response circuit, etc.).
- All voltages reduced to < 0.6V in ≤ 350µs from when input goes high.
- Although input has filtering, external filtering is recommended to avoid unintended NED activation by external system noise

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Input	Active High	Input Threshold	$V_{IN(H)}$	5V is lowest threshold	8.0		12.0	V

Application Characteristics

All of the following plots are at nominal line and 480W aggregate load unless otherwise noted.

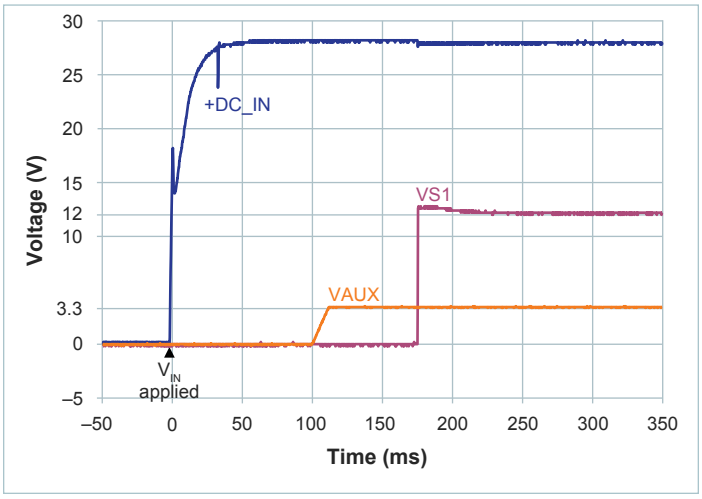


Figure 1 — *Response time from V_{IN} applied to outputs available; under 200ms start; V_{IN} = 28V; 20% load*

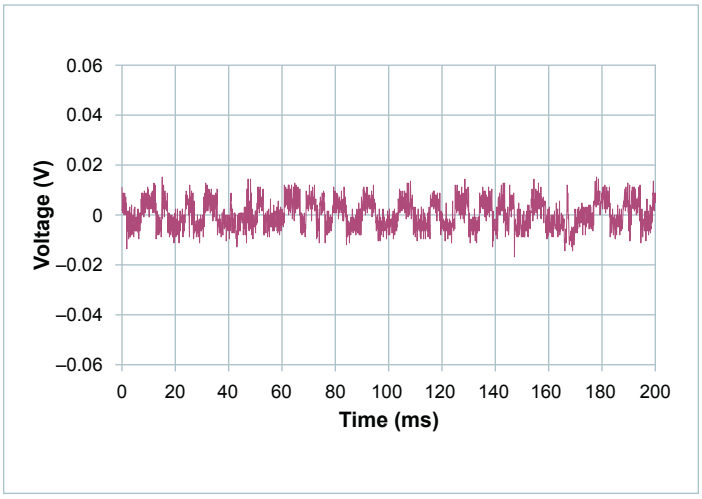


Figure 2 — *VS1 (+12V) ripple at 10% load (4A), AC-coupled*

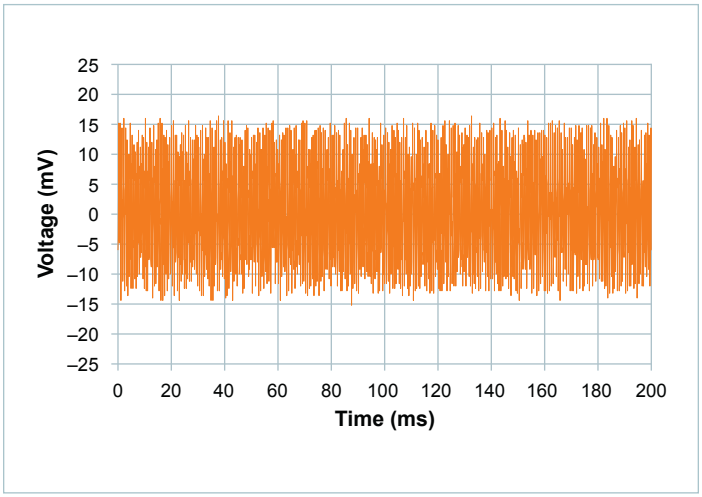


Figure 3 — *AUX (+3.3V) ripple, AC-coupled*

General Characteristics

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Per VITA62		6.634		in
Width	W	Per VITA62		3.937		in
Height	H	Per VITA62		1.55		in
Weight		Product weight		23.7 [672]		oz [g]
Wedge-Lock Torque		Manufacturer's recommended value		7		in·lbs
Thermal						
Operating Temperature	$T_{WEDGE-LOCKS}$		–40		85	°C
Assembly						
Storage Temperature			–40		125	°C

Signal Pin Functions

ENABLE* & INHIBIT*

Enable and Inhibit pins express active low logic. Table 1 has the truth table for the output state of the power supply. It is necessary to avoid the indeterminate output state where 0.8 – 2.0V is applied to the ENABLE* or INHIBIT* pins.

A digital debounce filter is present on the signals of both pins to prevent false transitions. The ENABLE* and INHIBIT* also have a minimum delay between successive output enable transitions to prevent repeated starts into high capacitance loads. See detailed specifications for delays time limits.

ENABLE* Pin	INHIBIT* Pin	Output State and Notes
< 0.8V, Logic 0	> 2.0V or NO, Logic 1	All outputs available
< 0.8V, Logic 0	< 0.8V, Logic 0	Only +3.3V_{AUX} output available
> 2.0V or NO, Logic 1	Any	All outputs disabled
0.8V > $V_{ENABLE*}$ < 2.0V	0.8V > $V_{INHIBIT*}$ < 2.0V	Indeterminate state and must be avoided

Table 1 — *ENABLE & INHIBIT logic*

Geographical Address: GA0* & GA1*

Geographical address pins also exhibit active low logic. Table 2 has the truth table for the output state of the power supply. It is necessary to avoid the indeterminate state where 0.8 – 2.0V is applied to either address pins. A digital debounce filter is present on the signals of both pins to incorrect address assignment.

The geographical address is static and set on power up. The power supply's address cannot not change until power has been cycled and the states of the address pins have been modified before power up.

GA1*	GA0*	Power Supply Address
> 2.0V or NO, Logic 1	> 2.0V or NO, Logic 1	20h
> 2.0V or NO, Logic 1	< 0.8V, Logic 0	21h
< 0.8V, Logic 0	> 2.0V or NO, Logic 1	22h
< 0.8V, Logic 0	< 0.8V, Logic 0	23h
0.8V > V_{GA1*} < 2.0V	0.8V > V_{GA0*} < 2.0V	Indeterminate state and must be avoided

Table 2 — *Geographical address assignment*

I²C Ports:

Both primary and redundant I²C ports have the same address set by the Geographical Address pins and identical functionality. There is a bidirectional buffer on both clock and data lines with internal pull ups on the IPMC and external pulls on the back plane to +3.3V are required.

FAIL*

This signal line is open drain and tracks SYSRESET* when the unit is powering up or pulled down to SIGNAL_RETURN when any of the outputs are out of specification. A pull up resistor is expected on the backplane per section 4.6.3.7 of VITA 62.

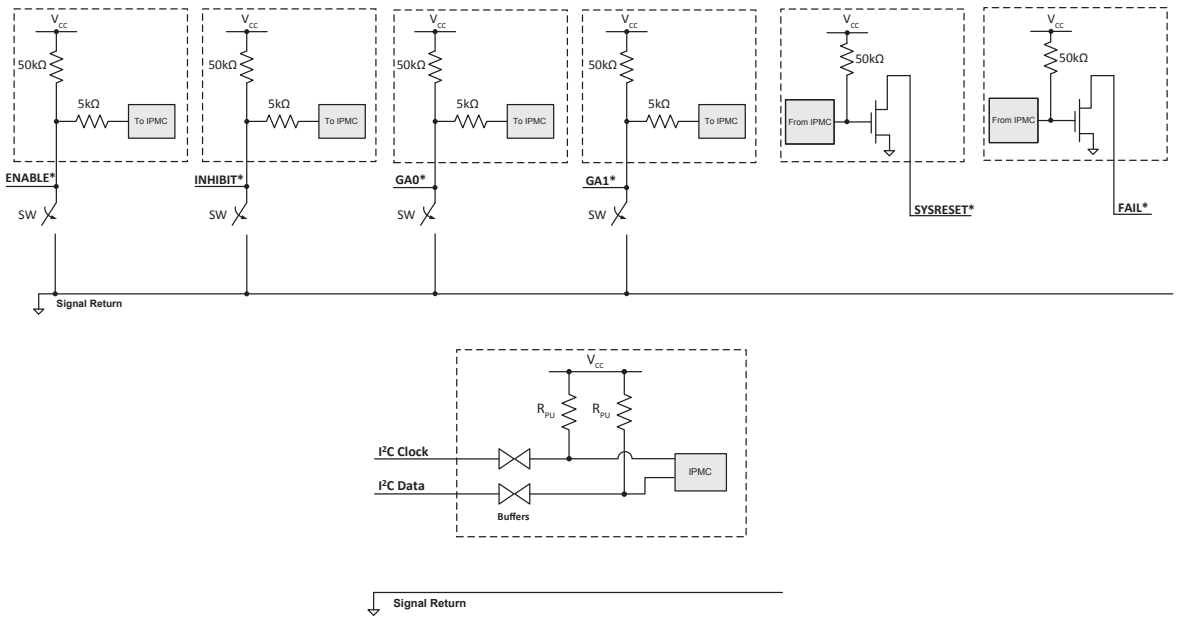
SYSRESET*

This signal line is open drain and is pulled down to SIGNAL_RETURN when the unit is powering up. The line is released when the power supply is ready for control. Appropriate pull-up/pull-down resistors are expected on the back plane per VITA 46 section 7.3.9.

SIGNAL RETURN

SIGNAL RETURN is used as the reference for signals pin connections and is to be tied to POWER_RETURN on the backplane per section 4.6.3.10-1 of VITA 62.

Typical External Circuits for Signal Pins (ENABLE*, INHIBIT*, GA0*, GA1*, SYSRESET*, FAIL* and I²C Channels)



Card Edge Temperature Sensors

The PCBA card edge temperature sensor internal to the power supply is mounted on the edge of the PCBA card edge. Consequently, the temperature sensor measures a temperature that is generally higher than the heat-sink-to-rail mounting interface and lower than the hot spot of the internal converters in the power supply.

Response from the power supply to I^2C command 0x21 provides the temperature measured by the internal sensor that reads the higher temperature. This temperature can exceed 85°C. I^2C command 0x92 will respond with both PCB mounted temperature sensors.

Power Limits

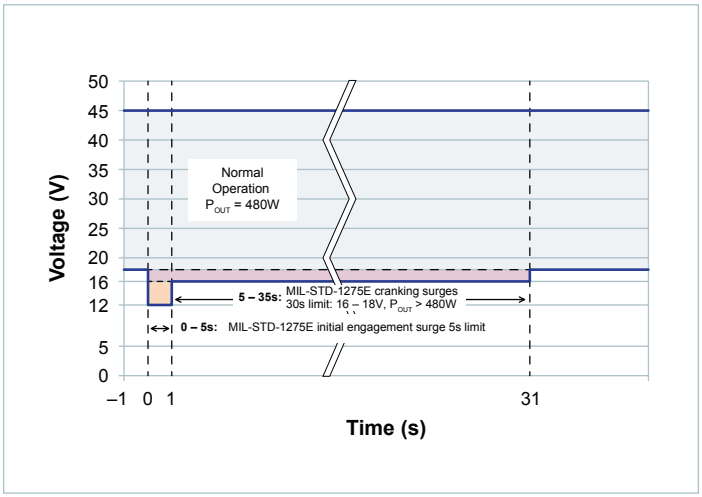


Figure 4 — *Power-time limits during transient cranking disturbances*

Per MIL-STD-1275E, the Initial Starter Engagement (ISE) can cause the nominal 28V bus to drop to 12V for 5s. Once the engine is cranking the voltage will be in the range of 16 – 18V and the full combined unit power of 480W is available for a maximum 35s.

Fault Operation

See Table 5 for nonrecoverable fault thresholds which trigger a fault and shut down/restart of the outputs of the supply.

Input Voltage Protection (IOVP)

If the input voltage to the power supply drops below $V_{UV\text{-}IN}$ or exceeds $V_{OV\text{-}IN}$ for at least 1ms, the power supply will shut down all outputs and digital communication lines until input voltage is within operating range V_{IN}. Triggering I_{OVP} has the same effect as power cycling the power supply. Supply currents and voltages are sampled every 200µs.

Output Voltage Protection (OOVP)

The power supply measures voltage from the remote-sense lines as well as the voltages on the VITA connector which do not include remote sense drop.

The FAIL* line will be asserted (pulled low) when output voltage at the connector of the power supply is greater than the nonrecoverable limit of any output. OVP will also shut down the outputs until the output voltage of the converter is within specification. The power supply will automatically restart the outputs every 1s until the fault clears.

Overcurrent Protection (OCP)*

During an overcurrent fault on any output, all outputs will shut off and the FAIL* line will be asserted. The power supply will automatically try to restart outputs every 1s if the fault has cleared.

Overtemperature Protection (OTP)

The power supply will go into overtemperature protection and shut down all outputs when either internal temperature sensor measures 95°C. The power converter will recover for normal operation when the internal temperature has dropped by 20°C.

At 85°C the Bit-5 of the Status Register (0x55) will clear if the system manager sets Bit-5 to 1 which will indicate the power supply is within 10°C from shutting down.

Standards Compliance

MIL-STD-461F		
CS106	±200V, 10µs	Designed to meet
	±400V, 5µs	Designed to meet
CS115	Bulk input power cables	Designed to meet
	Bulk output power cables	Designed to meet
CS116	Bulk input power cables	Designed to meet
	Bulk output power cables	Designed to meet
MIL-STD-461G		
CE102	Basic curve	Designed to meet
CS101	Figure CS101-1, Cuve #2	Designed to meet
CS114 Curve 5	Input power lead	Designed to meet
	Bulk input power cables	Designed to meet
CS118	Per test standard	Designed to meet
MIL-STD-704F		
LDC103 – Voltage Distortion Spectrum		Designed to meet
LDC105 – Normal Voltage Transients		Designed to meet
LDC302 – Abnormal Voltage Transients		Designed to meet
MIL-STD-810G		
Vibration, Method 514.5 Procedure I	1 – 100Hz PSD increasing at 3dB/octave	Designed to meet
	100 – 1000Hz PSD = 0.1g2/Hz	Designed to meet
	1000 – 2000Hz PSD decreasing at 6dB/octave	Designed to meet
Operating Shock, Method 516 Procedure I	40g, 11ms shock half-sine	Designed to meet
	40g, 11ms, terminal saw-tooth shock pulses in all three axes	Designed to meet
MIL-STD-1275E		
All Sections	12V initial engagement surge limited to 510W output power	Designed to meet
RTCA/DO-160G		
Section 15: ESD		Designed to meet
Section 17: Voltage Spike, Category A		Designed to meet
IEC 61000-4-2		
ESD, Level 4	±15kV Air Discharge	Designed to meet
VITA 47		
Humidity	Method 507 per VITA 47 Section 4.6	Designed to meet
Operating Temperature	VITA 47 Section 4.1.2 class CC4	Designed to meet
Temperature Cycling	MIL-STD-202 Method 107 per VITA 47 Section 4.3	Designed to meet
Altitude	1,500ft below sea level to 70,000ft above sea level	Designed to meet
Fungus Resistance	MIL-STD-810G, Method 508 per VITA47 Section 4.10	Designed to meet
Corrosion Resistance	ASTM G85, Annex A4, cycle A4.4.4.1 per VITA 47 Section 4.12	Designed to meet

I²C Sensor Commands

Commands are sent by SMBus-compatible packets over the I²C physical interface. The I²C bus will communicate at 100kHz. Pull-up resistors to +3.3V are expected on the system backplane.

Two pins, labeled *GA1 and *GA0 are provided at each power supply slot, where *GA1 and *GA0 are defined to be active (SET) when low. The power supply will respond to I²C address 010 00[GA1][GA0].

The power supply supports commands to read sensor data from the power supply without utilizing VITA 46.11 or IPMI. The commands are similar to register reads in from I²C memory and function in a parent/child configuration. Unlike VITA 46.11 which is a multi-parent protocol, commands defined in this section are parent-write and parent-read.

Table 3 shows the following transmission pattern for reading power supply rail temperatures with command 0x92 using the parent-write/parent-read transmission format. In all non-VITA 46.11 commands, the parent requests the data from the child, which is the power supply.

IPMB Byte Number	Hex Byte	Clock Pulses Generated By	Data Pulses Generated By	Comment	Real Value
1	40h	Requestor	Requestor	Initiation of Communication; transmit request to the power supply; Address byte of power supply with hardware address 0x20 and LSB read/write low	
2	92h	Requestor	Requestor	Command to read power supply temperatures	
3	6Eh	Requestor	Requestor	Zero checksum generated from IPMB byte 2 (or all bytes after Address Byte up to the checksum byte)	
4	41h	Requestor	Requestor	Read response from the power supply; Address byte of power supply with hardware address 0x20 and LSB read/write high	
5	92h	Requestor	Power Supply	Response byte 1 Echo of the command from the reques	
6	01h	Requestor	Power Supply	Response byte 2	013Bh = 31.5°C
7	3Bh	Requestor	Power Supply	Response byte 3	
8	01h	Requestor	Power Supply	Response byte 4	0146h = 32.6°C
9	46h	Requestor	Power Supply	Response byte 5	
10	EBh	Requestor	Power Supply	Zero checksum of IPMB bytes 6-9	

Table 3 — *Communication example of command non-VITA 46.11 command 0x92*

Checksum bytes are 2's complement checksum of bytes in the request excluding the address byte or between the previous checksum and next checksum excluding the address byte.

8-bit checksum algorithm:

1. Initialize checksum to 0.
2. For each applicable byte, checksum = (checksum + byte) modulo 256.
3. Then checksum = – checksum.

Verification

When the checksum and the bytes are added together, modulo 256, the result should be 0.

Example of the checksum for the data returned by the power supply in Table 5.

$$\Leftrightarrow 256 - \left(\left(\sum_{x=5}^{9} IPMB\_Bytes\ x\right) mod\ 256\right) = EBh$$

$$\Leftrightarrow 256 - \left((92h + 01h + 3Bh + 01h + 46h)\ mod\ 256\right) = EBh$$

Verification:

$$\left(Ebh + (92h + 01h + 3Bh + 01h + 46h)\right) mod\ 256 = 0$$

Table 4 shows how to set and read the Status Register Byte.

Checksum bytes are 2's complement checksum of bytes in the request excluding the address byte or between the previous checksum and next checksum excluding the address byte.

IPMB Byte Number	Hex Byte	Clock Pulses Generated By	Data Pulses Generated By	Comment	Real Value
0	40h	Requestor	Requestor	Initiation of Communication; transmit request to the power supply; Address byte of power supply with hardware address 0x20 and LSB read/write low	
1	55h	Requestor	Requestor	Command to set the status register	
2	6Eh	Requestor	Requestor	Zero checksum generated from IPMB byte 2 (or all bytes after Address Byte up to the checksum byte)	
4	41h	Requestor	Requestor	Read response from the power supply; Address byte of power supply with hardware address 0x20 and LSB read/write high.	
5	92h	Requestor	Power Supply	Response byte 1 Echo of the command from the reques	
6	01h	Requestor	Power Supply	Response byte 2	013Bh = 31.5°C
7	3Bh	Requestor	Power Supply	Response byte 3	
8	01h	Requestor	Power Supply	Response byte 4	0146h = 32.6,C
9	46h	Requestor	Power Supply	Response byte 5	
10	EBh	Requestor	Power Supply	Zero checksum of IPMB bytes 6-9	

Table 4 — *Communication example of status register byte*

Commands Recognized by Power Supply

0x21: Sensor Data (Read Only) [d]			
Byte Number	**Contents**	**Format**	**Scaling**
0	0x21	Byte	Echo of the command
1	Status Reg	Byte	See below, same as used by command 0x55
2, 3	PCBA Temperature °C	INT16	16384 = 100°C
4, 5	+12V VSENSE	UINT16	16384 = 12.0V
6, 7	Not Used	UINT16	
8, 9	Not Used	UINT16	
10, 11	+3.3VAUX VSENSE	UINT16	16384 = 3.3V
12, 13	Not Used	UINT16	
14, 15	Not Used	UINT16	
16, 17	+12V IOUT (contact P6)	UINT16	16384 = 40A
18, 19	Not Used	UINT16	
20, 21	+12V IOUT (contact P3)	UINT16	16384 = 40A
22, 23	+3.3VAUX IOUT	UINT16	16384 = 15A
24, 25	Not Used	UINT16	
26, 27	Not Used	UINT16	
28, 29	Not Used	UINT16	
30, 31	Input Voltage	UINT16	16384 = 28V
32 – 51	Part Number	CHAR[20]	no 0 term, padded with 0x20
52 – 55	Serial Number	UINT32	Unsigned 32-bit integer; last 9 digits of the serial number of the unit on the label
56, 57	Factory Use Only	UINT16	N/A: factory use only
58, 59	Hardware Rev	CHAR[2]	
60, 61	Firmware Rev	CHAR[2]	
62	Input Current	UINT8	255 = 80A
63	Zero Checksum	Byte	Sum(Bytes 0:63) mod 256 = 0

[d] Most-significant bit of each byte is transmitted first.
Most-significant byte of UINT16 and UINT32 transmitted first.

Non-VITA 46.11 Recognized by Power Supply

0x44: Firmware Date (Read Only) [d]			
• 22 byte response in ASCII form.			
Byte Number	**Contents**	**Format**	**Typical Value/Comment**
0	0x44	Byte	Echo of the command
1 – 20	Date	ASCII[20]	'NOV 28 14:32:54 2018'
21	Zero Checksum	Byte	Sum(Bytes 0:21) mod 256 = 0

0x45: Hardware Address (Read Only) [d]			
Byte Number	**Contents**	**Format**	**Typical Value/Comment**
0	0x45	Byte	
1	I^2C Address	Byte	0x23, set by *GA1, *GA0
2	Zero Checksum	Byte	Sum(Bytes 0:2) mod 256 = 0

0x55: Status Command (Read/Write) [d]			
Byte Number	**Contents**	**Format**	**Typical Value/Comment**
0	0x55	Byte	
1	Status Byte	Byte	0x18 = All outputs ON
2	Zero Checksum	Byte	Sum(Bytes 0:2) mod 256 = 0

0x90: All Voltages in mV (Read Only) [d]			
Byte Number	**Contents**	**Format**	**Scaling/Comment**
0	0x90	Byte	Echo of the command
1, 2	+12V SENSE	UINT16	10mV/bit
3, 4	Not Used	UINT16	
5, 6	Not Used	UINT16	
7, 8	+3.3VAUX SENSE	UINT16	10mV/bit
9, 10	Not Used	UINT16	
11, 12	Not Used	UINT16	
13, 14	Input Voltage	UINT16	10mV/bit
15	Zero Checksum	Byte	Sum(Bytes 0:15) mod 256 = 0

Non-VITA 46.11 Recognized by Power Supply (Cont.)

0x99: Main Outputs – Output and Input Current in mA (Read Only) [d]			
Byte Number	**Contents**	**Format**	**Scaling/Comment**
0	0x99	Byte	Echo of the command
1, 2	+12V IOUT	UINT16	10mA/bit
3, 4	Not Used	UINT16	
5, 6	Not Used	UINT16	
7, 8	Input Current	UINT16	10mA/bit
9	Zero Checksum	Byte	Sum(Bytes 0:9) mod 256 = 0

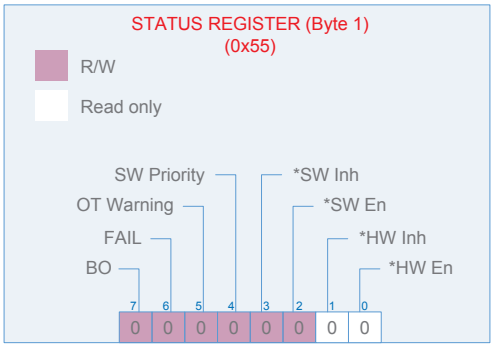
0x91: Auxiliary Outputs – Output Current in mA (Read Only) [d]			
Byte Number	**Contents**	**Format**	**Scaling/Comment**
0	0x91	Byte	Echo of the command
1, 2	+3.3VAUX IOUT	UINT16	1mA/bit
3, 4	Not Used	UINT16	
5, 6	Not Used	UINT16	
7	Zero Checksum	Byte	Sum(Bytes 0:7) mod 256 = 0

0x92: PCBA Card Edge Temperatures in °C x 10 (Read Only) [d]			
Byte Number	**Contents**	**Format**	**Scaling/Comment**
0	0x92	Byte	Echo of the command
1, 2	3U P0 connector, P1 side Rail	INT16	Temperature x 10, eg. –123 = –12.3°C
3, 4	3U P0 connector, P6 side Rail	INT16	Same as above
5	Zero Checksum	Byte	Sum(Bytes 0:5) mod 256 = 0

[d] Most-significant bit of each byte is transmitted first.
Most-significant byte of UINT16 and UINT32 transmitted first.

Status Register Bit Map used in command 0x55

Bit 0 and 1 allow you to monitor what the power supply is reading from the input connector.



Bit	Name	Condition	Default
7	BO	Battle override; see description	0
6	FAIL	If set to 1 by System Manager, a fault condition will clear this bit.	0
5	OT Warning	If set to 1 by System Manager, an OT fault will clear this bit.	0
4	SW Priority	Software Priority **1** = STATUS REGISTER overrides hardware inputs for INHIBIT* and ENABLE* **0** = Hardware is in control	0
3	*SW Inh	Software Inhibit **0** = Inhibit active (same as hardware input state)	0
2	*SW En	Software Enable **0** = Enable active (same as hardware input state)	0
1	*HW Inh	Status of ENABLE* pin (read only)	From backplane
0	*HW En	Status of INHIBIT* pin (read only)	From backplane

Under some conditions, it is desirable to ignore potentially damaging conditions. For this purpose the power supply provides a battle override function in the system status register. If bit 7 in the status register is set, then any non-recoverable events that would normally shut down the supply will not do so.

Event messages are still sent, but the power supply will continue to operate until the conditions cease to exist or it fails.

In order to enable battle override mode, the command message must include the exact same data byte three times in a row within the message where normally only a single byte would be needed.

IPMB Byte Number	Hex Byte	Clock Pulses Generated By	Data Pulses Generated By	Comment
1	40h	Requestor	Requestor	Address byte of power supply with hardware address 0x20 and LSB read/write low.
2	55h	Requestor	Requestor	Command byte. Request 1
3	80h	Requestor	Requestor	Only set BO.
4	2Bh	Requestor	Requestor	Zero checksum generated from IPMB bytes 2 – 3 and Stop Bit.
5	40h	Requestor	Requestor	Address byte of power supply with hardware address 0x20 and LSB read/write low.
6	55h	Requestor	Requestor	Command byte. Consecutive request 2
7	80h	Requestor	Requestor	Only set BO. Byte identical to IPMB byte 3.
8	2Bh	Requestor	Requestor	Zero checksum generated from IPMB Bytes 6 – 7 and Stop Bit.
9	40h	Requestor	Requestor	Address byte of power supply with hardware address 0x20 and LSB read/write low.
10	55h	Requestor	Requestor	Command byte. Consecutive request 3
11	29h	Requestor	Requestor	Only set BO. Byte identical to IPMB byte 3.
12	2Bh	Requestor	Requestor	Zero checksum generated from IPMB bytes 10 – 11. Battle override enabled after byte 12 is processed by the power supply IPMC.
13	40h	Requestor	Requestor	Address byte of power supply with hardware address 0x20 and LSB read/write high.
14	55h	Requestor	Requestor	Command byte.
15	ABh	Requestor	Requestor	Zero checksum generated from IPMB byte 14 and Stop Bit.
16	41h	Requestor	Requestor	Address byte of power supply with hardware address 0x20 and LSB read/write high.
17	55h	Requestor	Requestor	Echo Command byte.
18	82h	Requestor	Power Supply	Status register byte showing power supply is in battle override, enabled and not inhibited.
19	29h	Requestor	Requestor	Zero checksum generated from IPMB bytes 17 – 18 and Stop Bit.

Table 5 — *I^2C communication example for battle override*

IPMI Interface

The data interface is compliant with the requirements of VITA 46.11, VITA 62 -2016 and the IPMI v2.0 specifications. This section shows product specific information such as a sensor list and their coefficients.

Data Format

Four constants are used to calculate a real world value from the single byte variable returned in the response. The four constants are used in the equation Interpreting Received Values

$$y = \left(Mx + \left(B \bullet 10^{K1}\right)\right) \bullet 10^{K2}$$

Where:

y the converted reading

x the raw sensor reading

M the signed integer multiplier

B the signed additive offset

K1 signed exponent for constant B (sets decimal point for B)

K2 signed result exponent (sets decimal point for y)

Sensors and Constants

The list of sensors and coefficients can also be retrieved by the chassis manager by querying the "Sensor Data Record" (See VITA 46.11).

Sensor Number	Hex	Sensor Name	Type Code	Event / Reading Type	SI Units	M	B	K1	K2
2	**02h**	FRU Health	F2h	04h - Predictive Failure	Discrete				
3	**03h**	FRU Voltage	02h	05h - Limit Exceeded	Discrete				
4	**04h**	FRU Temperature	F3h	6Fh - Sensor Specific	Discrete				
7	**07h**	Input Voltage	02h	01h - Threshold	V	20	90	1	-2
8	**08h**	VS1, +12V Voltage	02h		V	54	0	0	-3
11	**0Bh**	AUX2, +3.3VAUX Voltage	02h		V	18	0	0	-3
14	**0Eh**	Input Current	03h		A	40	0	0	-2
15	**0Fh**	iS1, +12V Current through P6	03h		A	20	0	0	-2
16	**10h**	12V Total amps	03h		A	34	0	0	-2
17	**11h**	iS1, +12V Current through P3	03h		A	20	0	0	-2
18	**12h**	Card Edge Temperature towards P6	01h		K	1	20	1	0
19	**13h**	Card Edge Temperature towards P1	01h		K	1	20	1	0
21	**15h**	Input Power Consumption	0Bh		W	50	0	0	-1
22	**16h**	VS1, +12V Power Consumption	0Bh		W	32	0	0	-1
25	**19h**	iAUX2, +3.3VAUX Current	03h		A	1	0	0	-1
28	**1Ch**	AUX Power Consumption	0Bh		W	1	0	0	0
33	**21h**	Total Output Power	0Bh		W	40	0	0	-1

Table 6 — *Sensor list and coefficients*

Thresholds

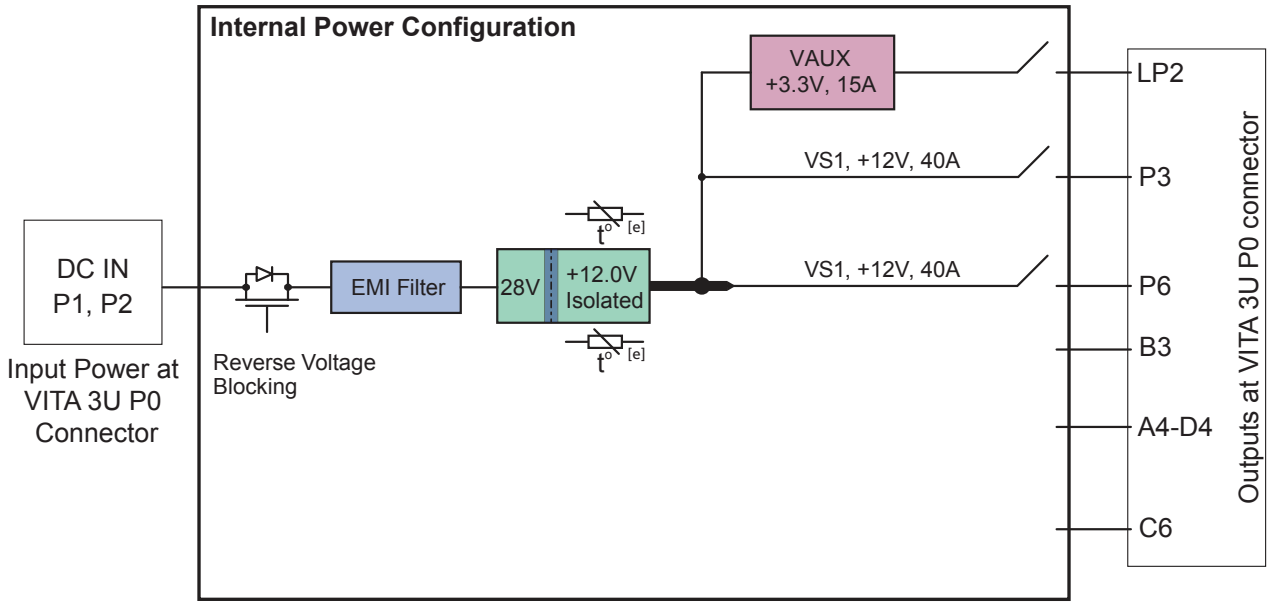
Upper and lower limits of the sensors are shown in Table 7.

Exceeding nonrecoverable limits of the power supply will cause the power supply to shut down all outputs except the 3.3V internal supply which powers the microcontroller and bus interface. The system will try to recover from all nonrecoverable faults after 1s shut down of all outputs.

Sensors		Critical Thresholds				Nonrecoverable Thresholds				Hysteresis
		Low		High		Low		High		
#	Name	Sensor Count	Actual Value	Sensor Count	Actual Value	Sensor Count	Actual Value	Sensor Count	Actual Value	Sensor Count
7	Input Voltage	185	46V	166	42.2V	5	10V	185	46V	5
8	VS1, +12V Voltage	213	11.502V	231	12.474V	208	11.232V	235	12.69V	5
11	AUX2, +3.3VAUX Voltage	181	3.258V	191	3.438V	180	3.24V	197	3.546V	5
14	Input Current			120	48A			180	72A	5
15	iS1, +12V Current through P6			180	36A			220	44A	20
16	12V Total Amps			128	43.52A			156	53.04A	20
17	iS1, +12V Current through P3			180	36A			220	44A	10
18	Card Edge Temp towards P6	38	238K	158	358K	32	232K	168	368K	10
19	Card Edge Temp towards P1	38	238K	158	358K	32	232K	168	368K	10
21	Input Power Consumption			150	750W			180	900W	10
22	VS1, +12V Power Consumption			140	448W			200	640W	6
25	+3.3VAUX Current			125	12.5A			185	18.5A	6
28	+3.3VAUX Power Consumption			50	50W			68	68W	6
33	Total Output Power			140	560W			158	632W	6

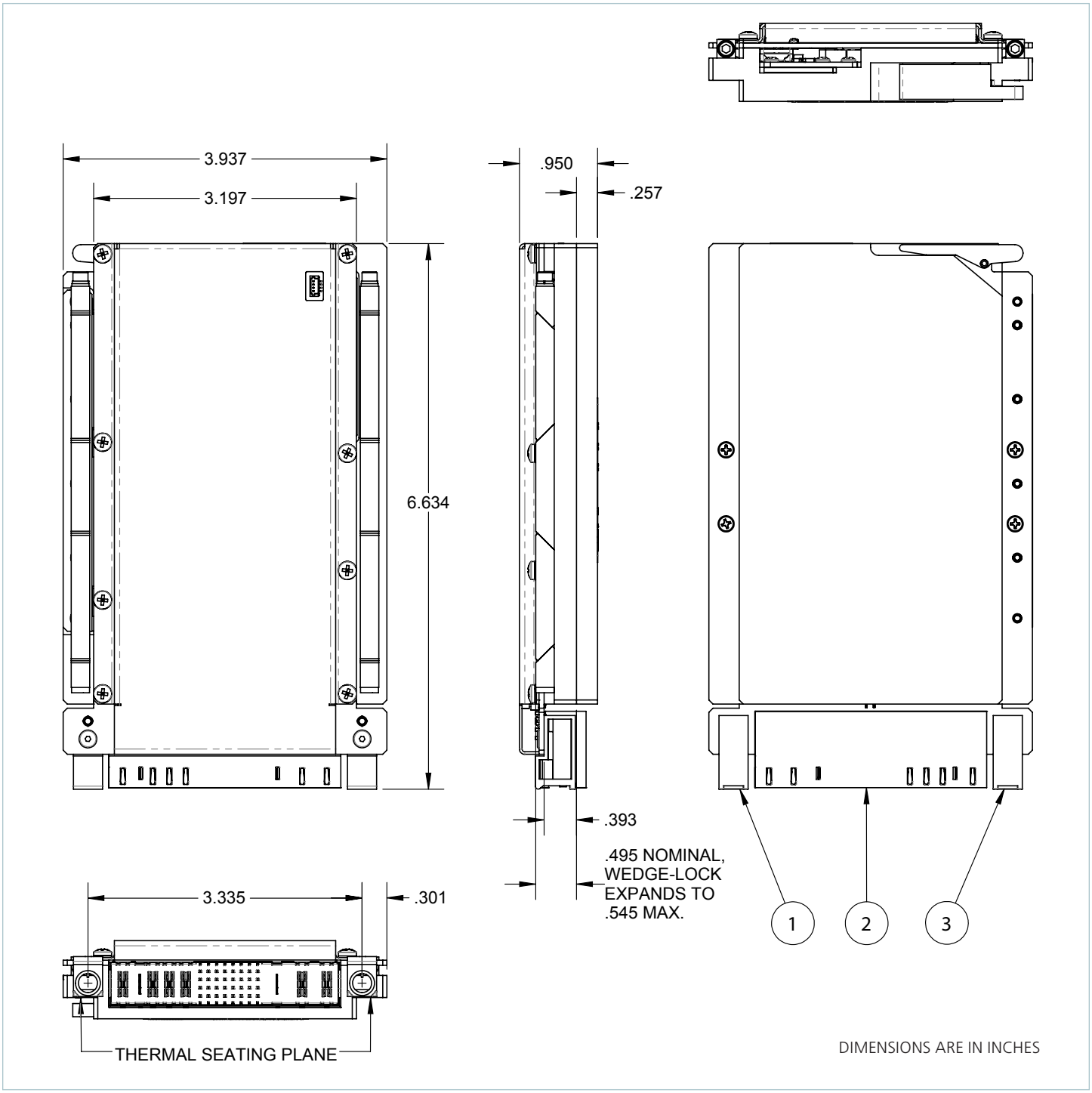
Table 7 — *Sensor thresholds*

Power Architecture



[e] Card edge temperature sensor proximity.

Mechanical Drawing



Connector Components			
Item #	**Description**	**Manufacturer**	**Manufacturer Part Number**
1	VITA46 315 DEG Guide Socket	TE Connectivity	1-2000713-4
2	VITA62 Connector Plug		6450849-7
3	VITA46 0 DEG Guide Socket		1-1469492-1

Revision History

Revision	Date	Description	Page Number(s)
1.0	08/12/25	Initial release	n/a

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