



SOSA™ Aligned Power Supply SOS028x3U600y00z

SOSA-Aligned DC-DC Converter

Features & Benefits

- Open VPX – VITA 62
- 18 – 45V input voltage range
- 600W output power
- 3U Open VPX power supply
- Conduction cooled
- I²C IPMI 46.11 monitoring and control
- Input voltage reverse-polarity protection
- Remote voltage sensing for +12V and +3.3V auxiliary
- Parallel operation capable with proprietary wireless current sharing
- Overcurrent, overvoltage and overtemperature protections
- IPC-A-610 class 3
- No aluminum electrolytic capacitors
- Enable, inhibit, system reset and power fail controls
- Meets military standard compliance: ^[a]
 - MIL-STD-704F
 - MIL-STD-461G
 - MIL-STD-810G
 - MIL-STD-1275E
 - RTCA/DO-160G

Typical Applications

- VPX power modules
- Avionics
- Shipborne electronics

Product Description

The Vicor SOSA-aligned power supply is a COTs power supply that is designed for 3U Open VPX systems that are developed to the SOSA standard. The module utilizes Vicor proprietary technology to enable high efficiency and power density for this highly rugged, conduction-cooled model.

Up to four power supplies can be paralleled to increase output power capability of +12V main and +3.3V auxiliary outputs with proprietary wireless current sharing. Need for conventional current-share pins are eliminated. Current share accuracy is $\pm 2A$.

^[a] See detailed specifications; contact Vicor Applications Engineering for report details.

Note: Product images may not highlight current product markings and cosmetic features.

Connector Pin Configuration

| ROWS | POWER | | | SIGNAL | | | | | | | | POWER | | | | | |
|------|-------|----|-----|--------|---|---|---|---|---|---|---|-------|----|----|----|-----|----|
| | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | | | | | | |
| D | P1 | P2 | LP1 | | | | | | | | | | P3 | P4 | P5 | LP2 | P6 |
| C | | | | | | | | | | | | | | | | | |
| B | | | | | | | | | | | | | | | | | |
| A | | | | | | | | | | | | | | | | | |

3U P0 Connector

Note: See mechanical drawing on page 30 for connector information.

Connector Pin Descriptions

| Pin | Function / Name | Description |
|----------------|------------------------------|---|
| P1 | -DC_IN | V _{IN-} |
| P2 | +DC_IN | V _{IN+} |
| LP1 | CHASSIS | Chassis |
| A1, B1, C1, D1 | No Connection | |
| A2 | No Connection | |
| B2 | FAIL* | When any of the output is not within specification, FAIL* signal will be driven low to indicate a failure |
| C2 | INHIBIT* | Input control signal as defined in VITA 62, referenced to SIGNAL_RETURN |
| D2 | ENABLE* | Input control signal as defined in VITA 62, referenced to SIGNAL_RETURN |
| A3, B3, C3, D3 | No Connection | |
| A4, B4, C4, D4 | No Connection | |
| A5 | *GA0 | Geographical address defined by VITA 46.11 |
| B5 | *GA1 | Geographical address defined by VITA 46.11 |
| C5 | SM0 (I ² C Clock) | Primary I ² C communication bus |
| D5 | SM1 (I ² C Data) | |
| A6 | I ² C Clock | Redundant I ² C communication bus |
| B6 | I ² C Data | |
| C6 | No Connection | |
| D6 | SYS_RESET* | System Reset is actively low. It will float when all outputs are within specification |
| A7, B7, C7 | No Connection | |
| D7 | SIGNAL_RETURN | Ground pin for control and communication signals; internally Kelvin-connected to POWER_RETURN. |
| A8 | +12V _{SENSE} | VS1 sense: shall be connected at point-of-load or on the backplane to corresponding voltage output |
| B8 | +3.3V _{SENSE} | VAUX sense: shall be connected at point-of-load or on the backplane to corresponding voltage output |
| C8 | No Connection | |
| D8 | SENSE_RETURN | Shall be connected to POWER_RETURN either remotely or at the connector |
| P3 | VS1 | +12V main output |
| P4, P5 | POWER_RETURN | Common output voltage return pin |
| LP2 | VAUX | +3.3V auxiliary output |
| P6 | VS1 | +12V main output |

Part Ordering Information

| Part Number | Product Grade | Conformal Coating | Factory-Configured Options |
|------------------|-----------------|----------------------------------|---|
| SOS028H3U600C000 | H = -40 to 85°C | C = Coated | 000 = Programmable, ^[b] SOSA standard keying ^[c] |
| SOS028H3U600D000 | | D = Coated + AU-plated Connector | |
| SOS028H3U600C001 | | C = Coated | 001 = Programmable, ^[b] VITA46 No-Key Guide Socket ^[c] |
| SOS028H3U600D001 | | D = Coated + AU-plated Connector | |

^[b] Programmable units can be set by the user to parallel ready or standalone operation only via I²C. Contact factory for options with no remote sense or different output voltages. See I²C user guide for information on changing the unit from Parallel operation to Standalone. By default, units are set to parallel from the factory.

^[c] Refer to connector components table, [page 25](#).

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

| Parameter | Comments | Min | Max | Unit |
|-------------------------------|--|------|-----|-----------------|
| Total Output Power | Combined outputs for all rails | | 600 | W |
| Operational Input Voltage | +IN to -IN, 100V 50ms operation MIL-STD-1275E surge only | -0.5 | 100 | V |
| Operating Temperature | Measured at card edge | -40 | 85 | °C |
| Storage Temperature | | -40 | 125 | |
| Isolation Voltage IN to OUT | | | 500 | V _{DC} |
| Isolation Voltage IN to CASE | | | 500 | V _{DC} |
| Isolation Voltage OUT to CASE | | | 100 | V _{DC} |

Electrical Characteristics

All data at nominal line and nominal load unless otherwise specified.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|------------------|--|-------|------|-------|-------------------|
| Overall System Characteristics | | | | | | |
| System Efficiency | | Nominal line, 25% aggregate loads | | 85 | | % |
| | | Nominal line, 50% aggregate loads | | 88 | | |
| | | Nominal line, 100% aggregate loads | | 90 | | |
| Power Input Characteristics | | | | | | |
| Operating Input Voltage Range | V_{IN} | | 18 | 28 | 45 | V |
| Input Current (No Load) | I_{IN-NL} | 28V Input, enable asserted, inhibit de-asserted | | 0.50 | 1.0 | A |
| Inrush Current | I_{INRUSH} | Peak no load, nominal line, high line; see Figure 5 | | 70 | 120 | A |
| Power On to +3.3V Auxiliary Output Delay | | If ENABLE* is tied to signal ground | 100 | 150 | 200 | ms |
| Input Undervoltage Lockout | | | | | 11.85 | V |
| Input Undervoltage Lockout Recovery | | | | | 17.8 | V |
| MIL-STD-1275E Operational Characteristics | | | | | | |
| Initial Engagement Surge (IES) Low Line Limit | | | | | 11.85 | V |
| Minimum Sustained IES Output Power Limit | | $12V < V_{IN} < 16V$ | | 320 | | W |
| Minimum Sustained IES Time Limit | | | 5 | | | s |
| Minimum Sustained Cranking Disturbance Time Limit | | $12V < V_{IN} < 16V$ | 30 | | | s |
| Maximum Sustained Cranking Disturbance Output Power | | | | 600 | | W |
| VS1: +12V Output | | | | | | |
| Output Voltage Set Point | V_{VS1} | | 11.85 | 12.1 | 12.15 | V |
| Output Regulation Over Line & Load | | Standalone mode | | 50 | | mV |
| | | Parallel mode | | 200 | 250 | |
| Output Voltage Ripple / Noise | | Nominal line from 6A load to full load | | 50 | 120 | mV _{p-p} |
| Rated Output Current | I_{R-VS1} | VS1 total | | | 48 | A |
| | $I_{R-VS1-P6}$ | Sourced through contact P6 | | | 40 | |
| | $I_{R-VS1-P3}$ | Sourced through contact P3 | | | 40 | |
| Maximum Operating Transmission Voltage Drop | V_{TD-VS1} | | | | 0.5 | V |
| Maximum Output Capacitance | C_{O-VS1} | | | | 9 | mF |
| Soft-Start Ramp Time | t_{SS-VS1} | All full load with max C_{O-VS1} | | 10 | | ms |
| Overcurrent Trip Threshold | $I_{OCP-VS1-P6}$ | Sourced through contact P6 | 42 | | | A |
| | $I_{OCP-VS1-P3}$ | Sourced through contact P3 | 42 | | | |
| VAUX: +3.3V Output | | | | | | |
| Output Voltage Set Point | V_{VAUX} | | 3.25 | 3.35 | 3.45 | V |
| Output Regulation Over Line & Load | | | | 100 | 150 | mV |
| Output Voltage Ripple / Noise | | Nominal line over load range, 20MHz BW; measured with 1 μ F and 10 μ F ceramic capacitor | | | 50 | mV _{p-p} |
| Rated Output Current | I_{R-VAUX} | | | | 15 | A |
| Maximum Output Capacitance | C_{O-VAUX} | | | | 5 | mF |
| Soft-Start Ramp Time | $t_{SS-VAUX}$ | All full load with max C_{O-VAUX} | | | 5 | ms |
| Overcurrent Trip Threshold | $I_{OCP-VAUX}$ | | 18 | | | A |

Signal Characteristics

All of the following plots are at nominal line and 600W aggregate load unless otherwise noted.

| ENABLE*: Enable* | | | | | | | | |
|---|-------|--|-------------------------|--------------------|------|------|------|------|
| <ul style="list-style-type: none"> The ENABLE* pin or control register bit enables and disables the +3.3V AUX output of the power supply. The ENABLE* pin has an internal pull-up to V_{CC} and is referenced to the Signal Return pin of the power supply. | | | | | | | | |
| Signal Type | State | Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
| Digital Input | Any | ENABLE* Enable Threshold | V _{ENABLE-EN} | | | | 0.8 | V |
| | | ENABLE* Disable Threshold | V _{ENABLE-DIS} | | 2.0 | | | V |
| | | Internally Generated V _{CC} | V _{CC} | | 3.21 | 3.30 | 3.39 | V |
| | | ENABLE* Internal Pull-Up Resistance to V _{CC} | R _{ENABLE-INT} | | 49 | 51 | 52 | kΩ |
| | | ENABLE* Enable Debounce Delay | t _{D-EN-E} | | 3 | 5 | | ms |
| | | ENABLE* Disable Debounce Delay | t _{D-EN-D} | | 3 | 5 | | ms |

| INHIBIT*: Inhibit* | | | | | | | | |
|---|-------|---|--------------------------|---|------|------|------|------|
| <ul style="list-style-type: none"> The INHIBIT* pin enables and disables all outputs except +3.3V_{AUX} if V_{ENABLE-EN} threshold has been met. The INHIBIT* pin has an internal pull up to V_{CC} and is referenced to the Signal Return pin of the power supply. | | | | | | | | |
| Signal Type | State | Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
| Digital Input | Any | INHIBIT* Enable Threshold | V _{INHIBIT-EN} | Status register bit 4 should be 0 (default) for digital input control line to have priority | 2.0 | | | V |
| | | INHIBIT* Disable Threshold | V _{INHIBIT-DIS} | | | | 0.8 | V |
| | | Internally Generated V _{CC} | V _{CC} | | 3.21 | 3.30 | 3.39 | V |
| | | INHIBIT* Internal Pull-Up Resistance to V _{CC} | R _{DISABLE-INT} | | 49 | 51 | 52 | kΩ |
| | | INHIBIT* Enable Debounce Delay after ENABLE* | t _{D-IN-E} | | 3 | 5 | | ms |
| | | INHIBIT* Disable Debounce Delay | t _{D-IN-D} | | 3 | 5 | | ms |
| | | Lockout Delay Between Consecutive INHIBIT* Enables | t _{D-IN-L} | | 3 | 5 | | ms |

Signal Characteristics (Cont.)

All of the following plots are at nominal line and 600W aggregate load unless otherwise noted.

| GA0*, GA1*: Geographical Address | | | | | | | | |
|---|----------|--|-----------------------|--------------------|------|------|------|------|
| <ul style="list-style-type: none"> The GA0* and GA1* pins sets the I²C address of the power supply. Geographical address is set at start up and cannot be changed without a power cycle. The GA0* and GA1* pins have an internal pull-up to V_{CC} and is referenced to the Signal Return pin of the power supply. | | | | | | | | |
| Signal Type | State | Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
| Digital Input | Start Up | Address Pins Low Threshold | V _{ADDR-L} | | | | 0.8 | V |
| | | Address Pins High Threshold | V _{ADDR-H} | | 2.0 | | | V |
| | | Internally Generated V _{CC} | V _{CC} | | 3.21 | 3.30 | 3.39 | V |
| | | ENABLE* Internal Pull-Up Resistance to V _{CC} | R _{ADDR-INT} | | 49 | 51 | 52 | kΩ |
| | | Address Pins Debounce Delay | t _{D-ADDR} | | 5 | | | ms |

| FAIL*, SYSRESET* & LED | | | | | | | | |
|--|------------------------------|-----------|---------------------|--|-----|-----|-----|------|
| <ul style="list-style-type: none"> The power supply has one two color LED located on the ejector edge of the power supply. The LED is either GREEN or RED depending on the state of operation. FAIL* and SYSRESET* lines are set with the LED. | | | | | | | | |
| Signal Type | State | Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
| Outputs | Steady RED | SYSRESET* | V _{SYSRST} | Start up: input voltage operating threshold V _{UV-IN} < V _{IN} < V _{OV-IN} has been met; if steady RED persists for >100ms, a critical system fault has been detected during start up | 0.0 | | 0.8 | V |
| | | FAIL* | V _{FAIL} | | 0.0 | | 0.8 | V |
| | Blinking GREEN | SYSRESET* | V _{SYSRST} | >100ms after V _{UV-IN} < V _{IN} < V _{OV-IN} has been met; power supply is ready for use | 2.0 | | 3.5 | V |
| | | FAIL* | V _{FAIL} | | 2.0 | | 3.5 | V |
| | Steady GREEN | SYSRESET* | V _{SYSRST} | All outputs are OK and ENABLE* is pulled low | 2.0 | | 3.5 | V |
| | | FAIL* | V _{FAIL} | | 2.0 | | 3.5 | V |
| | Blinking RED | SYSRESET* | V _{SYSRST} | Power supply has encountered a OT, OV, UV, OC or critical system failure during operating | 2.0 | | 3.5 | V |
| | | FAIL* | V _{FAIL} | | 0.0 | | 0.8 | V |
| | Fast Blinking GREEN | None | - | SW priority is set by 0x55 status command | - | - | - | - |
| | Blinking Alternate GREEN/RED | None | - | Battle Override mode is enabled successfully by 0x55 status command | - | - | - | - |

Application Characteristics

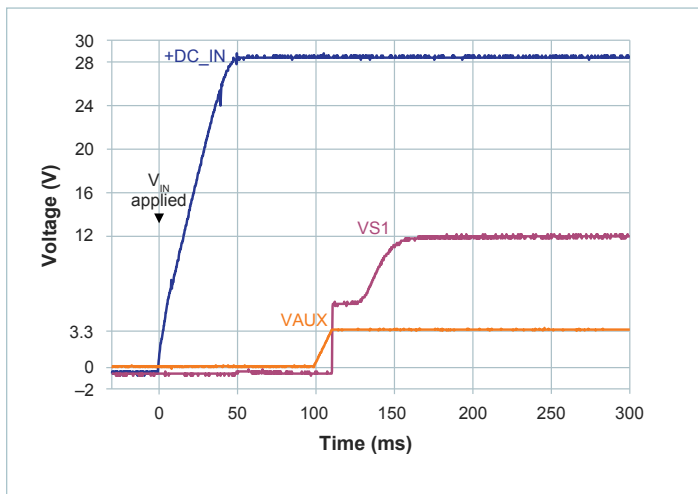


Figure 1 — Response time from V_{IN} applied to outputs available; under 200ms start; $V_{IN} = 28V$

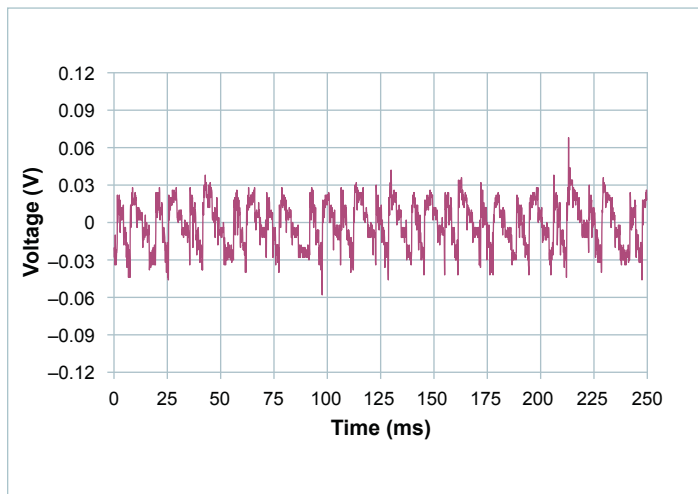


Figure 2 — VS1 (+12V) ripple at 10% load (4A), AC-coupled

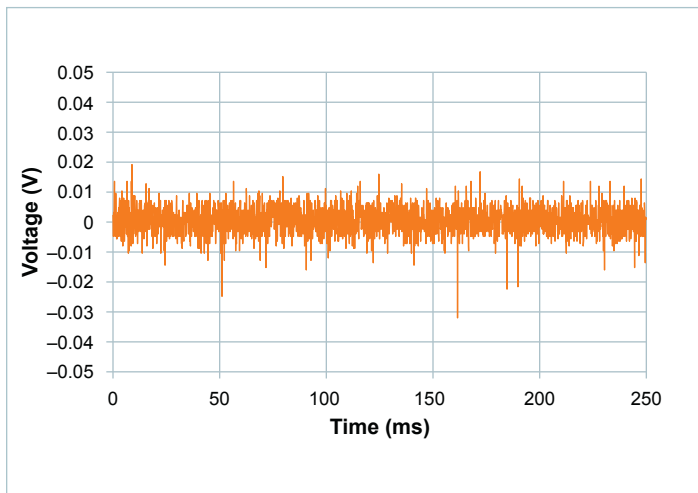


Figure 3 — AUX (+3.3V) ripple, AC-coupled

General Characteristics

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|-----------------------|--------------------------|---|-----|---------|-----|--------|
| Mechanical | | | | | | |
| Length | L | Per VITA62 | | 6.634 | | in |
| Width | W | Per VITA62 | | 3.937 | | in |
| Height | H | Per VITA62 | | 0.951 | | in |
| Weight | W | | | 630 | | g |
| Wedge-Lock Torque | | Manufacturer's recommended value | | 7 | | in-lbs |
| Thermal | | | | | | |
| Operating Temperature | T _{WEDGE-LOCKS} | | -40 | | 85 | °C |
| Assembly | | | | | | |
| Storage Temperature | | | -40 | | 125 | °C |
| Safety | | | | | | |
| MTBF | | MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer | | 614,742 | | Hrs |
| | | Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled | | 859,170 | | Hrs |

Signal Pin Functions

ENABLE* & INHIBIT*

Enable and Inhibit pins express active low logic. Table 1 has the truth table for the output state of the power supply. It is necessary to avoid the indeterminate output state where 0.8 – 2.0V is applied to the ENABLE* or INHIBIT* pins.

A digital debounce filter is present on the signals of both pins to prevent false transitions. The ENABLE* and INHIBIT* also have a minimum delay between successive output enable transitions to prevent repeated starts into high capacitance loads. See detailed specifications for delays time limits.

| ENABLE* Pin | INHIBIT* Pin | Output State and Notes |
|------------------------------------|-------------------------------------|--|
| < 0.8V, Logic 0 | > 2.0V or NO, Logic 1 | All outputs available |
| < 0.8V, Logic 0 | < 0.8V, Logic 0 | Only +3.3V _{AUX} output available |
| > 2.0V or NO, Logic 1 | Any | All outputs disabled |
| 0.8V > V _{ENABLE*} < 2.0V | 0.8V > V _{INHIBIT*} < 2.0V | Indeterminate state and must be avoided |

Table 1 — ENABLE & INHIBIT logic

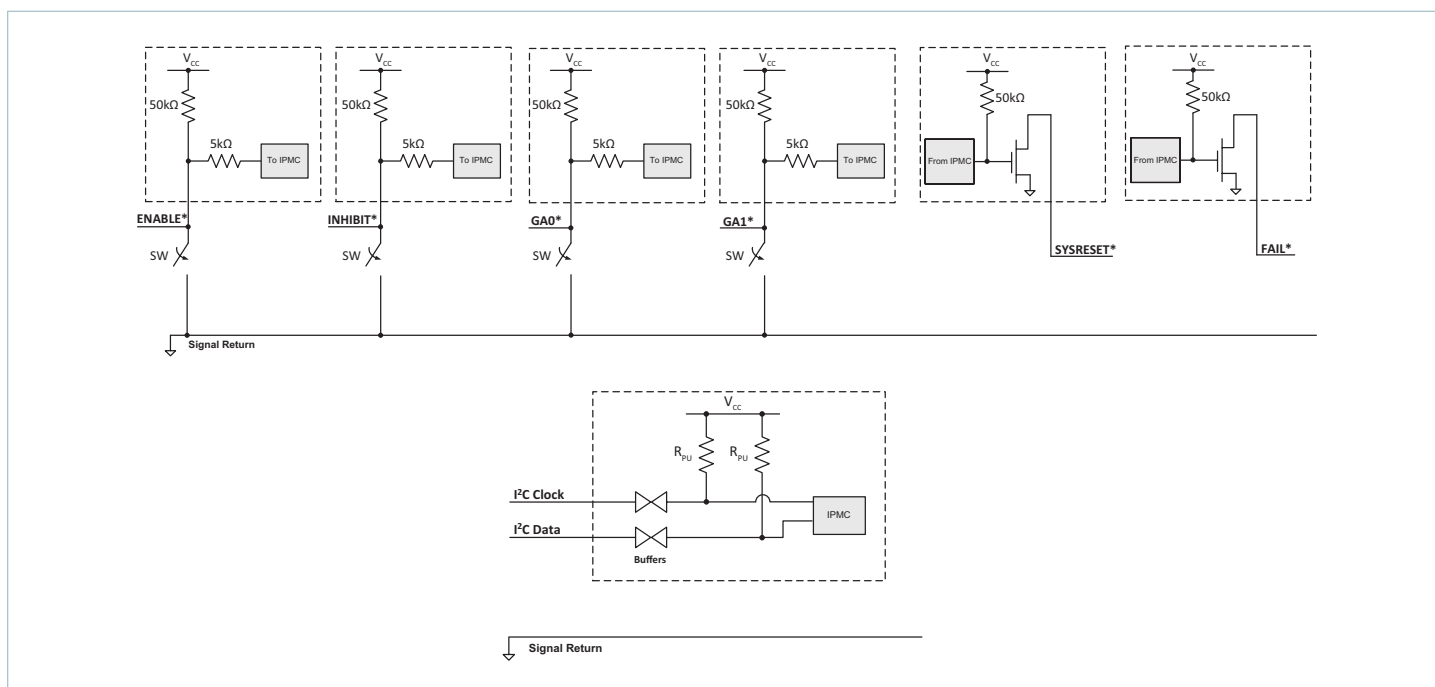
Geographical Address: GA0* & GA1*

Geographical address pins also exhibit active low logic. Table 2 has the truth table for the output state of the power supply. It is necessary to avoid the indeterminate state where 0.8 – 2.0V is applied to either address pins. A digital debounce filter is present on the signals of both pins to incorrect address assignment.

The geographical address is static and set on power up. The power supply's address cannot not change until power has been cycled and the states of the address pins have been modified before power up.

Typical External Circuits for Signal Pins

(ENABLE*, INHIBIT*, GA0*, GA1*, SYSRESET*, FAIL* and I²C Channels)



| GA1* | GA0* | Power Supply Address |
|---------------------------------|---------------------------------|---|
| > 2.0V or NO, Logic 1 | > 2.0V or NO, Logic 1 | 20h |
| > 2.0V or NO, Logic 1 | < 0.8V, Logic 0 | 21h |
| < 0.8V, Logic 0 | > 2.0V or NO, Logic 1 | 22h |
| < 0.8V, Logic 0 | < 0.8V, Logic 0 | 23h |
| 0.8V > V _{GA1*} < 2.0V | 0.8V > V _{GA0*} < 2.0V | Indeterminate state and must be avoided |

Table 2 — Geographical address assignment

I²C Ports:

Both primary and redundant I²C ports have the same address set by the Geographical Address pins and identical functionality. There is a bidirectional buffer on both clock and data lines with internal pull ups on the IPMC and external pulls on the back plane to +3.3V are required.

FAIL*

This signal line is open drain and tracks SYSRESET* when the unit is powering up or pulled down to SIGNAL_RETURN when any of the outputs are out of specification. A pull up resistor is expected on the backplane per section 4.6.3.7 of VITA 62.

SYSRESET*

This signal line is open drain and is pulled down to SIGNAL_RETURN when the unit is powering up. The line is released when the power supply is ready for control. Appropriate pull-up/pull-down resistors are expected on the back plane per VITA 46 section 7.3.9.

SIGNAL RETURN

SIGNAL RETURN is used as the reference for signals pin connections and is to be tied to POWER_RETURN on the backplane per section 4.6.3.10-1 of VITA 62.

Card Edge Temperature Sensors

The PCBA card edge temperature sensor internal to the power supply is mounted on the edge of the PCBA card edge. Consequently, the temperature sensor measures a temperature that is generally higher than the heat-sink-to-rail mounting interface and lower than the hot spot of the internal converters in the power supply.

Response from the power supply to I²C command 0x21 provides the temperature measured by the internal sensor that reads the higher temperature. This temperature can exceed 85°C. I²C command 0x92 will respond with both PCB mounted temperature sensors.

Power Limits

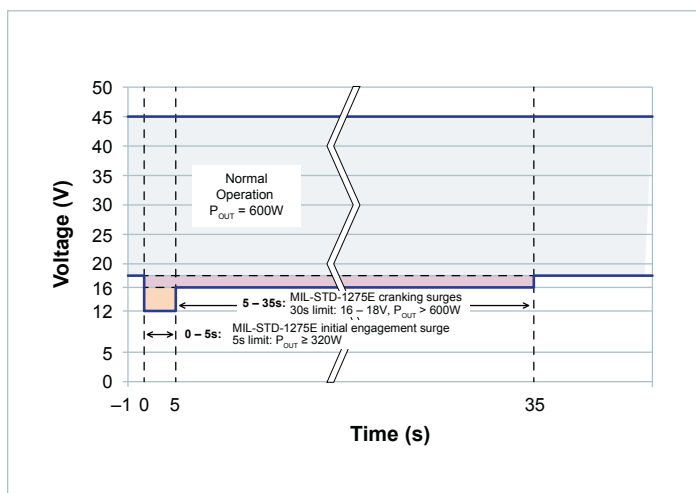


Figure 4 — Power-time limits during transient cranking disturbances

Per MIL-STD-1275E, the Initial Starter Engagement (ISE) can cause the nominal 28V bus to drop to 12V for 5s. During this time the available combined output power is required to be limited to 320W. Once the engine is cranking the voltage will be in the range of 16 – 18V and the full combined unit power of 600W is available for a maximum 30s.

Fault Operation

See Table 5 for nonrecoverable fault thresholds which trigger a fault and shut down/restart of the outputs of the supply.

Input Voltage Protection (IOVP)

If the input voltage to the power supply drops below V_{UV-IN} or exceeds V_{OV-IN} for at least 1ms, the power supply will shut down all outputs and digital communication lines until input voltage is within operating range V_{IN} . Triggering I_{OVP} has the same effect as power cycling the power supply. Supply currents and voltages are sampled every 200 μ s.

Output Voltage Protection (OVP)

The power supply measures voltage from the remote-sense lines as well as the voltages on the VITA connector which do not include remote sense drop.

The FAIL* line will be asserted (pulled low) when output voltage at the connector of the power supply is greater than the nonrecoverable limit of any output. OVP will also shut down the outputs until the output voltage of the converter is within specification. The power supply will automatically restart the outputs every 1s until the fault clears.

Overcurrent Protection (OCP)*

During an overcurrent fault on any output, all outputs will shut off and the FAIL* line will be asserted. The power supply will automatically try to restart outputs every 1s if the fault has cleared.

Overtemperature Protection (OTP)

The power supply will go into overtemperature protection and shut down all outputs when either internal temperature sensor measures 95°C. The power converter will recover for normal operation when the internal temperature has dropped by 20°C.

At 85°C the Bit-5 of the Status Register (0x55) will clear if the system manager sets Bit-5 to 1 which will indicate the power supply is within 10°C from shutting down.

Parallel Operation

For proper load regulation and paralleling of SOS028x3U600y00z power supplies, sense lines shall be connected to the load. An open or unconnected sense line will lead to a fault condition where all outputs remain off. A single kelvin connection between each sense pin and load is ideal on the backplane. Another method of connecting sense lines to the load is to bus sense lines between the power supplies and have a single backplane connection to the point-of-load. Under normal parallel power supply operation, each supply's PoL regulated output will be at different voltage with respect to its own backplane connector to compensate for transmission voltage drop. Figure 5a depicts an instance of a backplane with three power supplies where the point-of-load (PoL) sense pins on each power supply are connected.

It is not recommended to connect the PoL sense pins in a manner depicted in Figure 5b where each supply's PoL sense pins are connected to each other and also to each power supply's own PoL voltage output. In this case the system may appear to function normally temporarily but load regulation and sharing are not guaranteed.

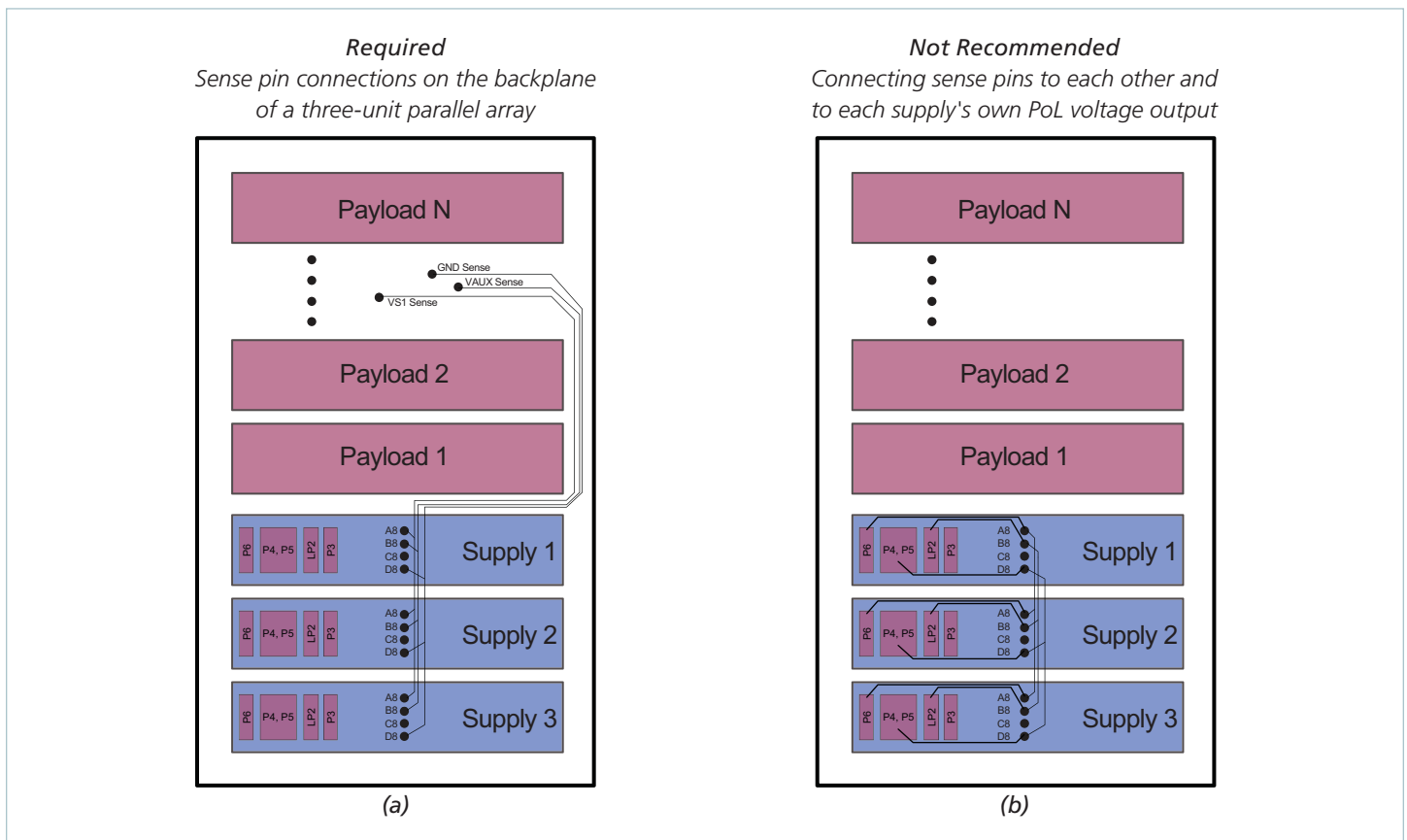


Figure 5 — Sense pin connection arrangement connects all supplies to the backplane of the array

All six outputs can be connected in parallel with the same output from other power supplies with the same part number. Only VS1, VS2 and VS3 support load sharing. The combined current output of paralleled AUX outputs is limited to the ampacity of respective individual AUX outputs of a single power supply.

Additional information on power supply paralleling can be found in [AN:801 – Parallel Operation](#).

| Output | Max Current vs. Paralleled Supplies | | | | Unit |
|--------------|-------------------------------------|----|-----|-----|------|
| | 1 | 2 | 3 | 4 | |
| VS1 (+12V) | 48 | 86 | 129 | 172 | A |
| VAUX (+3.3V) | 15 | 15 | 15 | 15 | A |

Table 3 — Maximum current rating by output for parallel arrays

Standalone Operation

Switching the power supply from paralleling to standalone can be done on a single-use basis or permanently by the user using I²C.

Each unit ships from the factory capable of paralleling multiple identical power supplies. If the power supply is used in standalone mode without additional identical supplies connected in parallel, the output voltages of the power supply that are shareable, namely, VS1 and VAUX, will not droop with increased current load and will regulate the output voltage close to the no-load voltage. The standalone mode of operation may be desirable in applications where output voltage tolerance requirements exceed the limits allowed by VITA 62 and only one power supply is required.

In order to set the power supply to standalone mode the byte sequence shown in Table 4 needs to be transmitted to the power supply.

| IPMB Byte Number | Hex Byte | Comment |
|------------------|----------|---|
| 0 | 40h | Initiation of Communication; transmit request to the power supply. Address byte of power supply with hardware address 0x20 and LSB read/write low. |
| 1 | 66h | Command byte 1 |
| 2 | 99h | Command byte 2 |
| 3 | 10h | Command byte 3 |
| 5 | F1h | Zero checksum of IPMB bytes 1-3 and Stop Bit |

Table 4 — Byte sequence to set the power supply in standalone

To verify if the power supply is in standalone mode, VS1 remote-load sense voltage can be measured between connector pin A8 and sense return D8. The voltage between A8 and D8 will drop less than 40mV between no-load and full-load. If the power supply is in paralleling mode, VS1 remote-load sense voltage measured between connector pin A8 and sense return D8 will vary over 100mV between no-load and full-load.

To set the power supply to share mode again, command byte 3 in Table 4 needs to change to 00h. The checksum for bytes 1 – 3 will need to be recalculated and transmitted to the power supply. The sequence will need to be transmitted to the power supply a total of 3 times for the power supply to permanently change its mode at power up to support current share or paralleling.

To permanently change the power supply to either standalone or paralleling mode, the sequence in Table 4 with byte 3 set correctly needs to be transmitted three times consecutively. Committing the change permanently will cause the power supply to adopt the desired mode of operation from power up. If the power supply mode of operation is changed permanently, the power supply will perform a soft reboot once to store settings in its internal memory. The power supply can be switched from paralleling to standalone and vice-versa permanently up to 100,000 times due to memory wear limitations. Switching mode of operation without committing changes permanently can be done as many times as the user requires. If the mode of operation is switched without committing the change permanently, the power supply will revert to the mode of operation set permanently after a power cycle.

Conducted Emissions Testing

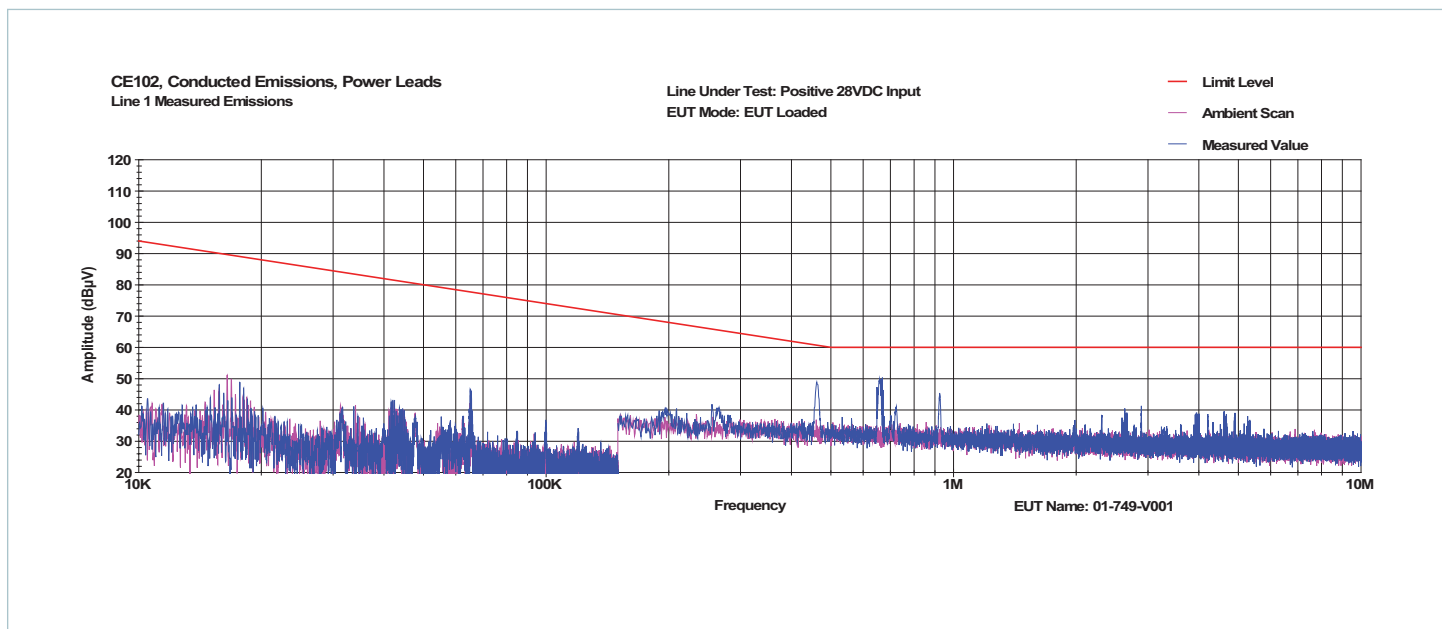


Figure 6 — Conducted emissions of +28V input line at full load

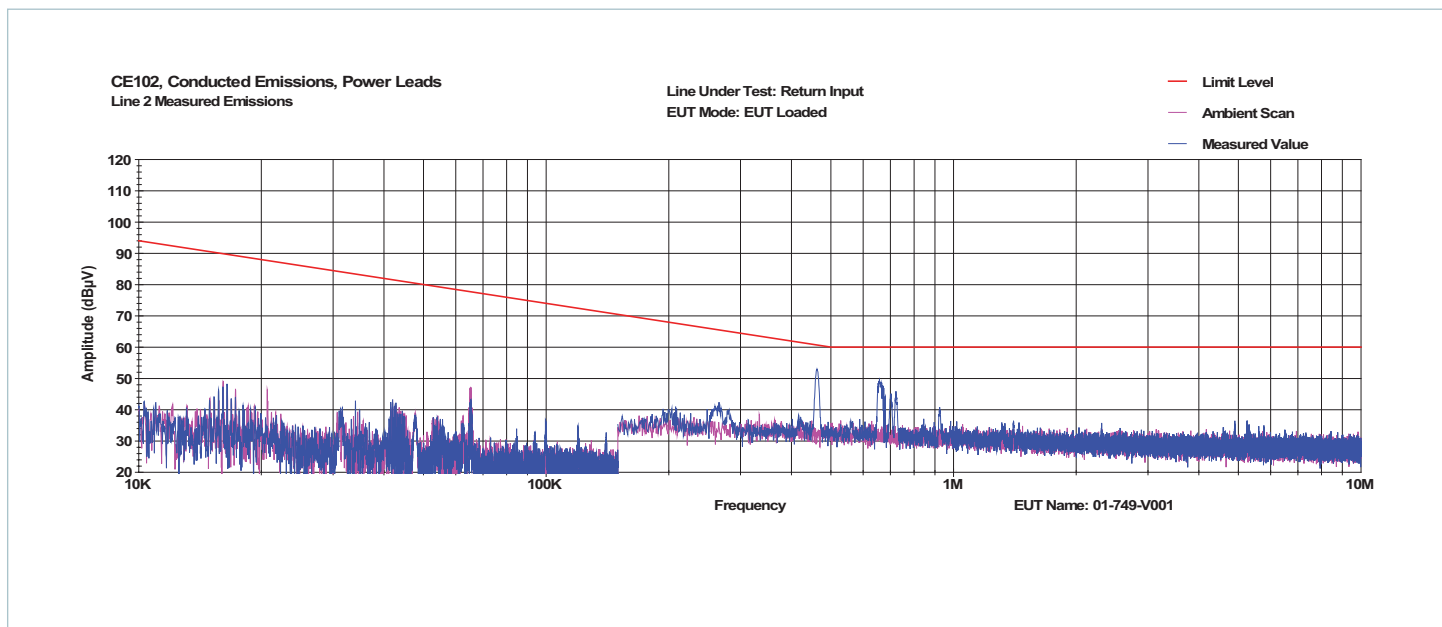


Figure 7 — Conducted emissions of +28V return line at full load

Conducted Emissions Testing (Cont.)

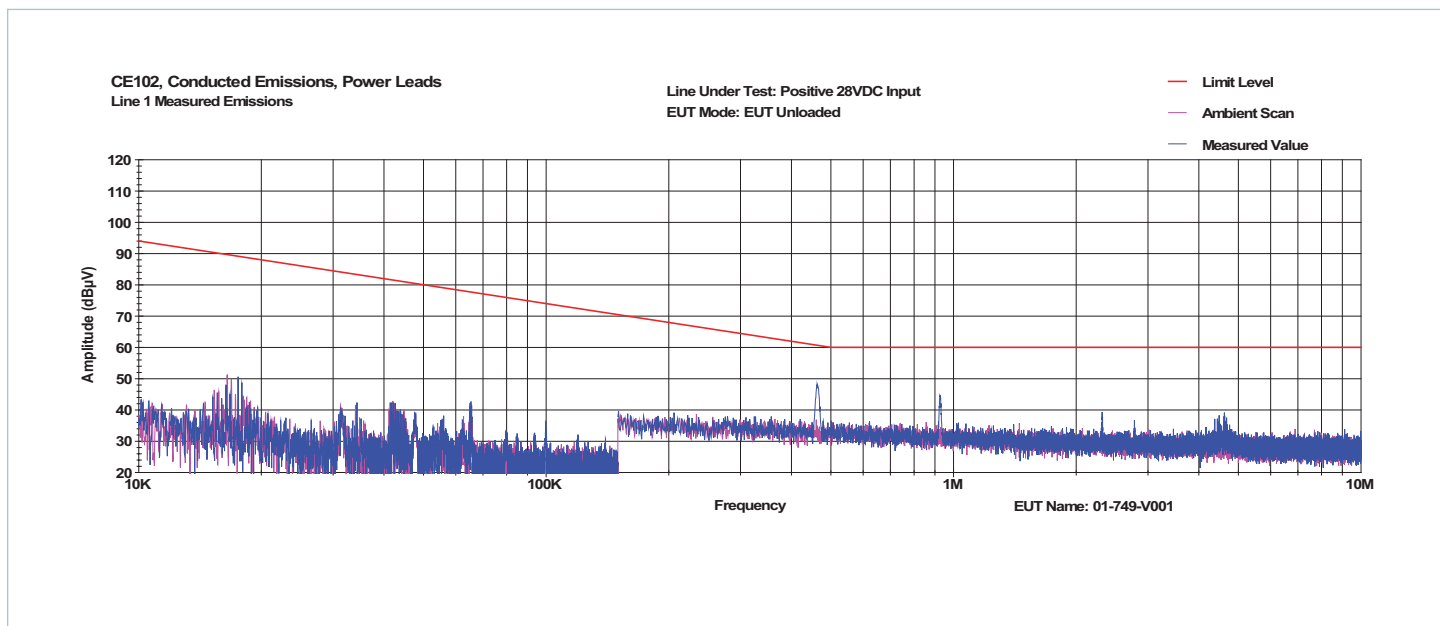


Figure 8 — Conducted emissions of +28V input line at no load

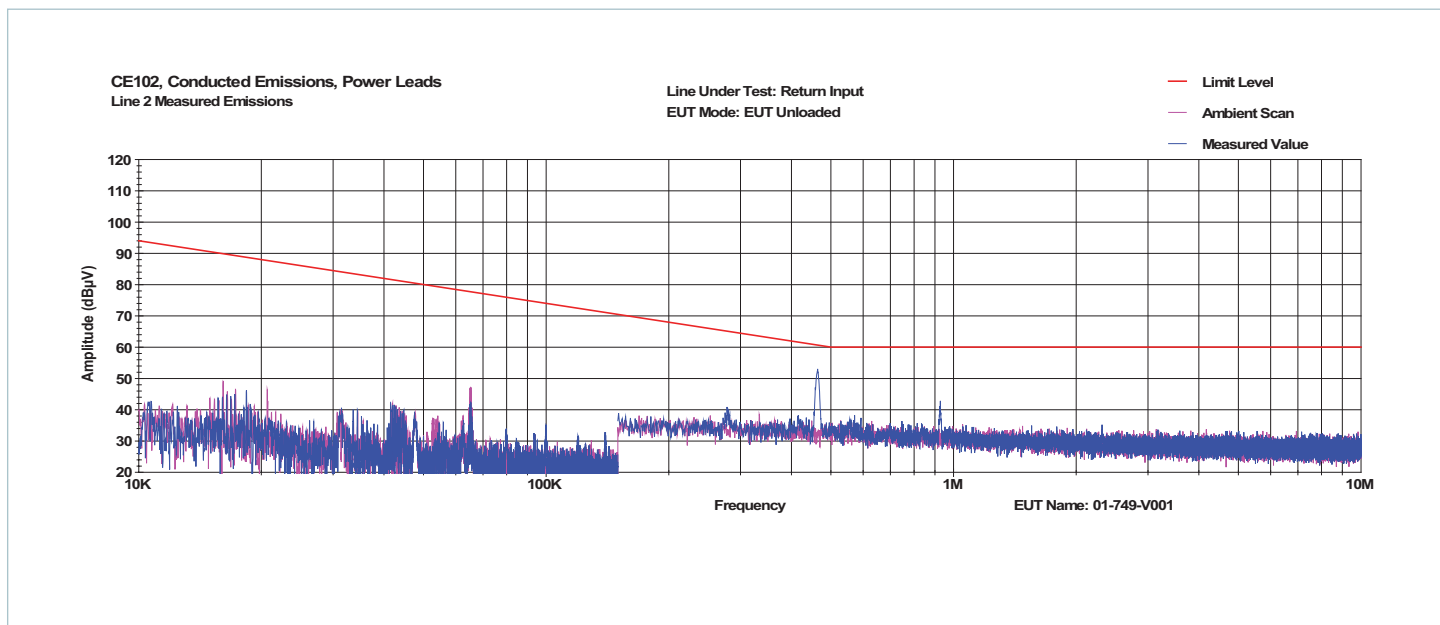


Figure 9 — Conducted emissions of +28V return line at no load

Standards Compliance

| MIL-STD-461F | | |
|---|--|--------|
| CS06 | ±200V, 10µs | Passed |
| | ±400V, 5µs | Passed |
| | 1000 – 2000Hz PSD decreasing at 6dB/octave | Passed |
| CS115 | Bulk input power cables | Passed |
| | Bulk output power cables | Passed |
| CS116 | Bulk input power cables | Passed |
| | Bulk output power cables | Passed |
| MIL-STD-461G | | |
| CE102 | Basic curve | Passed |
| CS101 | Figure CS101-1, Cuve #2 | Passed |
| CS114 Curve 5 | Input power lead | Passed |
| | Bulk input power cables | Passed |
| MIL-STD-704F | | |
| LDC103 – Voltage Distortion Spectrum | | Passed |
| LDC105 – Normal Voltage Transients | | Passed |
| LDC302 – Abnormal Voltage Transients | | Passed |
| MIL-STD-810G | | |
| Vibration, Method 514.5 Procedure I | 1 – 100Hz PSD increasing at 3dB/octave | Passed |
| | 100 – 1000Hz PSD = 0.1g ² /Hz | Passed |
| | 1000 – 2000Hz PSD decreasing at 6dB/octave | Passed |
| Operating Shock, Method 516 Procedure I | 40g, 11ms shock half-sine | Passed |
| | 40g, 11ms, terminal saw-tooth shock pulses in all three axes | Passed |
| MIL-STD-1275E | | |
| All Sections | 12V initial engagement surge limited to 510W output power | Passed |
| RTCA/DO-160G | | |
| Section 15: ESD | | Passed |
| Section 17: Voltage Spike, Category A | | Passed |
| IEC 61000-4-2 | | |
| ESD, Level 4 | ±15kV Air Discharge | Passed |
| VITA 47 | | |
| Humidity | Method 507 per VITA 47 Section 4.6 | Passed |
| Operating Temperature | VITA 47 Section 4.1.2 class CC4 | Passed |
| Temperature Cycling | MIL-STD-202 Method 107 per VITA 47 Section 4.3 | Passed |
| Altitude | 1,500ft below sea level to 70,000ft above sea level | Passed |
| Fungus Resistance | MIL-STD-810G, Method 508 per VITA47 Section 4.10 | Passed |
| Corrosion Resistance | ASTM G85, Annex A4, cycle A4.4.4.1 per VITA 47 Section 4.12 | Passed |

I²C Sensor Commands

Commands are sent by SMBus-compatible packets over the I²C physical interface. The I²C bus will communicate at 100kHz. Pull-up resistors to +3.3V are expected on the system backplane.

Two pins, labeled *GA1 and *GA0 are provided at each power supply slot, where *GA1 and *GA0 are defined to be active (SET) when low. The power supply will respond to I²C address 010 00[GA1][GA0].

The power supply supports commands to read sensor data from the power supply without utilizing VITA 46.11 or IPMI. The commands are similar to register reads in from I²C memory and function in a parent/child configuration. Unlike VITA 46.11 which is a multi-parent protocol, commands defined in this section are parent-write and parent-read.

Table 5 shows the following transmission pattern for reading power supply rail temperatures with command 0x92 using the parent-write/parent-read transmission format. In all non-VITA 46.11 commands, the parent requests the data from the child, which is the power supply.

| IPMB Byte Number | Hex Byte | Clock Pulses Generated By | Data Pulses Generated By | Comment | Real Value |
|------------------|----------|---------------------------|--------------------------|---|----------------|
| 1 | 40h | Requestor | Requestor | Initiation of Communication; transmit request to the power supply; Address byte of power supply with hardware address 0x20 and LSB read/write low | |
| 2 | 92h | Requestor | Requestor | Command to read power supply temperatures | |
| 3 | 6Eh | Requestor | Requestor | Zero checksum generated from IPMB byte 2 (or all bytes after Address Byte up to the checksum byte) | |
| 4 | 41h | Requestor | Requestor | Read response from the power supply; Address byte of power supply with hardware address 0x20 and LSB read/write high | |
| 5 | 92h | Requestor | Power Supply | Response byte 1 Echo of the command from the requestor | |
| 6 | 01h | Requestor | Power Supply | Response byte 2 | 013Bh = 31.5°C |
| 7 | 3Bh | Requestor | Power Supply | Response byte 3 | |
| 8 | 01h | Requestor | Power Supply | Response byte 4 | 0146h = 32.6°C |
| 9 | 46h | Requestor | Power Supply | Response byte 5 | |
| 10 | EBh | Requestor | Power Supply | Zero checksum of IPMB bytes 6-9 | |

Table 5 — Communication example of command non-VITA 46.11 command 0x92

Checksum bytes are 2's complement checksum of bytes in the request excluding the address byte or between the previous checksum and next checksum excluding the address byte.

8-bit checksum algorithm:

1. Initialize checksum to 0.
2. For each applicable byte, checksum = (checksum + byte) modulo 256.
3. Then checksum = - checksum.

Verification

When the checksum and the bytes are added together, modulo 256, the result should be 0.

Example of the checksum for the data returned by the power supply in Table 5.

$$\Leftrightarrow 256 - \left(\sum_{x=5}^9 \text{IPMB_Bytes } x \right) \bmod 256 = \text{EBh}$$

$$\Leftrightarrow 256 - \left((92h + 01h + 3Bh + 01h + 46h) \bmod 256 \right) = \text{EBh}$$

Verification:

$$\left(\text{EBh} + (92h + 01h + 3Bh + 01h + 46h) \right) \bmod 256 = 0$$

Table 6 shows how to set and read the Status Register Byte.

Checksum bytes are 2's complement checksum of bytes in the request excluding the address byte or between the previous checksum and next checksum excluding the address byte.

| IPMB Byte Number | Hex Byte | Clock Pulses Generated By | Data Pulses Generated By | Comment | Real Value |
|------------------|----------|---------------------------|--------------------------|---|----------------|
| 0 | 40h | Requestor | Requestor | Initiation of Communication; transmit request to the power supply; Address byte of power supply with hardware address 0x20 and LSB read/write low | |
| 1 | 55h | Requestor | Requestor | Command to set the status register | |
| 2 | 6Eh | Requestor | Requestor | Zero checksum generated from IPMB byte 2 (or all bytes after Address Byte up to the checksum byte) | |
| 4 | 41h | Requestor | Requestor | Read response from the power supply; Address byte of power supply with hardware address 0x20 and LSB read/write high. | |
| 5 | 92h | Requestor | Power Supply | Response byte 1 Echo of the command from the requestor | |
| 6 | 01h | Requestor | Power Supply | Response byte 2 | 013Bh = 31.5°C |
| 7 | 3Bh | Requestor | Power Supply | Response byte 3 | |
| 8 | 01h | Requestor | Power Supply | Response byte 4 | 0146h = 32.6°C |
| 9 | 46h | Requestor | Power Supply | Response byte 5 | |
| 10 | EBh | Requestor | Power Supply | Zero checksum of IPMB bytes 6-9 | |

Table 6 — Communication example of status register byte

Commands Recognized by Power Supply

| 0x21: Sensor Data (Read Only) ^[d] | | | |
|--|------------------------|----------|--|
| Byte Number | Contents | Format | Scaling |
| 0 | 0x21 | Byte | Echo of the command |
| 1 | Status Reg | Byte | See below, same as used by command 0x55 |
| 2, 3 | PCBA Temperature °C | UINT16 | 16384 = 100°C |
| 4, 5 | +12V VSENSE | UINT16 | 16384 = 12.0V |
| 6, 7 | Not Used | UINT16 | |
| 8, 9 | Not Used | UINT16 | |
| 10, 11 | +3.3VAUX VSENSE | UINT16 | 16384 = 3.3V |
| 12, 13 | Not Used | UINT16 | |
| 14, 15 | Not Used | UINT16 | |
| 16, 17 | +12V IOUT (contact P6) | UINT16 | 16384 = 40A |
| 18, 19 | Not Used | UINT16 | |
| 20, 21 | +12V IOUT (contact P3) | UINT16 | 16384 = 40A |
| 22, 23 | +3.3VAUX IOUT | UINT16 | 16384 = 15A |
| 24, 25 | Not Used | UINT16 | |
| 26, 27 | Not Used | UINT16 | |
| 28, 29 | Not Used | UINT16 | |
| 30, 31 | Input Voltage | UINT16 | 16384 = 28V |
| 32 – 51 | Part Number | CHAR[20] | no 0 term, padded with 0x20 |
| 52 – 55 | Serial Number | UINT32 | Unsigned 32-bit integer; last 9 digits of the serial number of the unit on the label |
| 56, 57 | Factory Use Only | UINT16 | N/A: factory use only |
| 58, 59 | Hardware Rev | CHAR[2] | |
| 60, 61 | Firmware Rev | CHAR[2] | |
| 62 | Input Current | UINT8 | 255 = 80A |
| 63 | Zero Checksum | Byte | Sum(Bytes 0:63) mod 256 = 0 |

^[d] Most-significant bit of each byte is transmitted first.
Most-significant byte of UINT16 and UINT32 transmitted first.

Non-VITA 46.11 Recognized by Power Supply

| 0x44: Firmware Date (Read Only) ^[d] | | | |
|---|--------------------------|-----------|-----------------------------|
| • 22 byte response in ASCII form. | | | |
| Byte Number | Contents | Format | Typical Value/Comment |
| 0 | 0x44 | Byte | Echo of the command |
| 1 – 20 | Date | ASCII[20] | 'NOV 28 14:32:54 2018' |
| 21 | Zero Checksum | Byte | Sum(Bytes 0:21) mod 256 = 0 |
| 0x45: Hardware Address (Read Only) ^[d] | | | |
| Byte Number | Contents | Format | Typical Value/Comment |
| 0 | 0x45 | Byte | |
| 1 | I ² C Address | Byte | 0x23, set by *GA1, *GA0 |
| 2 | Zero Checksum | Byte | Sum(Bytes 0:2) mod 256 = 0 |
| 0x55: Status Command (Read/Write) ^[d] | | | |
| Byte Number | Contents | Format | Typical Value/Comment |
| 0 | 0x55 | Byte | |
| 1 | Status Byte | Byte | 0x18 = All outputs ON |
| 2 | Zero Checksum | Byte | Sum(Bytes 0:2) mod 256 = 0 |
| 0x90: All Voltages in mV (Read Only) ^[d] | | | |
| Byte Number | Contents | Format | Scaling/Comment |
| 0 | 0x90 | Byte | Echo of the command |
| 1, 2 | +12V SENSE | UINT16 | 10mV/bit |
| 3, 4 | Not Used | UINT16 | |
| 5, 6 | Not Used | UINT16 | |
| 7, 8 | +3.3VAUX SENSE | UINT16 | 10mV/bit |
| 9, 10 | Not Used | UINT16 | |
| 11, 12 | Not Used | UINT16 | |
| 13, 14 | Input Voltage | UINT16 | 10mV/bit |
| 15 | Zero Checksum | Byte | Sum(Bytes 0:15) mod 256 = 0 |

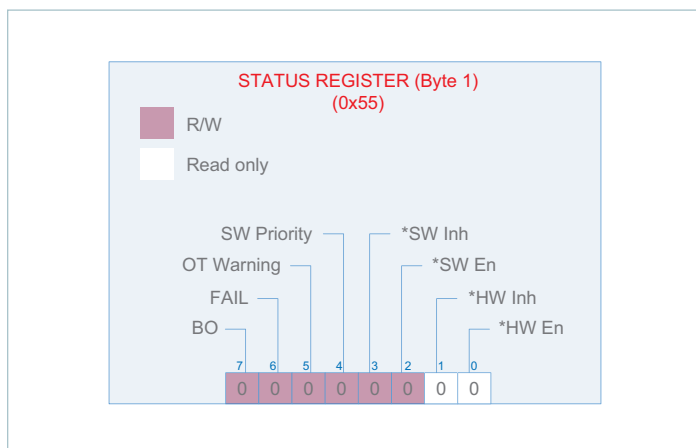
Non-VITA 46.11 Recognized by Power Supply (Cont.)

| 0x99: Main Outputs – Output and Input Current in mA (Read Only) ^[d] | | | |
|--|----------------------------------|--------|---|
| Byte Number | Contents | Format | Scaling/Comment |
| 0 | 0x99 | Byte | Echo of the command |
| 1, 2 | +12V IOUT | UINT16 | 10mA/bit |
| 3, 4 | Not Used | UINT16 | |
| 5, 6 | Not Used | UINT16 | |
| 7, 8 | Input Current | UINT16 | 10mA/bit |
| 9 | Zero Checksum | Byte | Sum(Bytes 0:9) mod 256 = 0 |
| 0x91: Auxiliary Outputs – Output Current in mA (Read Only) ^[d] | | | |
| Byte Number | Contents | Format | Scaling/Comment |
| 0 | 0x91 | Byte | Echo of the command |
| 1, 2 | +3.3VAUX IOUT | UINT16 | 1mA/bit |
| 3, 4 | Not Used | UINT16 | |
| 5, 6 | Not Used | UINT16 | |
| 7 | Zero Checksum | Byte | Sum(Bytes 0:7) mod 256 = 0 |
| 0x92: PCBA Card Edge Temperatures in °C x 10 (Read Only) ^[d] | | | |
| Byte Number | Contents | Format | Scaling/Comment |
| 0 | 0x92 | Byte | Echo of the command |
| 1, 2 | 3U P0 connector, P1 side Rail | INT16 | Temperature x 10, eg. -123 = -12.3°C |
| 3, 4 | 3U P0 connector, P6 side Rail | INT16 | Same as above |
| 5 | Zero Checksum | Byte | Sum(Bytes 0:5) mod 256 = 0 |

^[d] Most-significant bit of each byte is transmitted first.
Most-significant byte of UINT16 and UINT32 transmitted first.

Status Register Bit Map used in command 0x55

Bit 0 and 1 allow you to monitor what the power supply is reading from the input connector.



Under some conditions, it is desirable to ignore potentially damaging conditions. For this purpose the power supply provides a battle override function in the system status register. If bit 7 in the status register is set, then any non-recoverable events that would normally shut down the supply will not do so.

Event messages are still sent, but the power supply will continue to operate until the conditions cease to exist or it fails.

In order to enable battle override mode, the command message must include the exact same data byte three times in a row within the message where normally only a single byte would be needed.

| Bit | Name | Condition | Default |
|-----|-------------|--|----------------|
| 7 | BO | Battle override; see description | 0 |
| 6 | FAIL | If set to 1 by System Manager, a fault condition will clear this bit. | 0 |
| 5 | OT Warning | If set to 1 by System Manager, an OT fault will clear this bit. | 0 |
| 4 | SW Priority | Software Priority 1 = STATUS REGISTER overrides hardware inputs for INHIBIT* and ENABLE* 0 = Hardware is in control | 0 |
| 3 | *SW Inh | Software Inhibit 0 = Inhibit active (same as hardware input state) | 0 |
| 2 | *SW En | Software Enable 0 = Enable active (same as hardware input state) | 0 |
| 1 | *HW Inh | Status of ENABLE* pin (read only) | From backplane |
| 0 | *HW En | Status of INHIBIT* pin (read only) | From backplane |

| IPMB Byte Number | Hex Byte | Clock Pulses Generated By | Data Pulses Generated By | Comment |
|------------------|----------|---------------------------|--------------------------|--|
| 1 | 40h | Requestor | Requestor | Address byte of power supply with hardware address 0x20 and LSB read/write low. |
| 2 | 55h | Requestor | Requestor | Command byte. Request 1 |
| 3 | 80h | Requestor | Requestor | Only set BO. |
| 4 | 2Bh | Requestor | Requestor | Zero checksum generated from IPMB bytes 2 – 3 and Stop Bit. |
| 5 | 40h | Requestor | Requestor | Address byte of power supply with hardware address 0x20 and LSB read/write low. |
| 6 | 55h | Requestor | Requestor | Command byte. Consecutive request 2 |
| 7 | 80h | Requestor | Requestor | Only set BO. Byte identical to IPMB byte 3. |
| 8 | 2Bh | Requestor | Requestor | Zero checksum generated from IPMB Bytes 6 – 7 and Stop Bit. |
| 9 | 40h | Requestor | Requestor | Address byte of power supply with hardware address 0x20 and LSB read/write low. |
| 10 | 55h | Requestor | Requestor | Command byte. Consecutive request 3 |
| 11 | 29h | Requestor | Requestor | Only set BO. Byte identical to IPMB byte 3. |
| 12 | 2Bh | Requestor | Requestor | Zero checksum generated from IPMB bytes 10 – 11. Battle override enabled after byte 12 is processed by the power supply IPMC. |
| 13 | 40h | Requestor | Requestor | Address byte of power supply with hardware address 0x20 and LSB read/write high. |
| 14 | 55h | Requestor | Requestor | Command byte. |
| 15 | ABh | Requestor | Requestor | Zero checksum generated from IPMB byte 14 and Stop Bit. |
| 16 | 41h | Requestor | Requestor | Address byte of power supply with hardware address 0x20 and LSB read/write high. |
| 17 | 55h | Requestor | Requestor | Echo Command byte. |
| 18 | 82h | Requestor | Power Supply | Status register byte showing power supply is in battle override, enabled and not inhibited. |
| 19 | 29h | Requestor | Requestor | Zero checksum generated from IPMB bytes 17 – 18 and Stop Bit. |

Table 7 — I²C communication example for battle override

IPMI Interface

The data interface is compliant with the requirements of VITA 46.11, VITA 62 -2016 and the IPMI v2.0 specifications. This section shows product specific information such as a sensor list and their coefficients.

Data Format

Four constants are used to calculate a real world value from the single byte variable returned in the response. The four constants are used in the equation Interpreting Received Values

$$y = (Mx + (B \cdot 10^{K1})) \cdot 10^{K2}$$

Where:

- y** the converted reading
- x** the raw sensor reading
- M** the signed integer multiplier
- B** the signed additive offset
- K1** signed exponent for constant B (sets decimal point for B)
- K2** signed result exponent (sets decimal point for y)

Sensors and Constants

The list of sensors and coefficients can also be retrieved by the chassis manager by querying the "Sensor Data Record" (See VITA 46.11).

| Sensor Number | Hex | Sensor Name | Type Code | Description | SI Units | M | B | K1 | K2 |
|---------------|-----|------------------------------------|-----------|--------------------------|----------|----|----|----|----|
| 2 | 02h | FRU Health | F2h | 04h - Predictive Failure | Discrete | | | | |
| 3 | 03h | FRU Voltage | 02h | 05h - Limit Exceeded | Discrete | | | | |
| 4 | 04h | FRU Temperature | F3h | 6Fh - Sensor Specific | Discrete | | | | |
| 7 | 07h | Input Voltage | 02h | 01h - Threshold | V | 20 | 90 | 1 | -2 |
| 8 | 08h | VS1, +12V Voltage | 02h | | V | 20 | 90 | 2 | -3 |
| 11 | 0Bh | AUX, +3.3VAUX Voltage | 02h | | V | 10 | 20 | 2 | -3 |
| 14 | 0Eh | Input Current | 03h | | A | 40 | 0 | 0 | -2 |
| 15 | 0Fh | iS1, +12V Current, P6 | 03h | | A | 32 | 0 | 0 | -2 |
| 17 | 0Fh | iS1, +12V Current, P3 | 03h | | A | 32 | 0 | 0 | -2 |
| 18 | 12h | Card Edge Temp towards P6 | 01h | | K | 1 | 20 | 1 | 0 |
| 19 | 13h | Card Edge Temp towards P1 | 01h | | K | 1 | 20 | 1 | 0 |
| 21 | 15h | Input Power Consumption | 0Bh | | W | 50 | 0 | 0 | -1 |
| 22 | 16h | VS1, +12V Power Consumption | 0Bh | | W | 32 | 0 | 0 | -1 |
| 25 | 19h | iAUX, +3.3VAUX Current | 03h | | A | 10 | 0 | 0 | -2 |
| 28 | 1Ch | AUX Power Consumption | 0Bh | | W | 1 | 0 | 0 | 0 |
| 33 | 21h | Output Power Consumption | 0Bh | | W | 40 | 0 | 0 | -1 |
| 34 | 23h | iS1, +12V Current, Total (P1 + P6) | 02h | | A | 40 | 0 | 0 | -2 |

Table 8 — Sensor list and coefficients

Thresholds

Upper and lower limits of the sensors are shown in Table 5. Exceeding the nonrecoverable or critical limits will trigger a system event message and set the appropriate bits in the warning sensor registers (Sensors 2, 3 and 4). They reflect a degradation of the power supply towards its operational limits but are still within operating norms.

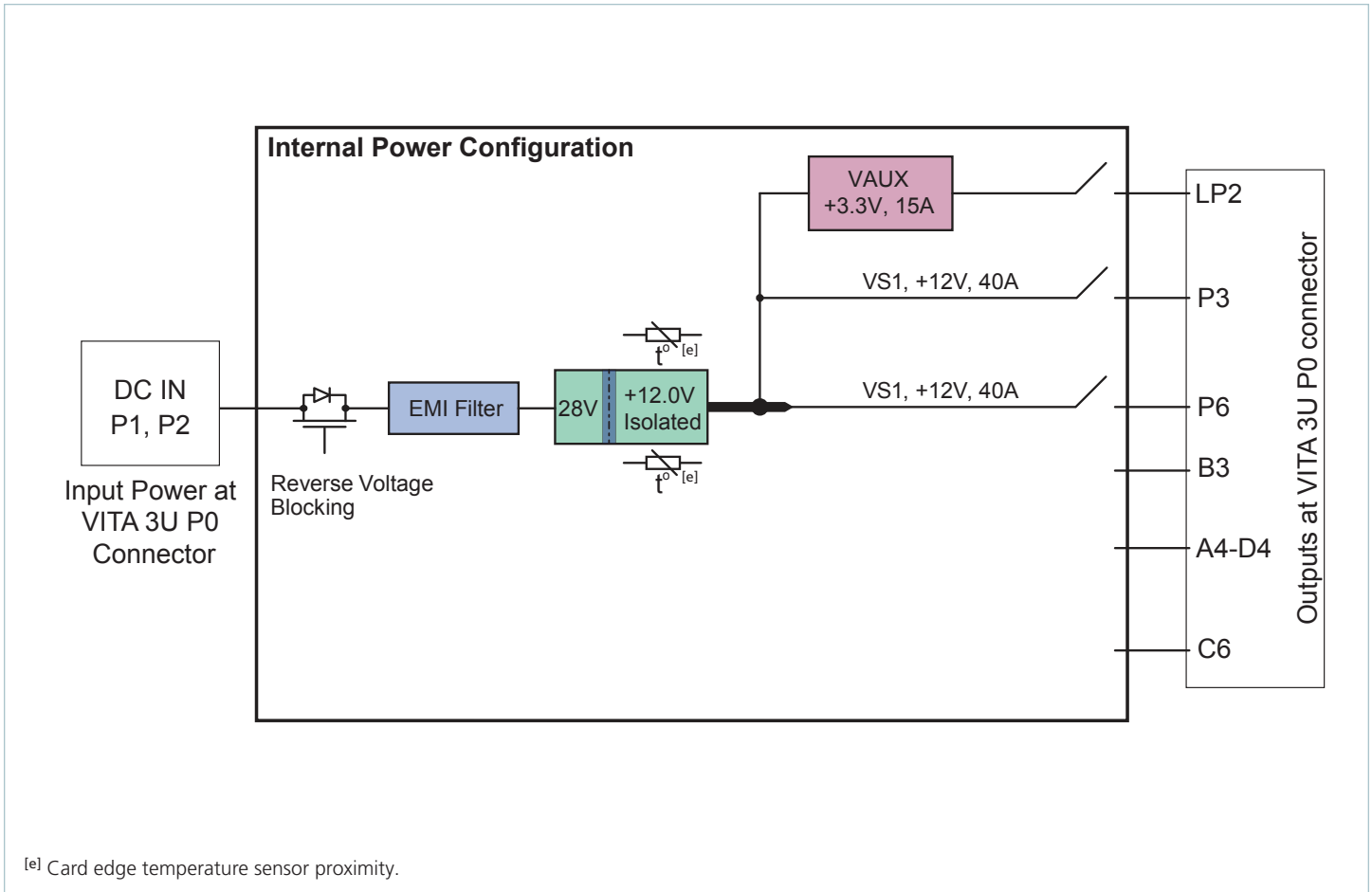
Exceeding nonrecoverable limits of the power supply will cause the power supply to shut down all outputs except the 3.3V internal supply which powers the microcontroller and bus interface. The system will try to recover from all nonrecoverable faults after 1s shut down of all outputs.

The high non-recoverable threshold of the input voltage is set to 255h (60V) since the unit is capable of operating through MIL-STD-1275E surges. The surge protection circuit inside the power supply will limit the input voltage to be inside the units allowable range during a surge. If a surge exceeding the maximum allowable limits persists, the unit will shut down for at least 25s and attempt auto-recovery.

| Sensors | | Critical Thresholds | | | | Nonrecoverable Thresholds | | | | Hysteresis |
|---------|------------------------------------|---------------------|--------------|--------------|--------------|---------------------------|--------------|--------------|--------------|--------------|
| | | LOW | | High | | LOW | | High | | |
| # | Name | Sensor Count | Actual Value | Sensor Count | Actual Value | Sensor Count | Actual Value | Sensor Count | Actual Value | Sensor Count |
| 7 | Input Voltage | 40 | 17V | 166 | 42.2V | 14 | 11.8V | 255 | 60V | 10 |
| 8 | VS1, +12V Voltage | 126 | 11.52V | 174 | 12.48V | 114 | 11.28V | 187 | 12.74V | 15 |
| 11 | AUX, +3.3VAUX Voltage | 120 | 3.2V | 144 | 3.44V | 100 | 3V | 155 | 3.55V | 15 |
| 14 | Input Current | | | 160 | 48A | | | 180 | 54A | 10 |
| 15 | iS1, +12V Current, P6 | | | 110 | 34A | | | 140 | 42A | 20 |
| 17 | iS1, +12V Current, P3 | | | 110 | 34A | | | 140 | 42A | 20 |
| 18 | Card Edge Temp towards P6 | 38 | 238K | 158 | 358K | 32 | 232K | 168 | 368K | 15 |
| 19 | Card Edge Temp towards P1 | 38 | 238K | 158 | 358K | 32 | 232K | 168 | 368K | 15 |
| 21 | Input Power Consumption | | | 190 | 950W | | | 215 | 1075W | 13 |
| 22 | VS1, +12V Power Consumption | | | 215 | 688W | | | 248 | 793.6W | 13 |
| 25 | iAUX2, +3.3VAUX Current | | | 125 | 12.5A | | | 170 | 17A | 30 |
| 28 | AUX Power Consumption | | | 50 | 50W | | | 60 | 60W | 7 |
| 33 | AUX Power Consumption | | | 165 | 660W | | | 210 | 840W | 7 |
| 34 | iS1, +12V Current, Total (P1 + P6) | | | 181 | 43.5A | | | 225 | 52A | 20 |

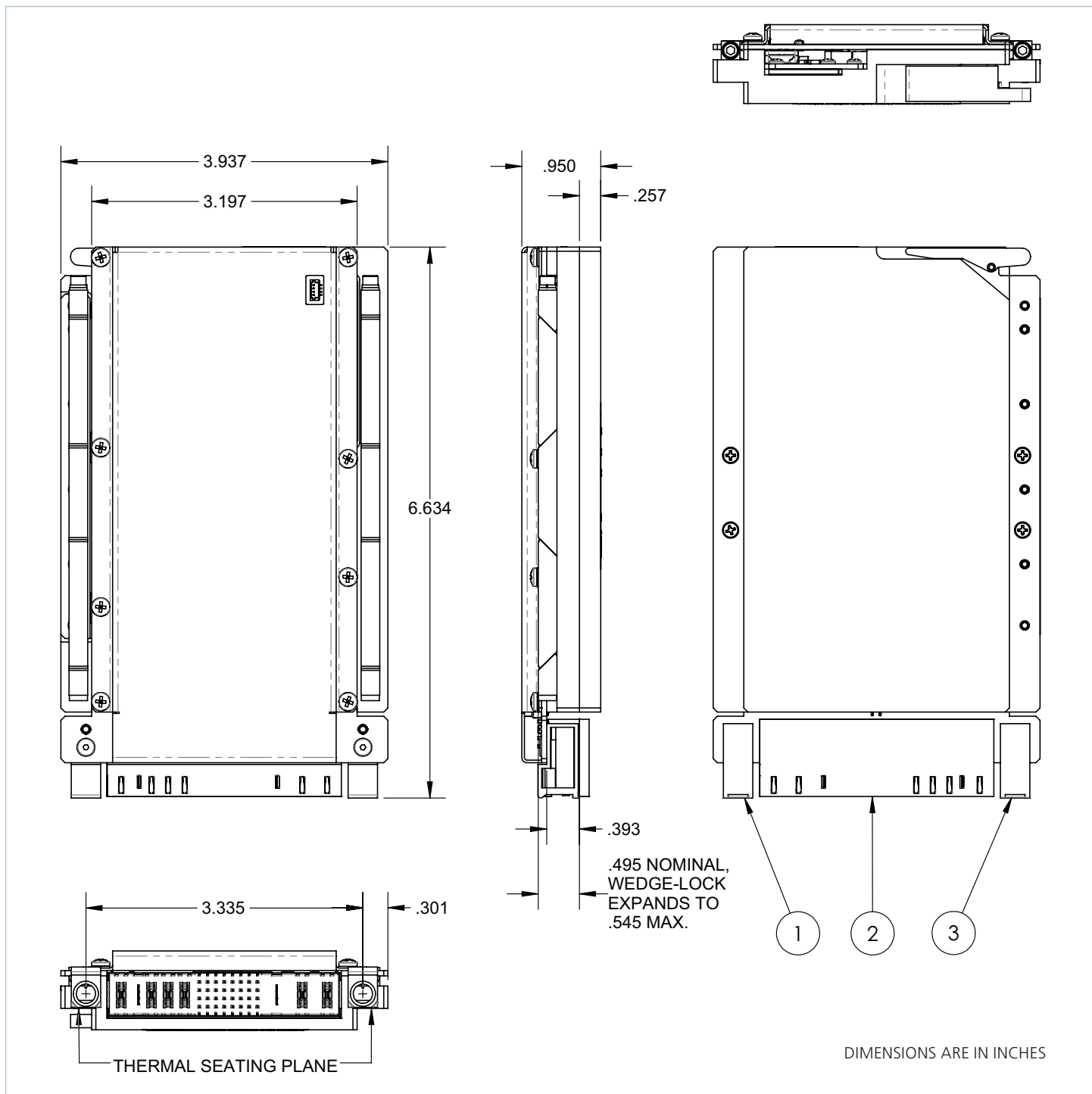
Table 9 — Sensor thresholds

Power Architecture



^[e] Card edge temperature sensor proximity.

Mechanical Drawing



Connector Components

| Item # | Vicor Factory-Configured Option | Description | Manufacturer | Manufacturer Part Number |
|--------|---------------------------------|---------------------------------|-----------------|--------------------------|
| 1 | 000 | VITA46 135 DEG Guide Socket | TE Connectivity | 1-2000713-4 |
| | 001 | VITA46 No-Key Guide Socket | | 1-1469492-9 |
| 2 | C000, C001 | VITA62 Connector Plug | | 6450849-7 |
| | D000, D001 | VITA62 Au-Plated Connector Plug | | 2314578-2 |
| 3 | 000, 001 | VITA46 0 DEG Guide Socket | | 1-1469492-1 |

Revision History

| Revision | Date | Description | Page Number(s) |
|----------|----------|-----------------|----------------|
| 1.0 | 09/15/23 | Initial release | n/a |

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