30V_{IN} to 65V_{IN} Cool-Power ZVS Buck Regulator

Product Description

The PI3527-65 is a high input voltage, wide input range DC-DC ZVS Buck regulator integrating controller, power switches, and support components all within a high density System-in-Package (SiP).

The integration of a high-performance Zero-Voltage Switching (ZVS) topology, within the PI3527-65, increases point of load performance providing best in class power efficiency. The PI3527-65 requires only an external inductor, two voltage selection resistors and minimal capacitors to form a complete DC-DC switch mode buck regulator.

Device	Output Voltage		I_{OUT} Max
	Set	Range	
PI3527-65-LGIZ	12V	6.5V to 15V	18A

Features & Benefits

- High Efficiency HV ZVS Buck Topology
- Wide input voltage range of 30V to 65V
- Wide output range
- Parallel capable with single wire current sharing
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- Differential amplifier for output remote sensing
- User adjustable soft-start & tracking
- -40°C to 120°C operating range (T_{INT})

Applications

- HV to PoL Buck Regulator Applications
- Computing, Communications, Industrial, Automotive Equipment

Package Information

- 10mm x 14mm x 2.6mm LGA SiP

Contents

Order Information

Product	Nominal Output	Rated I_{OUT}	Package	Transport Media
PI3527-65-LGIZ	12V	18A	10mm x 14mm LGA	TRAY

Thermal, Storage and Handling Information

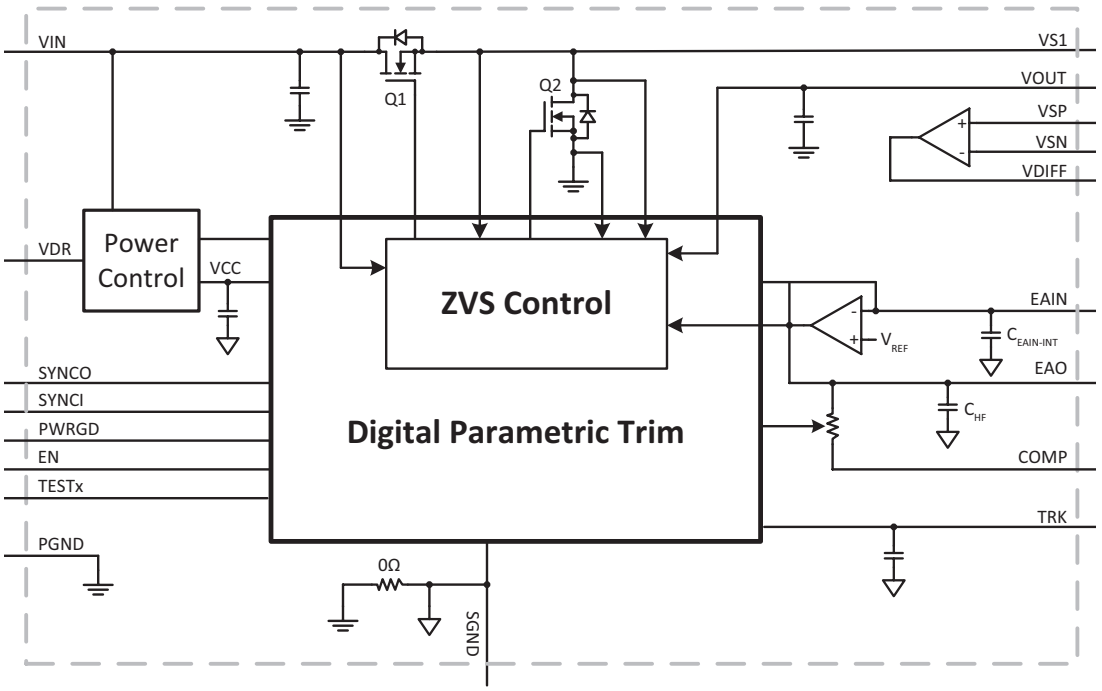
Name	Rating
Storage Temperature	-65°C to 150°C
Internal Operating Temperature	-40°C to 120°C
Soldering Temperature for 20 seconds	245°C
MSL Rating	3
ESD Rating, JESD22-A114F, JESD22-C101F	2kV HBM; 1kV CDM, respectively

Absolute Maximum Ratings

Name	Rating
V_{IN}	-0.7V_{DC} to 75V
VS1	-0.7V_{DC} to 75V
V_{OUT}	-0.5V_{DC} to 25V
SGND	±100mA
TRK	-0.3V to 5.5V, ±30mA
VDR, SYNCI, SYNCO, PWRGD, EN, COMP, EAO, EAIN, VDIFF, VSN, VSP, TESTx	-0.3V to 5.5V, ±5mA

Notes: Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltages are referenced to PGND unless otherwise noted.

Functional Block Diagram



Simplified Block Diagram

Pin Description

Name	Location	I/O	Description
VS1	Block 1	Power	**Switching node:** and ZVS sense for power switches.
VIN	Block 3	Power	**Input voltage:** and sense for UVLO, OVLO and feed forward ramp.
VDR	5K	I/O	**Gate Driver VCC:** Internally generated 5.1V. May be used as a bias supply for low power external loads. See Application Description for important considerations.
SYNCI	4K	I	**Synchronization input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use. The PI3527-65 is not optimized for external synchronization functionality. Refer to Application Description of Parallel Operation for details.
SYNCO	3K	O	**Synchronization output:** Outputs a high signal at the start of each clock cycle for the longer of ½ of the minimum period or the on time of the high side switch.
TEST1	2K	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
TEST2	1K	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
TEST3	1J	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
TEST4	1H	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
TEST5	1E	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
PWRGD	1G	O	**Power Good:** High impedance when regulator is operating and V_{OUT} is in regulation. Otherwise pulls to SGND.
EN	1F	I/O	**Enable Input:** Regulator enable control. When asserted active or left floating: regulator is enabled. Otherwise regulator is disabled.
SGND	Block 5		**Signal ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO communication returns. SGND and PGND are star connected within the regulator package.
TRK	1C	I	**Soft-start and track input:** An external capacitor may be connected between TRK pin and SGND to increase the rise time of the internal reference during soft-start.
COMP	1B	O	**Compensation Capacitor:** Connect capacitor for control loop dominant pole. See Error Amplifier section for details. A default C_{COMP} of 4.7nF is used in the example.
EAO	1A	O	**Error amp output:** External connection for additional compensation and current sharing.
EAIN	2A	I	**Error Amp Inverting Input:** Connection for the main Vout feedback divider tap.
VDIFF	3A	O	**Independent Amplifier Output:** Active only when module is enabled.
VSN	4A	I	**Independent Amplifier Inverting Input:** If unused connect in unity gain.
VSP	5A	I	**Independent Amplifier Non-Inverting Input:** If unused connect to SGND.
VOUT	6A,B	Power	**Direct V_{OUT} Connect:** for per-cycle internal clamp node and feed-forward ramp.
PGND	Block2	Power	**Power Ground:** V_{IN} and V_{OUT} power returns.

Package Pin-Out

PI332x & PI352x
TOP THROUGH VIEW OF PRODUCT

110 Pad LGA SiP (10mm x 14mm)
Top view

Pin Block Name	Group of pins
VIN	A8-10, B8-10, C8-10, D8-10, E8-10, F8-10, G8-10, H8-10, J8-10, K8-10
VS1	A14, B14, C14, D14, E14, F14, G14, H14, J14, K14
PGND	A12, B12, C12, D12, E12, F12, G12, H12, J12, K12
PGND	B5, C4-6, D4-6, E4-6, F2-6, G2-6, H2-6, J2-6, K6
VOUT	A6, B6
SGND	B2-4, C2-3, D1-3, E2-3

PI3527-65 Electrical Characteristics

Specifications apply for -40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, L = 480nH unless otherwise noted. [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Amp						
Open Loop Gain			96	120	140	dB
Small Signal Gain-bandwidth			5	7	12	MHz
Input Offset				0.5	1	mV
Common Mode Input Range			-0.1		2.5	V
Differential Mode Input Range					2	V
Input Bias Current			-1		1	µA
Output Current			-1		1	mA
Maximum V_{OUT}		I_{VDIFF} = -1mA	4.85			V
Minimum V_{OUT}		I_{VDIFF} = -1mA			20	mV
Capacitive Load Range for Stability			0		50	pF
Slew Rate				11		V/µs
PWRGD						
V_{OUT} Rising Threshold	$V_{PG\_HI\%}$		78	84	90	% V_{OUT_DC}
V_{OUT} Falling Threshold	$V_{PG\_LO\%}$		75	81	87	% V_{OUT_DC}
PWRGD Output Low	V_{PG_SAT}	Sink = 4mA			0.4	V
VDR						
Voltage Setpoint	V_{VDR}	V_{IN_DC} > 10V	4.9	5.05	5.2	V
External Loading	I_{VDR}	See Application Description for details	0		2	mA
Enable						
High Threshold	V_{EN_HI}		0.9	1.0	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Pull-Up Voltage Level for Source Current	V_{EN_PU}			2		V
Pull-Up Current	$I_{EN\_PU\_POS}$	V_{IN} > 8V, excluding t_{FR_DLY}		50		µA
Reliability						
MTBF		MIL-HDBK-217, 25°C, Ground Benign: GB		12.6		MHrs
		Telcordia SR-332, 25°C, Ground Benign: GB		96.9		MHrs

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI352x evaluation board with 3.1 x 3.3" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

PI3527-65 Electrical Characteristics (Cont.)

Specifications apply for -40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, L = 480nH unless otherwise noted. [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		30	48	65	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_{CASE} = 25°C, I_{OUT} = 18A		4.68		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	Short at terminals		4.5		mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.75	1.2	mA
Input Quiescent Current	I_{Q_VIN}	Enabled, no load, T_{CASE} = 25°C		3.2		mA
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Input capacitance, Internal	C_{IN_INT}	Effective value V_{IN} = 48V, 25°C		0.50		µF
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[2]	0.975	0.990	1.005	V
Output Voltage Trim Range	V_{OUT_DC}	[2] [3]	6.5	12.0	15.0	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	@ 25°C, 30V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	@ 25°C, 2A < I_{OUT} < 20A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 18A, C_{OUT} = 8 x 10µF, 20MHz BW [4]		240		mVp-p
Output Current	I_{OUT_DC}	[5]	0		18	A
Current Limit	I_{OUT_CL}	Typical current limit based on nominal 480nH inductor.		20.7		A
Maximum Array Size	$N_{PARALLEL}$	[2]			3	Modules
Output Current, array of 2	$I_{OUT\_DC\_ARRAY2}$	Total array capability, [2] see applications section for details	0		[7]	A
Output Current, array of 3	$I_{OUT\_DC\_ARRAY3}$	Total array capability, [2] see applications section for details	0		[7]	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}			27	29.1	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		1.66	2.08	2.50	V
Input UVLO Response Time				1.25		µs
Input OVLO Stop Threshold	V_{OVLO}	[2]	66.5			V
Input OVLO Start Hysteresis	V_{OVLO_HYS}	Hysteresis active when OVLO present for at least t_{FR_DLY} [2]		1.30		V
Input OVLO Response Time	t_f			1.25		µs
Output Overvoltage Protection, Relative	V_{OVP_REL}	Above set V_{OUT}		20		%
Output Overvoltage Protection, Absolute	V_{OVP_ABS}		15.6	16.5		V

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[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.
[7] Contact factory applications for array derating and layout best practices to minimize sharing errors.

PI3527-65 Electrical Characteristics (Cont.)

Specifications apply for -40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, L = 480nH unless otherwise noted. [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_s	[6] While in DCM operating mode only, SYNCI grounded	658	700	742	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Synchronization Input (SYNCI)						
Synchronization Frequency Range	f_{SYNCI}	-50% and +10% relative to set switching frequency (f_S), while in DCM operating mode only. [3] and [6]	350		770	kHz
SYNCI Threshold	V_{SYNCI}			2.5		V
Synchronization Output (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EAIN_OV}		50	80	110	mV
Charge Current (Soft Start)	I_{TRK}		30	50	70	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		8.7		mA
TRK Capacitance, Internal	C_{TRK_INT}			47		nF
Soft-Start Time	t_{SS}	C_{TRK_EXT} = 0µF	0.6	0.94	1.6	ms
Error Amplifier Trans-Conductance	GM_{EAO}	[2]		7.6		mS
PSM Skip Threshold	PSM_{SKIP}	[2]		0.8		V
EAIN Capacitance, Internal	$C_{EAIN-INT}$			56		pF
Error Amplifier Output Impedance	R_{OUT}	[2]	1			MΩ
Internal Compensation Capacitor	C_{HF}	[2]		56		pf
Internal Compensation Resistor	R_{ZI}	[2]		5		kΩ

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI352x evaluation board with 3.1 x 3.3" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
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[6] Refer to Switching Frequency vs. Load current curves.

PI3527-65 Electrical Characteristics (Cont.)

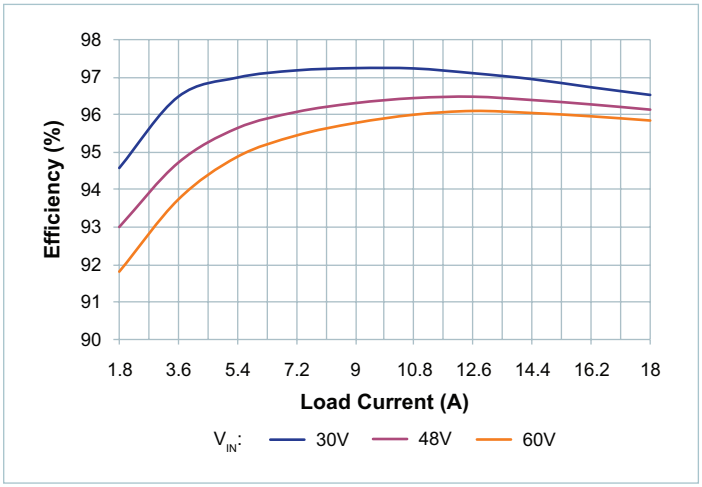


Figure 1 — *System Efficiency, 12V Trim, Board Temperature = 25°C*

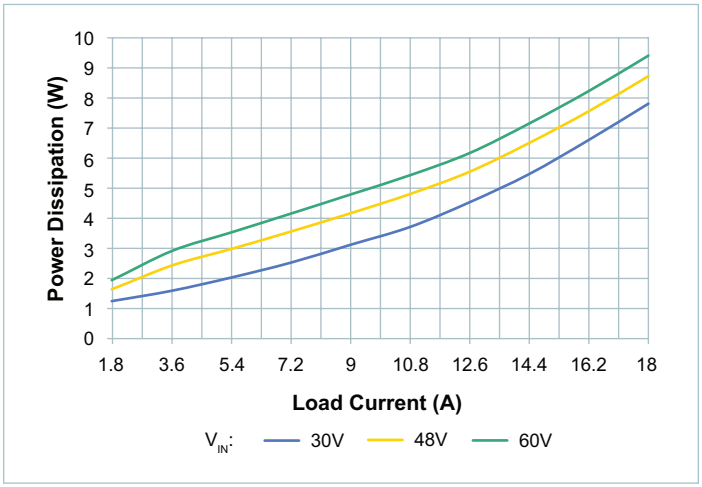


Figure 4 — *System Power Dissipation, 12V Trim, Board Temperature = 25°C*

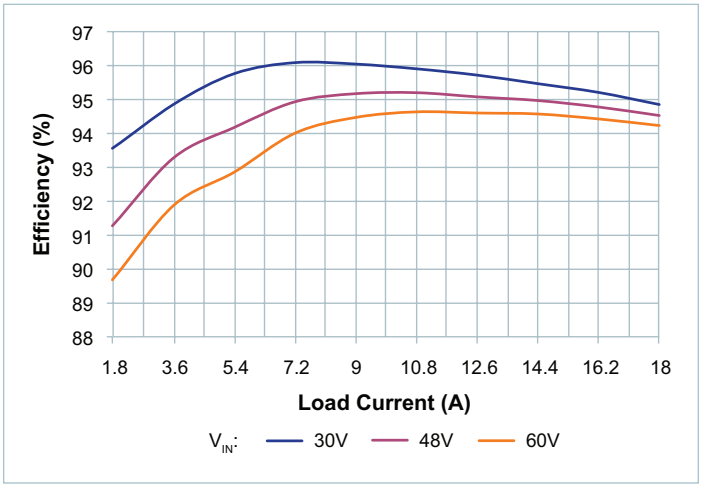


Figure 2 — *System Efficiency, 6.5V Trim, Board Temperature = 25°C*

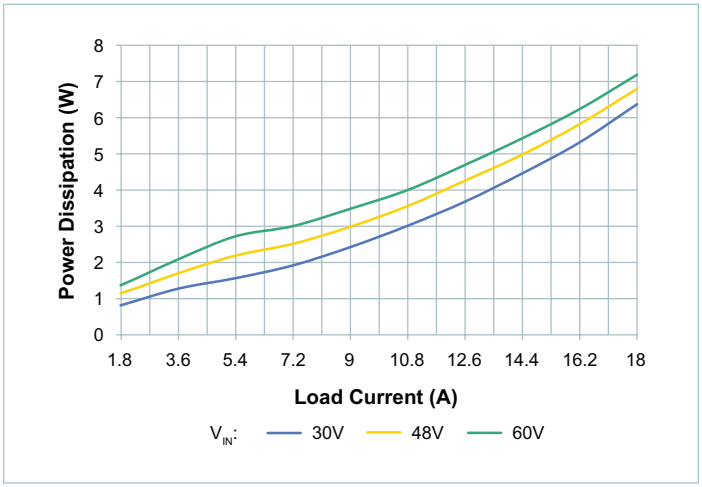


Figure 5 — *System Power Dissipation, 6.5V Trim, Board Temperature = 25°C*

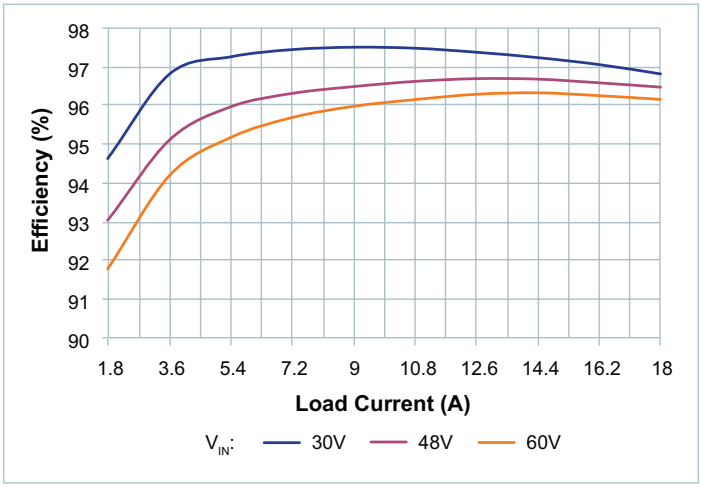


Figure 3 — *System Efficiency, 14V Trim, Board Temperature = 25°C*

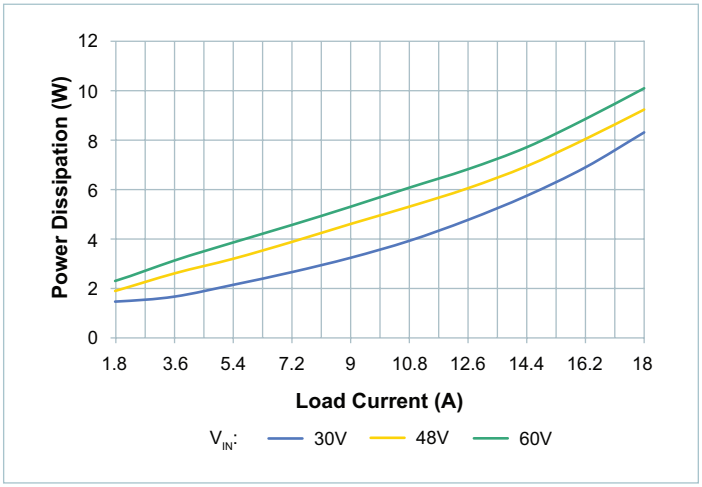


Figure 6 — *System Power Dissipation, 14V Trim, Board Temperature = 25°C*

PI3527-65 Electrical Characteristics (Cont.)

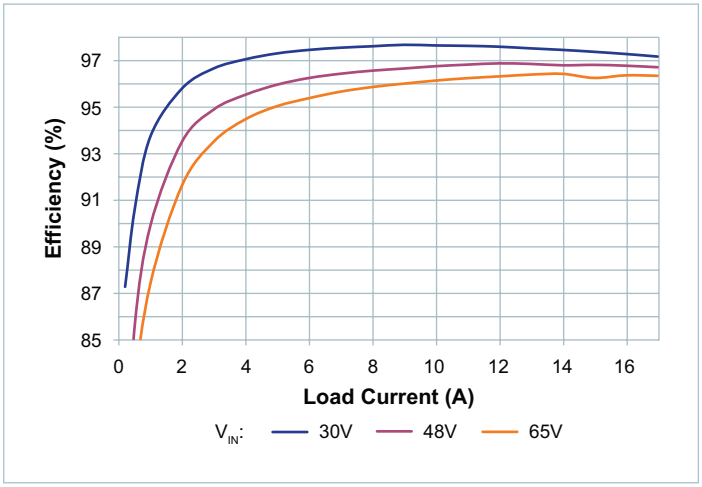


Figure 7 — *System Efficiency, 15V Trim, Board Temperature = 25°C*

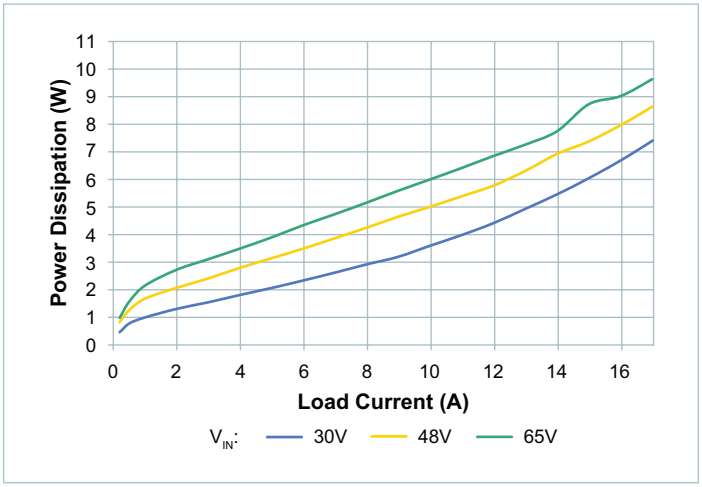


Figure 10 — *System Power Dissipation, 15V Trim, Board Temperature = 25°C*

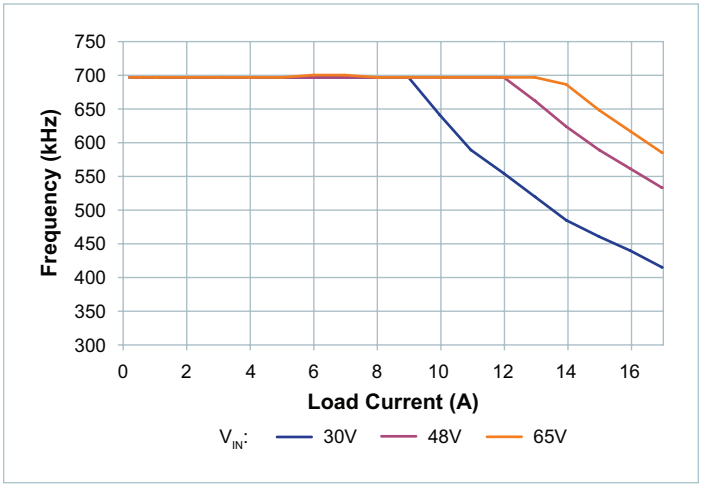


Figure 8 — *Switching Frequency vs. Load, 15V Trim*

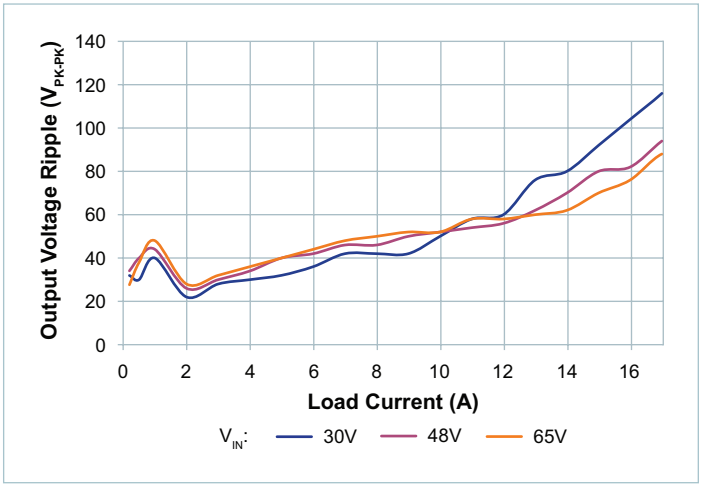


Figure 11 — *Output Voltage Ripple: 15V Trim*

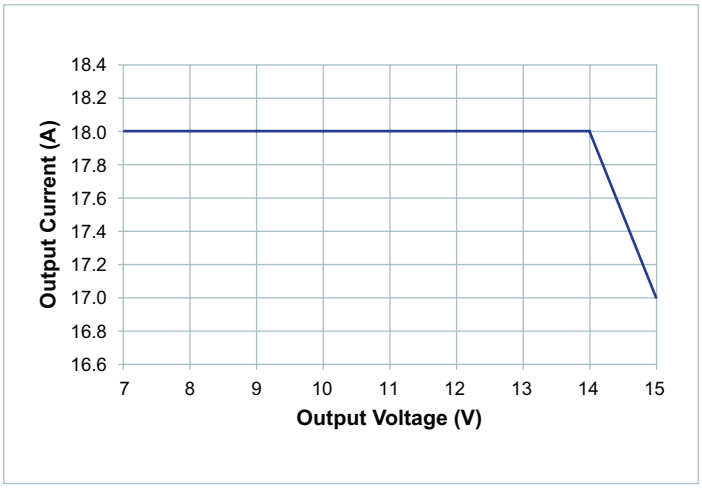


Figure 9 — *Output current derating*

PI3527-65 Electrical Characteristics (Cont.)

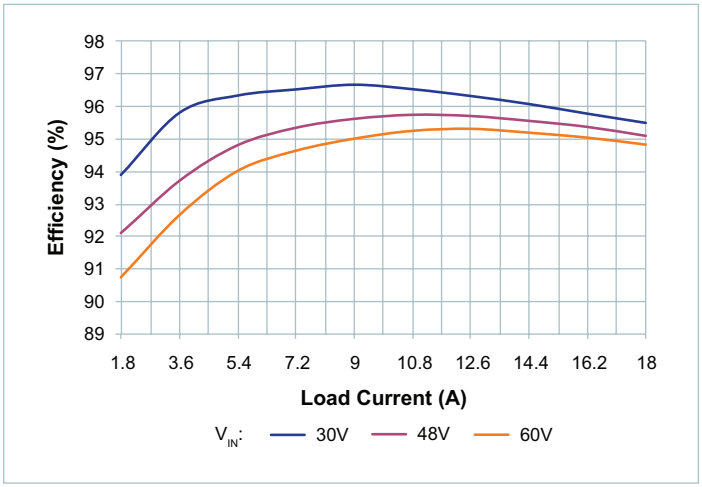


Figure 12 — *System Efficiency, 12V Trim, Board Temperature = 100°C*

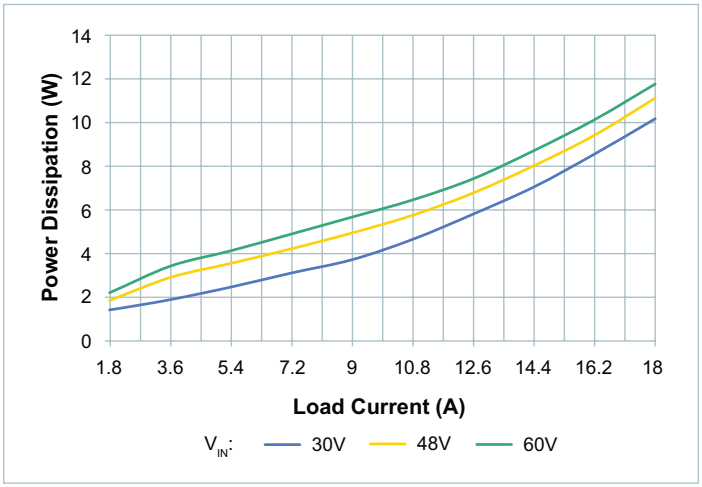


Figure 15 — *System Power Dissipation, 12V Trim, Board Temperature = 100°C*

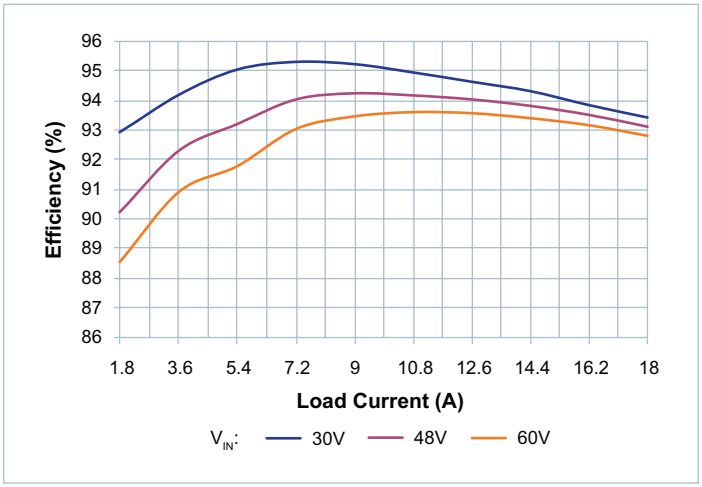


Figure 13 — *System Efficiency, 6.5V Trim, Board Temperature = 100°C*

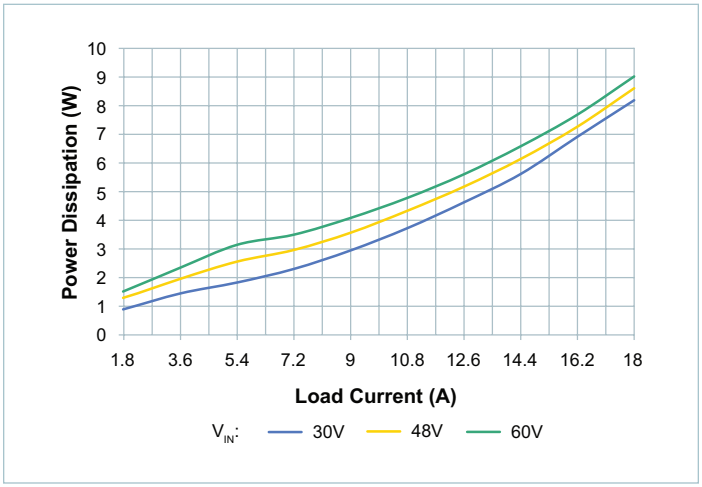


Figure 16 — *System Power Dissipation, 6.5V Trim, Board Temperature = 100°C*

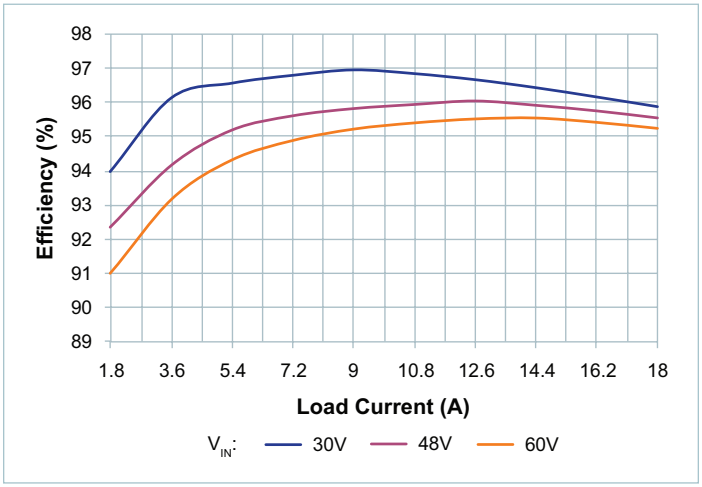


Figure 14 — *System Efficiency, 14V Trim, Board Temperature = 100°C*

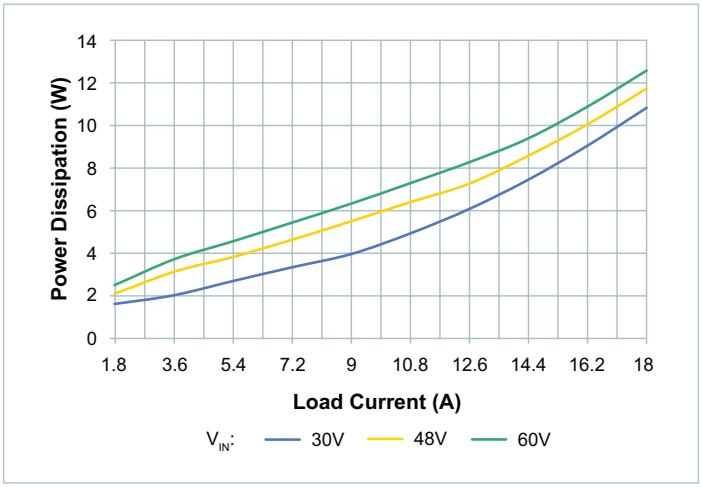


Figure 17 — *System Power Dissipation, 14V Trim, Board Temperature = 100°C*

PI3527-65 Electrical Characteristics (Cont.)

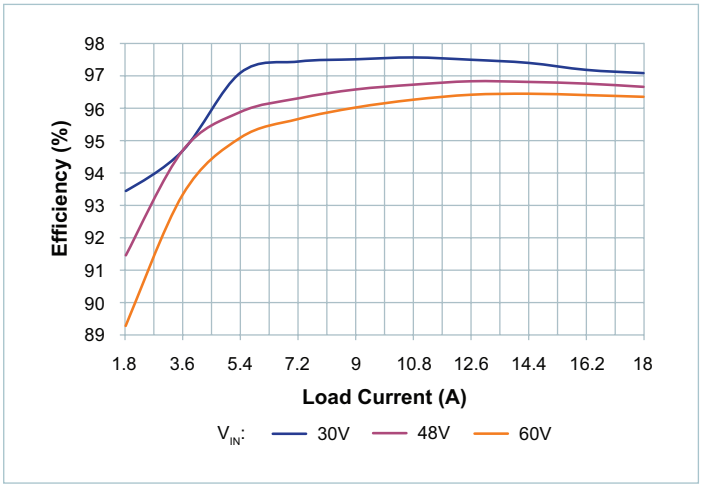


Figure 18 — *System Efficiency, 12V Trim, Board Temperature = -40°C*

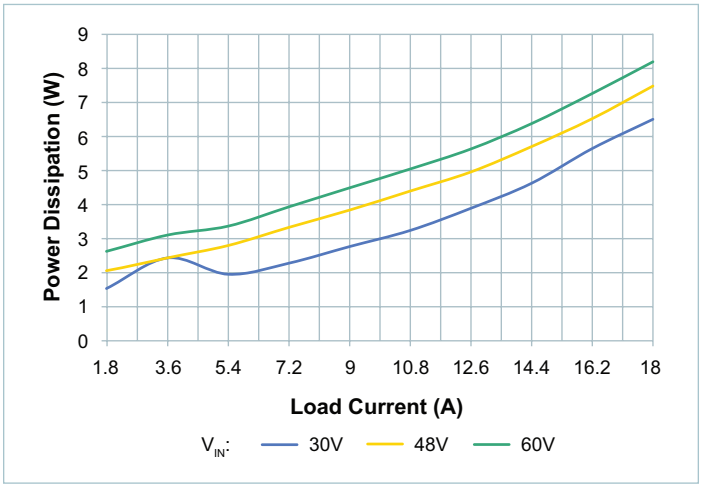


Figure 21 — *System Power Dissipation, 12V Trim, Board Temperature = -40°C*

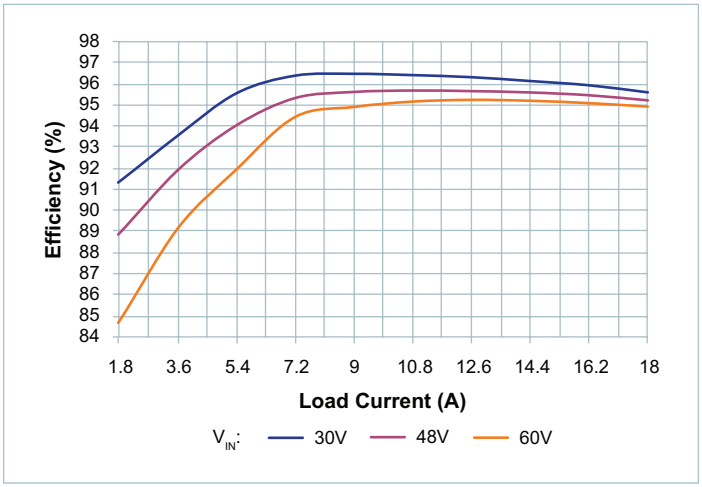


Figure 19 — *System Efficiency, 6.5V Trim, Board Temperature = -40°C*

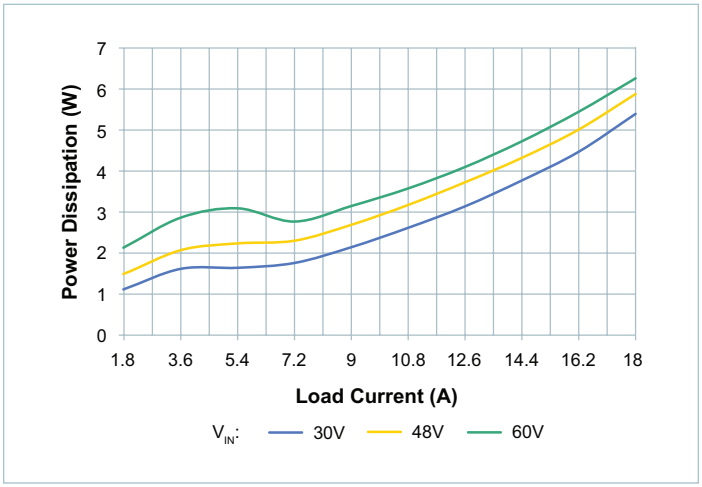


Figure 22 — *System Power Dissipation, 6.5V Trim, Board Temperature = -40°C*

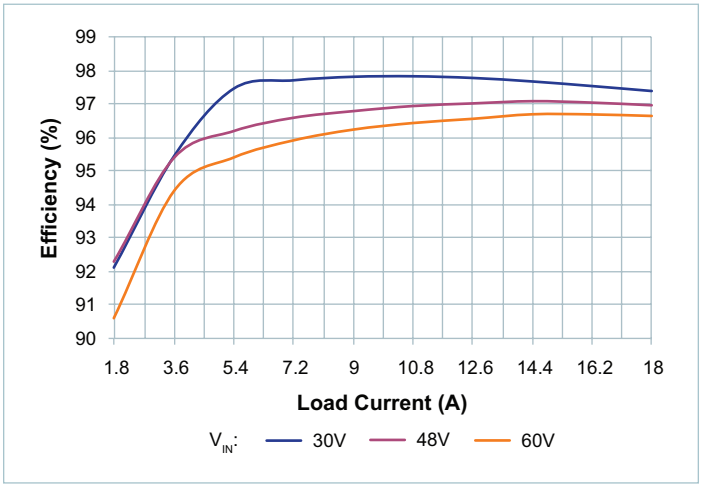


Figure 20 — *System Efficiency, 14V Trim, Board Temperature = -40°C*

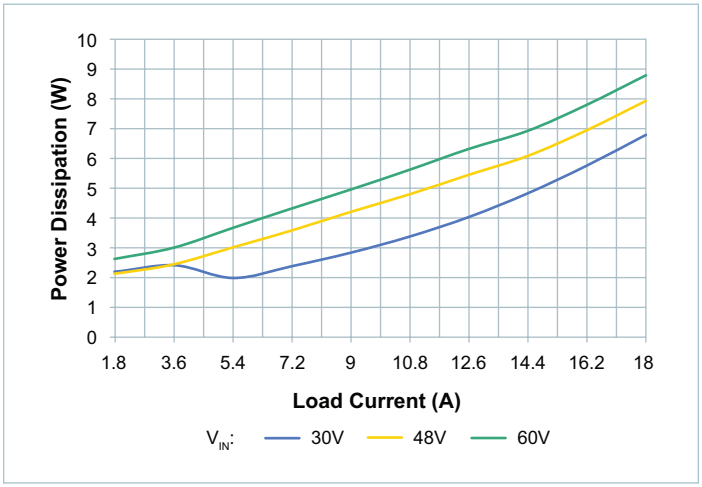


Figure 23 — *System Power Dissipation, 14V Trim, Board Temperature = -40°C*

PI3527-65 Electrical Characteristics (Cont.)

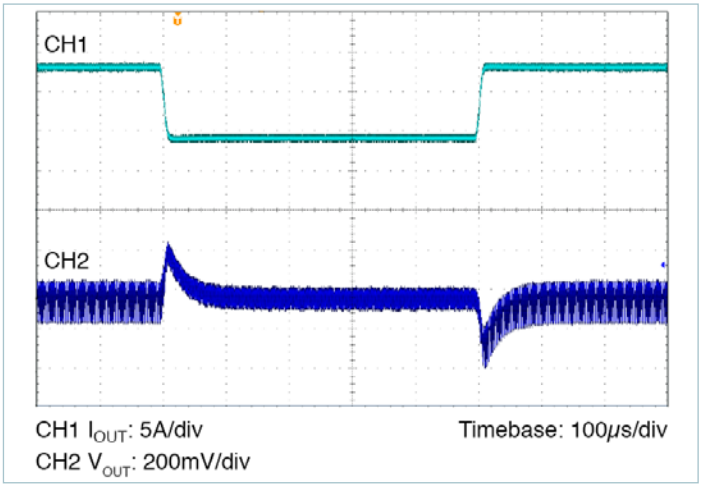


Figure 24 — *Transient Response: 50% to 100% load, at 1A/µs. Nominal Line, 12V Trim, C_{OUT} = 8 x 10µF Ceramic*

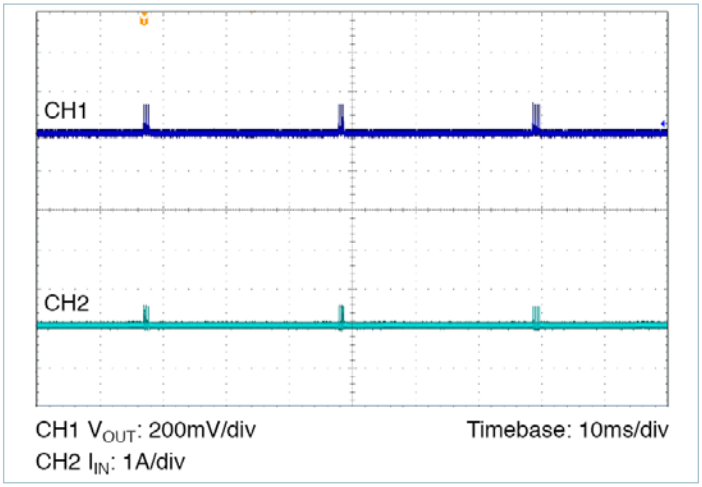


Figure 27 — *Output Short Circuit, Nominal Line*

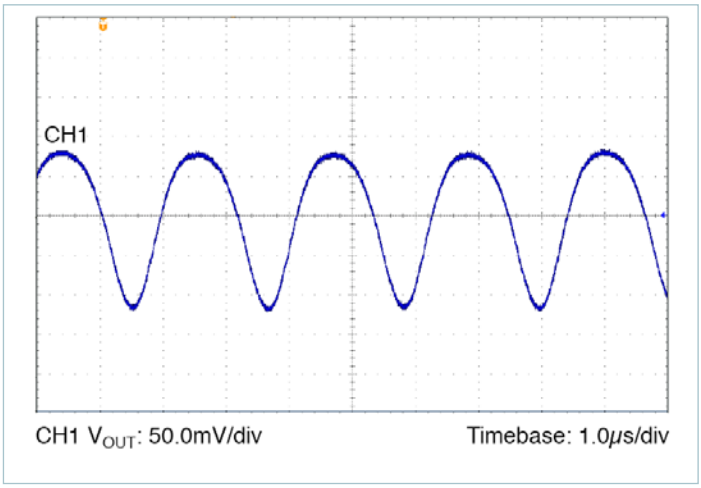


Figure 25 — *Output Voltage Ripple: Nominal Line, 12V Trim, 100% load, C_{OUT} = 8 x 10µF Ceramic*

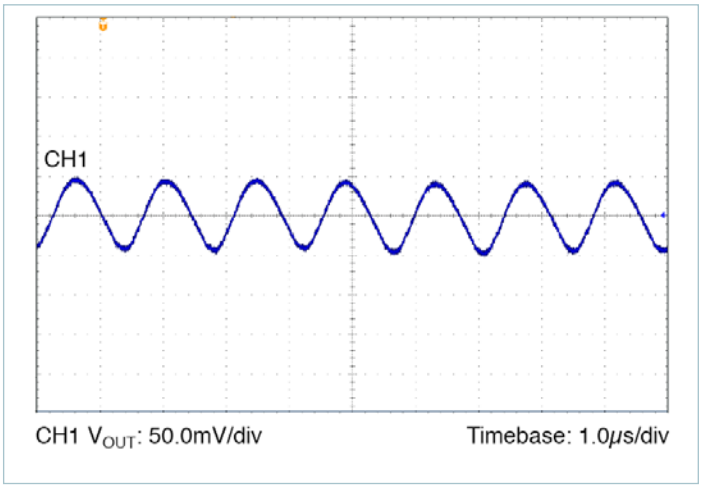


Figure 28 — *Output Voltage Ripple: Nominal Line, 12V Trim, 50% load, C_{OUT} = 8 x 10µF Ceramic*

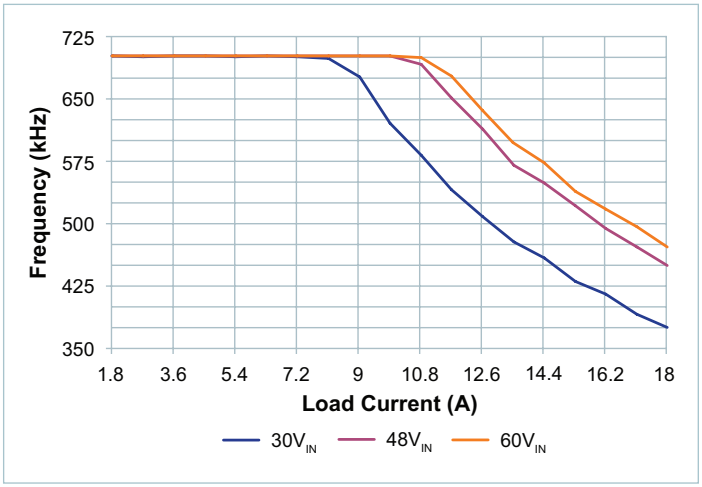


Figure 26 — *Switching Frequency vs. Load, 12V Trim*

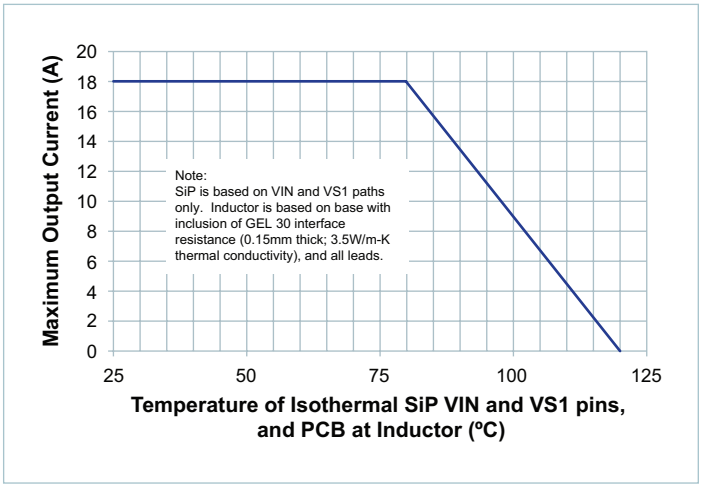


Figure 29 — *System Thermal Specified Operating Area: Max I_{OUT} at 12V Trim vs. temperature at locations noted*

PI3527-65 Electrical Characteristics (Cont.)

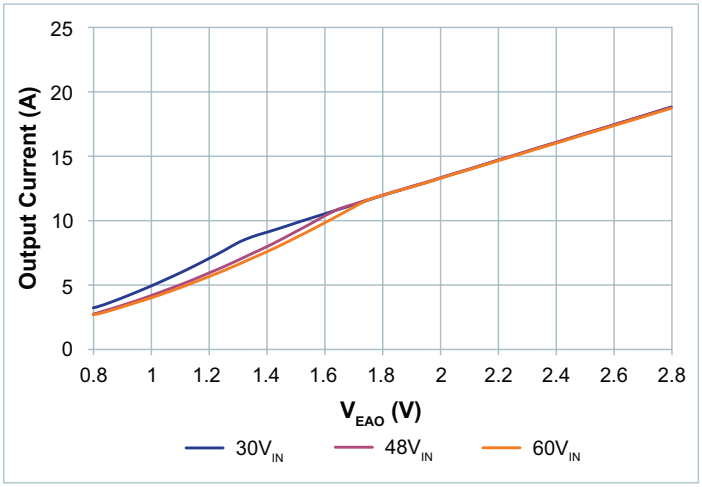


Figure 30 — *Output Current vs. V_{EAO}, 12V Trim*

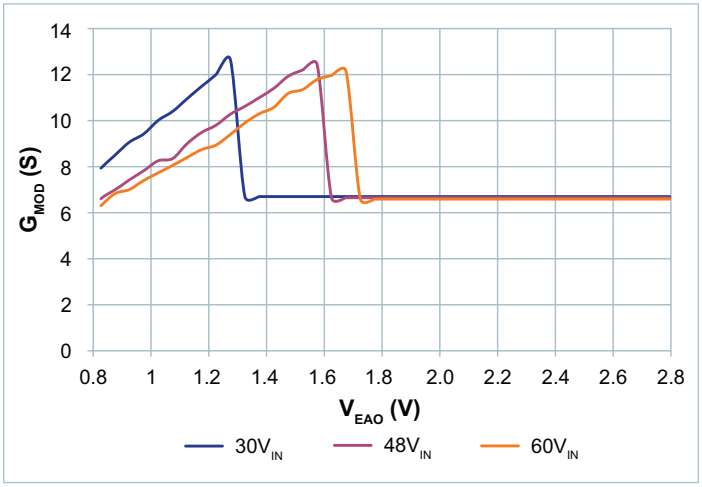


Figure 31 — *Small Signal Modulator Gain vs. V_{EAO}, 12V Trim*

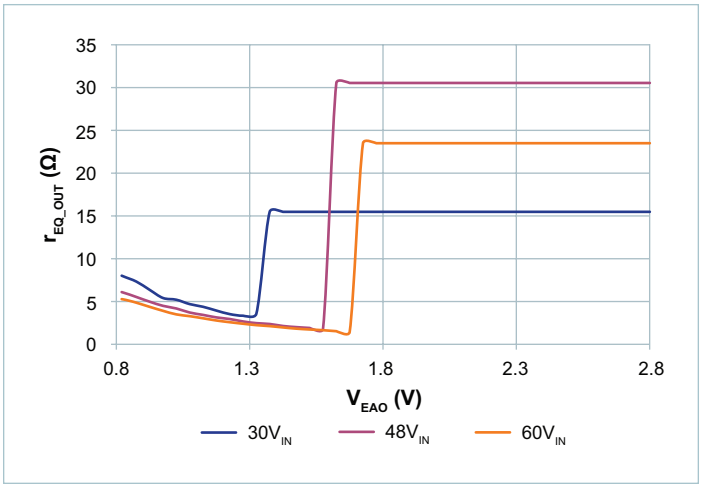


Figure 32 — *r_{EQ_OUT} vs V_{EAO}, 12V Trim*

Functional Description

The PI3527-65 is a highly integrated ZVS Buck regulator. The PI3527-65 has an output voltage that can be set within a prescribed range shown in Table 1. Performance and maximum output current are characterized with a specific external power inductor (see Table 4).

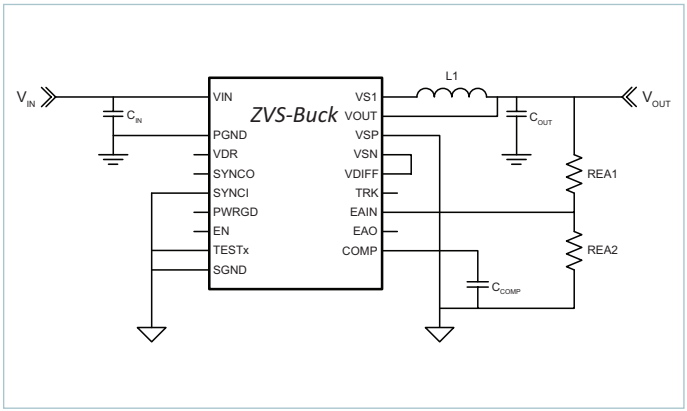


Figure 33 — *ZVS Buck with required components*

For basic operation, Figure 33 shows the connections and components required. No additional design or settings are required.

ENABLE (EN)

EN is the enable pin of the converter. The EN Pin is referenced to SGND and permits the user to turn the regulator on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below V_{EN_LO} with respect to SGND will disable the regulator output.

Remote Sensing

If remote sensing is required, the PI3527-65 is equipped with a general purpose op-amp. This amplifier can allow full differential remote sense by configuring it as a differential follower and connecting the VDIFF pin to the EAIN pin.

Soft-Start

The PI3527-65 includes an internal soft-start capacitor to control the rate of rise of the output voltage. See the Electrical Characteristics Section for the default value. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, "Soft Start Adjustment and Track," in the Applications Description section for more details.

Output Voltage Selection

The PI3527-65 output voltage can be trimmed with REA1 and REA2 as shown in Figure 33. Table 1 defines the allowable operational voltage ranges for the PI3527-65. Refer to the Output Voltage Set Point Application Description for details.

Device	Output Voltage	
	Nom.	Range
PI3527-65-LGIZ	12V	6.5V to 15V

Table 1 — *PI3527-65 output voltage range*

Output Current Limit Protection

The PI3527-65 has a current limit protection, which prevents the output from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for 1024µs, a slow current limit fault is initiated and the regulator is shutdown which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

The PI3527-65 also has short circuit protection which can immediately stop switching to protect against catastrophic failure of an external component such as a saturated inductor. If short circuit protection is triggered the PI3527-65 will complete the current cycle and stop switching. The module will attempt to soft-start after Fault Restart Delay (t_{FR_DLY}).

Input Undervoltage Lockout

If V_{IN} falls below the input Undervoltage Lockout (UVLO) threshold, but remains high enough to power the internal bias supply, the PI3527-65 will complete the current cycle and stop switching. The system will soft start once the input voltage is reestablished and after the Fault Restart Delay.

Input Overvoltage Lockout

If V_{IN} exceeds the input Overvoltage Lockout (OVLO) threshold (V_{OVLO}), while the controller is running, the PI3527-65 will complete the current cycle and stop switching. If V_{IN} remains above OVLO for at least t_{FR_DLY}, then the input voltage is considered reestablished once V_{IN} goes below V_{OVLO}-V_{OVLO_HYS}. If V_{IN} goes below OVLO before t_{FR_DLY} elapses, then the input voltage is considered reestablished once V_{IN} goes below V_{OVLO}. The system will soft start once the input voltage is reestablished and after the Fault Restart Delay.

Output Overvoltage Protection

The PI3527-65 is equipped with output Overvoltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds $V_{OVP\text{-}REL}$ or $V_{OVP\text{-}ABS}$, the regulator will complete the current cycle and stop switching. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

Overtemperature Protection

The PI3527-65 features an over temperature protection (OTP), which will not engage until after the product is operated above the maximum rated temperature. The OTP circuit is only designed to protect against catastrophic failure due to excessive temperatures and should not be relied upon to ensure the device stays within the recommended operating temperature range. Thermal shutdown terminates switching and discharges the soft-start capacitor. The PI3527-65 will restart after the excessive temperature decreases by 30°C.

Pulse Skip Mode (PSM)

PI3527-65 features a Pulse Skip Mode (PSM) to achieve high efficiency at light loads. The regulators are setup to skip pulses if EAO falls below a PSM threshold (PSM_{SKIP}). Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Pulse Skip Mode threshold.

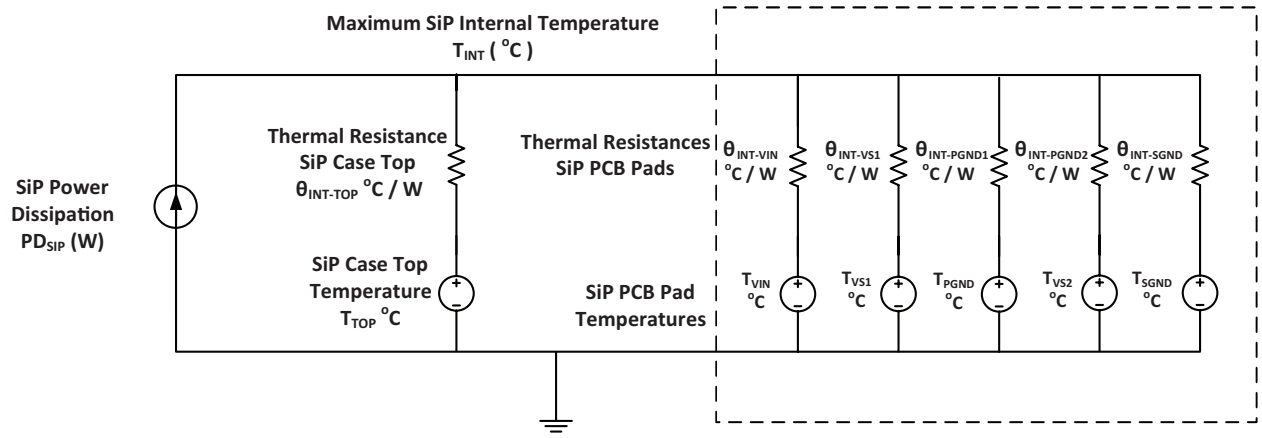
Variable Frequency Operation

Each PI3527-65 is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 4), to operate at peak efficiency across line and load variations. At low line and high load applications, the base frequency will decrease to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

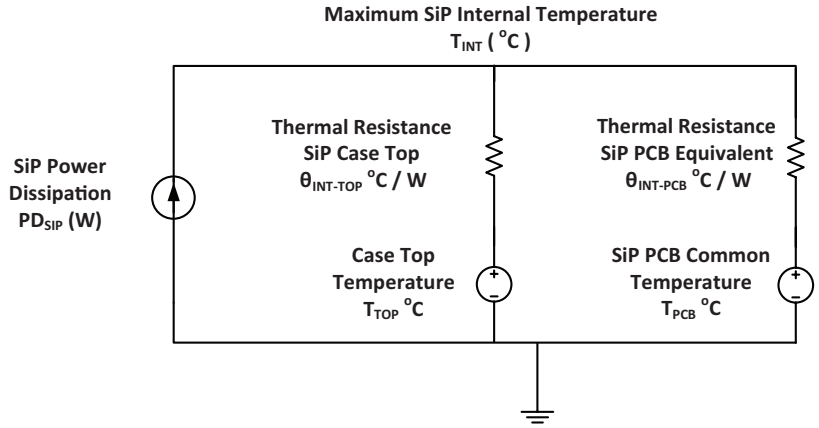
Thermal Characteristics

Figure 34(a) and 34(c) thermal impedance models that can predict the maximum temperature of the hottest component for a given operating condition. This model assumes that all customer PCB connections are at one temperature, which is PCB equivalent Temperature T_{PCB} °C.

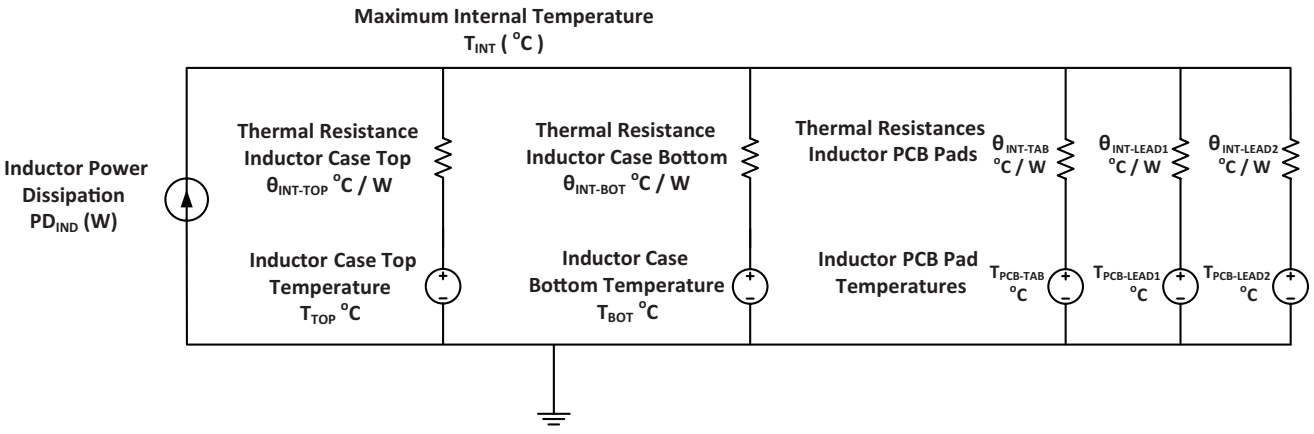
The SiP model can be simplified as shown in Figure 34(b). which assumes all PCB nodes are at the same temperature.



(a)



(b)



(c)

Figure 34 — *PI3527-65 Thermal model (a), SiP simplified version (b) and inductor thermal model (c)*

Where the symbol in Figure 34(a) and (b) is defined as the following:

$\theta_{INT-TOP}$	the thermal impedance from the hottest component inside the SiP to the top side.
$\theta_{INT-PCB}$	the thermal impedance from the hottest component inside the SiP to the customer PCB, assuming all pins are at one temperature.
$\theta_{INT-VIN}$	the thermal impedance from the hottest component inside the SiP to the circuit board VIN pads.
$\theta_{INT-VS1}$	the thermal impedance from the hottest component inside the SiP to the circuit board VS1 pads.
$\theta_{INT-PGND1}$	the thermal impedance from the hottest component inside the SiP to the circuit board at the PGND1 pads. PGND1 is pins 12A-K.
$\theta_{INT-PGND2}$	the thermal impedance from the hottest component inside the SiP to the circuit board at the PGND2 pads . PGND2 is pins 2F-J, 3F-J, 4C-J, 5B-J and 6C-K.
$\theta_{INT-SGND}$	the thermal impedance from the hottest component inside the SiP to the circuit board at the SGND pads.

Where the symbol in Figure 34(c) is defined as the following:

$\theta_{INT-TOP}$	the thermal impedance from the hot spot to the top surface of the core.
$\theta_{INT-PCB}$	the thermal impedance from the hot spot to the circuit board it is mounted on, assuming all customer PCB connections at one temperature.
$\theta_{INT-BOT}$	the thermal impedance from the hot spot to the bottom surface of the core.
$\theta_{INT-TAB}$	the thermal impedance from the hot spot to the metal mounting tab on the core body.
$\theta_{INT-LEAD1}$	the thermal impedance from the hot spot to one of the mounting leads. Since the leads are the same thermal impedance, there is no need to specify by explicit pin number.
$\theta_{INT-LEAD2}$	the thermal impedance from the hot spot to the other mounting lead.

Thermal Characteristics (Cont.)

The following equation can predict the junction temperature based on the heat load applied to the SiP and the known ambient conditions with the simplified thermal circuit model:

$$T_{INT} = \frac{PD + \frac{T_{TOP}}{\theta_{INT\text{-}TOP}} + \frac{T_{PCB}}{\theta_{INT\text{-}PCB}}}{\frac{1}{\theta_{INT\text{-}TOP}} + \frac{1}{\theta_{INT\text{-}PCB}}} \qquad (1)$$

Product System	Simplified SiP Thermal Impedances		Detailed SiP Thermal Impedances					
	$\theta_{INT\text{-}TOP}$ (°C / W)	$\theta_{INT\text{-}PCB}$ (°C / W)	$\theta_{INT\text{-}TOP}$ (°C / W)	$\theta_{INT\text{-}VIN}$ (°C / W)	$\theta_{INT\text{-}VS1}$ (°C / W)	$\theta_{INT\text{-}PGND1}$ (°C / W)	$\theta_{INT\text{-}PGND2}$ (°C / W)	$\theta_{INT\text{-}SGND}$ (°C / W)
PI3527-65	108	1.79	108.25	3.40	5.75	23.80	26.65	86.44

Table 2 — *PI3527-65 SiP Thermal Impedance*

Inductor Part Number	Thermal Impedances						Simplified SiP Thermal Impedances	
	$\theta_{INT\text{-}TOP}$ (°C / W)	$\theta_{INT\text{-}BOT}$ (°C / W)	$\theta_{INT\text{-}TAB}$ (°C / W)	$\theta_{INT\text{-}LEAD1}$ (°C / W)	$\theta_{INT\text{-}LEAD2}$ (°C / W)	$\theta_{INT\text{-}LEADS}$ (°C / W)	$\theta_{INT\text{-}TOP}$ (°C / W)	$T_{INT\text{-}PCB}$ (°C)
HCV1707R1-R48-R	65.41	20.46	700	17.74	17.74	8.87	65.41	6.13

Table 3 — *Inductor thermal model parameters*

SiP Power Dissipation as Percentage of Total System Losses

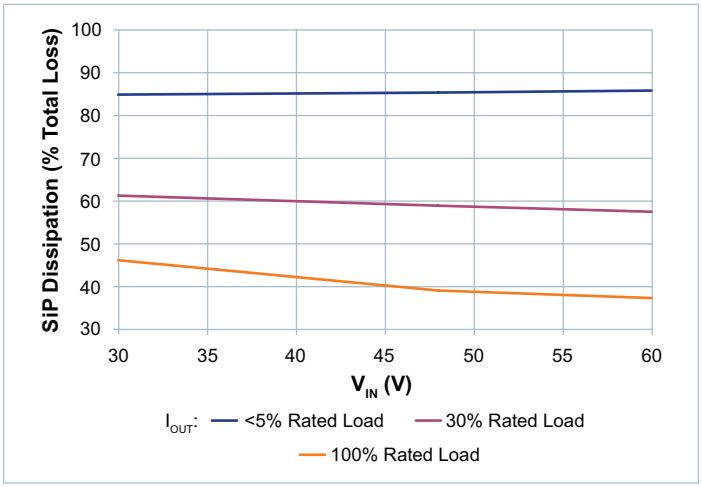


Figure 35 — *PI3527-65-LGIZ*

Application Description

Output Voltage Set Point

The PI3527-65 Buck Regulator utilizes V_{REF}, an internal reference for regulating the output voltage. The output voltage setting is accomplished using external resistors as shown in Figure 36. Select R2 to be at or around 1kΩ for best noise immunity. Use Equations (2) and (3) to determine the proper value based on the desired output voltage.

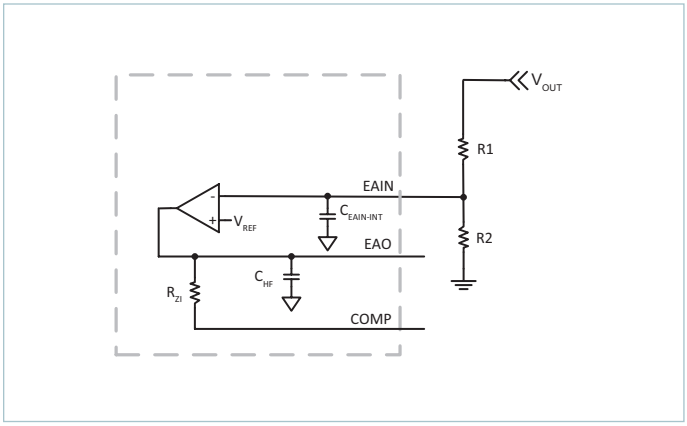


Figure 36 — *External resistor divider network*

$$V_{OUT} = V_{REF} \bullet \frac{R1 + R2}{R2} \qquad (2)$$

$$R1 = R2 \bullet \frac{V_{OUT} - V_{REF}}{V_{REF}} \qquad (3)$$

$$where\ V_{REF} = V_{EAIN}$$

Note: When using the above method of trimming by adjusting the value of R1, the compensation of the control loops is modified and additional C_{OUT} may be needed.

Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal capacitor and a fixed charge current to provide a Soft-Start Time t_{SS} for the PI3527-65 regulators. By adding an additional external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start time in excess of t_{SS}:

$$C_{TRK} = (t_{TRK} \bullet I_{TRK}) - C_{TRK\_INT} \qquad (4)$$

where t_{TRK} is the soft-start time and I_{TRK} is a 50µA internal charge current (see Electrical Characteristics for limits).

In applications such as battery or super-capacitor charging where the load is pre-biased, the PI3527-65 can start into output voltages up to the externally applied trim setpoint, or the minimum absolute OVP, provided the value does not exceed 6V. For startup into loads which are pre-biased above 6V, an ORing FET or equivalent sub-circuit is required to decouple the buck output from the load during startup. In any application with a CV type load, the regulator must be configured in a constant-current mode of operation; the built-in current limit is a fault protection only.

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at startup, simply connect all PI3527-65 device TRK pins together. This type of tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 37a).

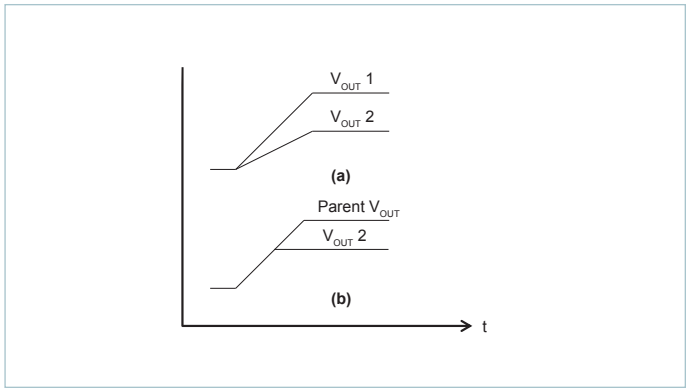


Figure 37 — *PI3527-65 tracking responses*

For Direct Tracking, choose the PI3527-65 with the highest output voltage as the parent and connect the parent to the TRK pin of the other PI3527-65 regulators through a divider (Figure 37) with the same ratio as the child's feedback divider.

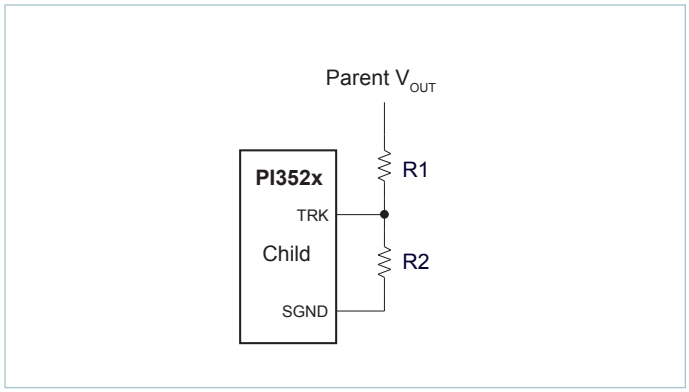


Figure 38 — *Voltage divider connections for direct tracking*

All connected PI3527-65 regulator soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 37b. All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI3527-65 utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 4 details the specific inductor value and part number utilized for the PI3527-65.

Product System	Value (nH)	Manufacturer	Part Number
PI3527-65-LGIZ	480	Eaton	HCV1707R1-R48-R

Table 4 — *PI3527-65 Inductor pairing*

Parallel Operation

Multiple PI3527-65 can be connected in parallel to increase the output capability of a single output rail. When connecting modules in parallel, each EAO, TRK, and EN pin should be connected together. EAIN pins should remain separated, each with an REA1 and REA2, to reject noise differences between different modules' SGND pins. Current sharing will occur automatically in this manner so long as each inductor is the same value. Refer to the Electrical Characteristics table for maximum array size and array rated output current. Current sharing may be considered independent of synchronization and/or interleaving. Modules do not have to be interleaved or synchronized to share current.

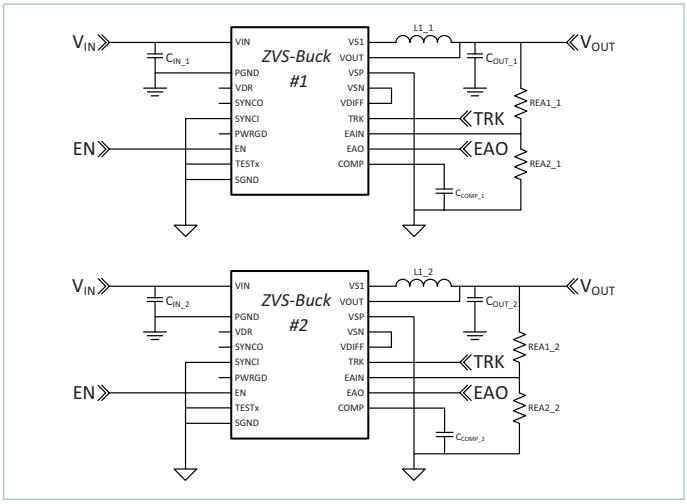


Figure 39 — *PI3527-65 parallel operation*

Due to the high output current capability of a single module and Critical Conduction Mode (CrCM) occurring at approximately 50% rated load, interleaving is not supported.

Use of the PI3527-65 SYNCI pin is practical only under a limited set of conditions. Synchronizing to another converter or to a fixed external clock source can result in a significant reduction in output power capability or higher than expected ripple.

Filter Considerations

The PI3527-65 requires low impedance ceramic input capacitors (X7R/X5R or equivalent) to ensure proper start up and high frequency decoupling for the power stage. The PI3527-65 will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET(s) are conducting. During the time the MOSFET(s) are off, the input capacitors are replenished from the source.
Table 6 shows the recommended input and output capacitors to be used for the PI3527-65 as well as per capacitor RMS ripple current and the input and output ripple voltages. Table 5 lists the recommended input and output ceramic capacitors manufacturer and part numbers. It is very important to verify that the voltage supply source as well as the interconnecting lines are stable and do not oscillate.

Input Filter Case 1 — Inductive source and local, external, input decoupling capacitance with negligible ESR (i.e.: ceramic type):

The voltage source impedance can be modeled as a series R_{line} L_{line} circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{line} > \frac{L_{line}}{\left(C_{IN\_INT} + C_{IN\_EXT}\right) \bullet \left| r_{EQ\_IN} \right|} \qquad (5)$$

$$R_{line} << \left| r_{EQ\_IN} \right| \qquad (6)$$

Where r_{EQ_IN} can be calculated by dividing the lowest line voltage by the full load input current. It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, Equation (6). However, R_{line} cannot be made arbitrarily low otherwise Equation (5) is violated and the system will show instability, due to an under-damped RLC input network.

Input Filter case 2 — Inductive source and local, external input decoupling capacitance with significant $R_{C_{IN\_EXT}}$ ESR (i.e.: electrolytic type):

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor L_{line}.

Notice that the high performance ceramic capacitors C_{IN_INT} within the PI3527-65 should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$\left|r_{EQ\_IN}\right| > R_{C_{IN\_EXT}} \quad (7)$$

$$\frac{L_{line}}{C_{IN\_INT} \bullet R_{C_{IN\_EXT}}} < \left|r_{EQ\_IN}\right| \quad (8)$$

Equation (8) shows that if the aggregate ESR is too small – for example by using very high quality input capacitors (C_{IN_EXT}) – the system will be under-damped and may even become destabilized. As noted, an octave of design margin in satisfying Equation (7) should be considered the minimum. When applying an electrolytic capacitor for input filter damping the ESR value must be chosen to avoid loss of converter efficiency and excessive power dissipation in the electrolytic capacitor.

VDR Bias Regulator

The VDR internal bias regulator is a ZVS switching regulator that resides internal to the PI3527-65 SiP. It is intended primarily to power the internal controller and driver circuitry. The power capability of this regulator is sized for the PI3527-65, with adequate reserve for the application it was intended for.

It may be used for as a pullup source for open collector applications and for other very low power uses with the following restrictions:

1. The total external loading on VDR must be less than I_{VDR}.

2. No direct connection is allowed. Any noise source that can disturb the VDR voltage can also affect the internal controller operation. A series impedance is required between the VDR pin and any external circuitry.

3. All loads must be locally de-coupled using a 0.1µF ceramic capacitor. This capacitor must be connected to the VDR output through a series resistor no smaller than 1kΩ, which forms a low-pass filter.

Additional System Design Considerations

1. *Inductive loads:* As with all power electronic applications, consideration must be given to driving inductive loads that may be exposed to a fault in the system which could result in consequences beyond the scope of the power supply primary protection mechanisms. An inductive load could be a filter, fan motor or even excessively long cables. Consider an instantaneous short circuit through an un-damped inductance that occurs when the output capacitors are already at an initial condition of fully charged. The only thing that limits the current is the inductance of the short circuit and any series resistance. Even if the power supply is off at the time of the short circuit, the current could ramp up in the external inductor and store considerable energy. The release of this energy will result in considerable ringing, with the possibility of ringing nodes connected to the output voltage below ground. The system designer should plan for this by considering the use of other external circuit protection such as load switches, fuses, and transient voltage protectors. The inductive filters should be critically damped to avoid excessive ringing or damaging voltages. Adding a high current Schottky diode from the output voltage to PGND close to the PI3527-65 is recommended for these applications.

2. *Low voltage operation:* There is no isolation from an SELV (Safety-Extra-Low-Voltage) power system. Powering low voltage loads from input voltages as high as 60V may require additional consideration to protect low voltage circuits from excessive voltage in the event of a short circuit from input to output. A fast TVS (transient voltage suppressor) gating an external load switch is an example of such protection.

Input / Output	Manufacturer	Part Number	Value	Description
Input	Murata	GRM32ER71K475KE14L	4.7µF	4.7µF 80V 1210 X7R
	or Murata	GRM32ER72A225KA35	2.2µF	2.2µF 100V 1210 X7R
Output	Murata	GRM32DR71E106MA12	10µF	10µF 25V 1210 X7R

Table 5 — *Recommended input and output capacitor components*

Product	Load Current (A)	C_{IN}	C_{OUT}	C_{IN} Ripple Current (I_{RMS})	C_{OUT} Ripple Current (I_{RMS})	V_{IN} Ripple (mVpp)	V_{OUT} Ripple (mVpp)	Load Step (% Rating) (1A/µs)	Transient Deviation Excluding Ripple (mVpk)	V_{OUT} Recovery Time (µs)
PI3527	18	10 x 2.2µF	8 x 10µF	10.1	11	700	210	50 – 100	260	<80

Table 6 — *Recommended input and output capacitor quantity and performance at nominal line, nominal trim.*

Layout Guidelines

To optimize maximum efficiency and low noise performance from a PI3527-65 design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 40. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

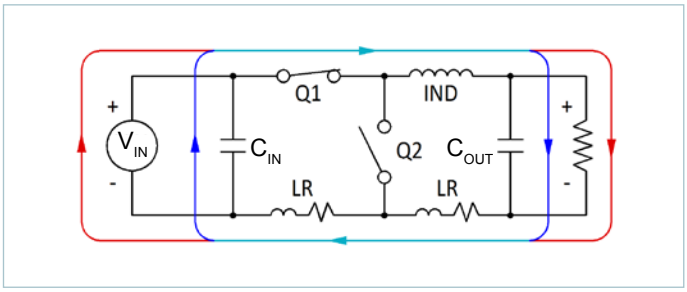


Figure 40 — *Typical Buck Regulator*

The path between the C_{OUT} and C_{IN} capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on. Figure 41, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI3527-65 performance.

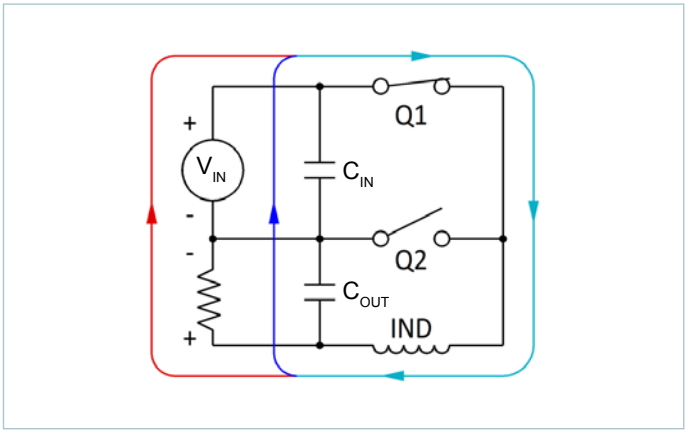


Figure 41 — *Current flow: Q1 closed*

When Q1 is on and Q2 is off, the majority of C_{IN}'s current is used to satisfy the output load and to recharge the C_{OUT} capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the C_{OUT} capacitor as shown in Figure 42. During this period C_{IN} is also being recharged by the V_{IN}. Minimizing C_{IN} loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the C_{IN} loop and C_{OUT} loop is vital to minimize switching and GND noise.

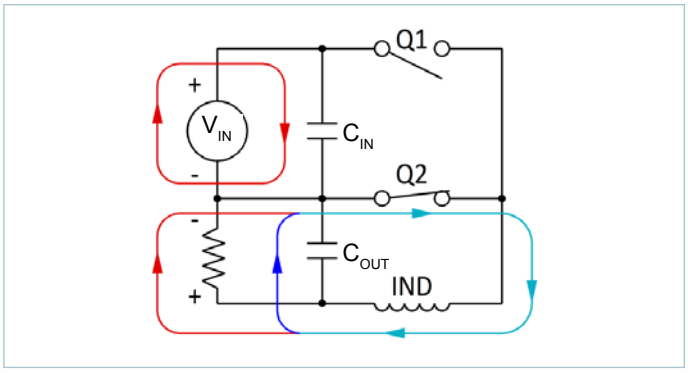


Figure 42 — *Current flow: Q2 closed*

Figure 43 illustrates the tight path between C_{IN} and C_{OUT} (and V_{IN} and V_{OUT}) for the high AC return current. The PI3527-65 evaluation board uses a layout optimized for performance in this way.

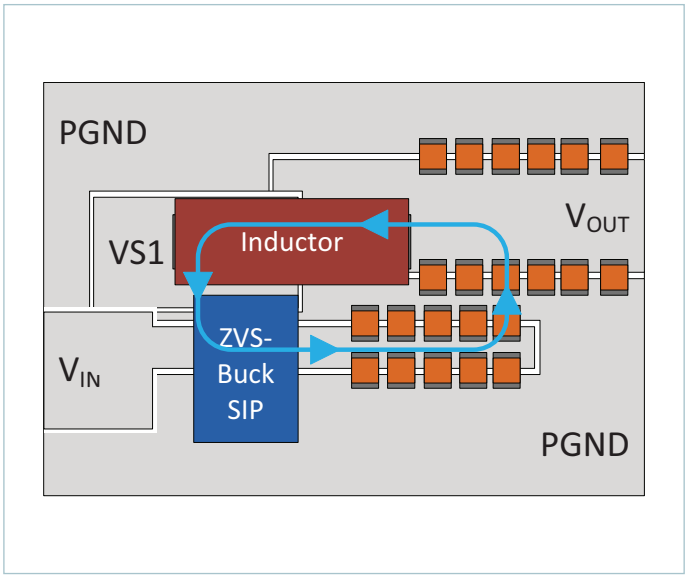
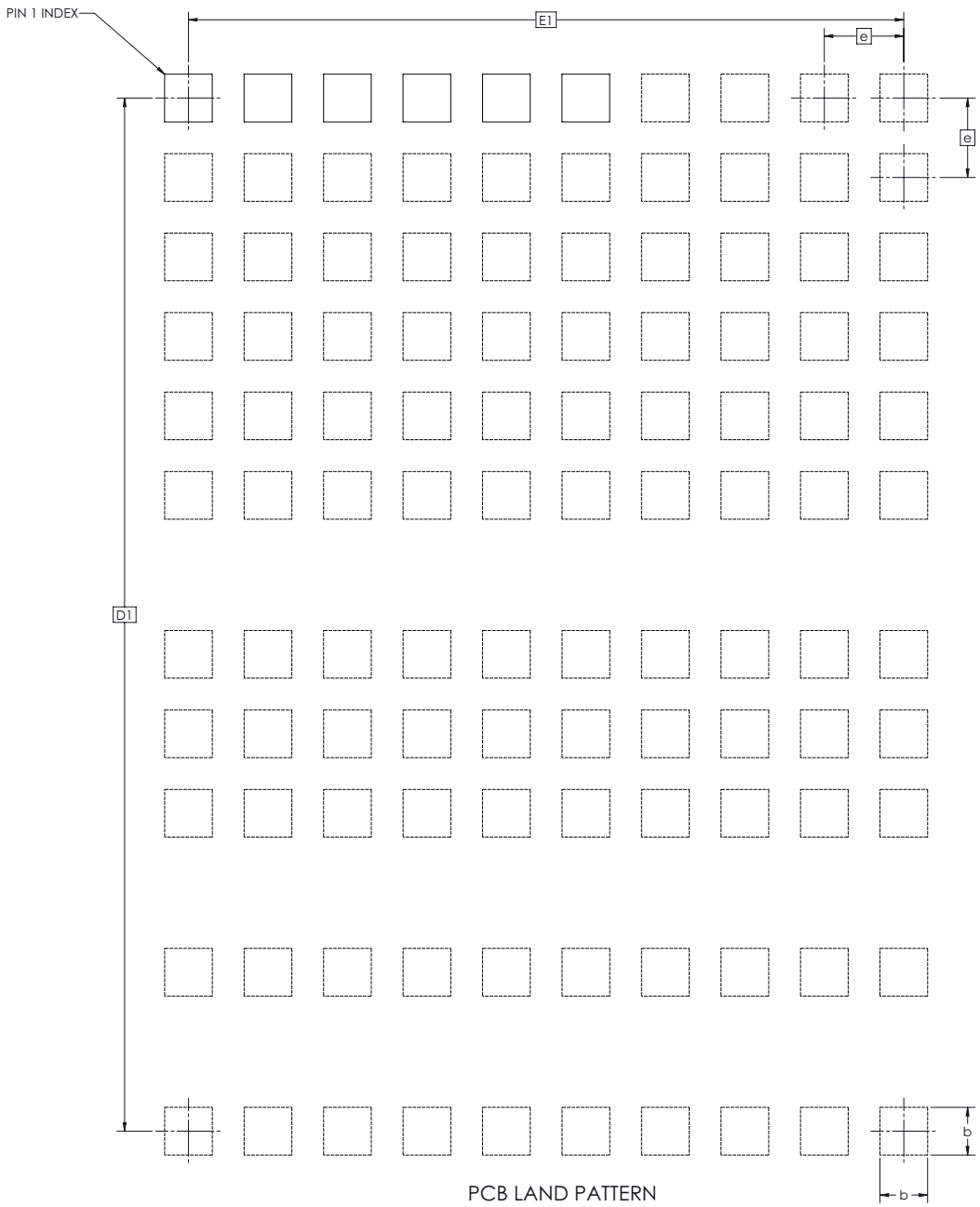


Figure 43 — *Recommended layout for Optimized AC Current within the SiP, Inductor, and Ceramic Input and Output Capacitors*

Recommended PCB Footprint and Stencil

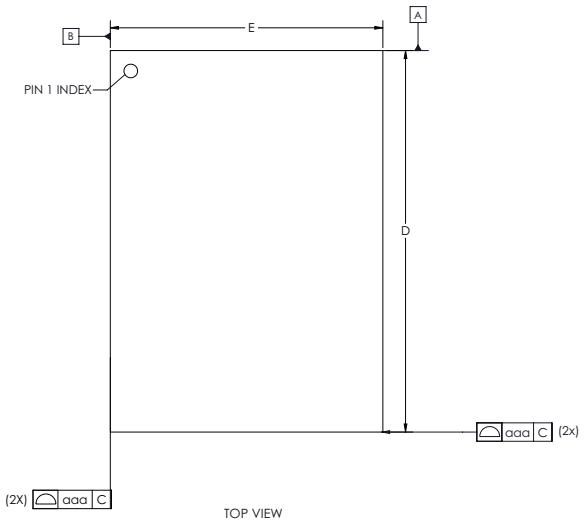


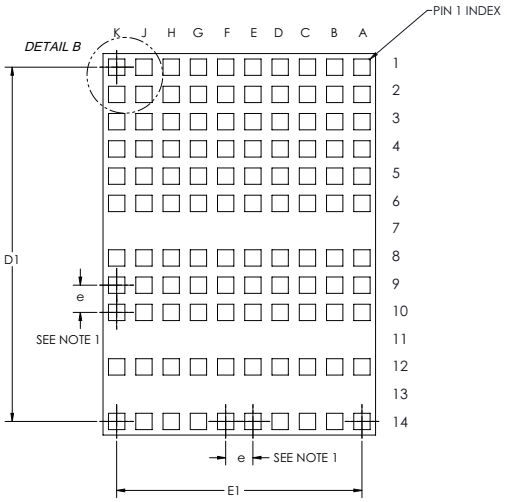
PCB LAND PATTERN
PI332x & PI352x

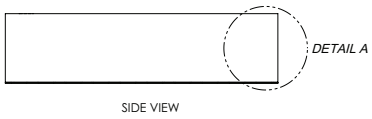
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
b	0.50	0.55	0.60
D1		13.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	

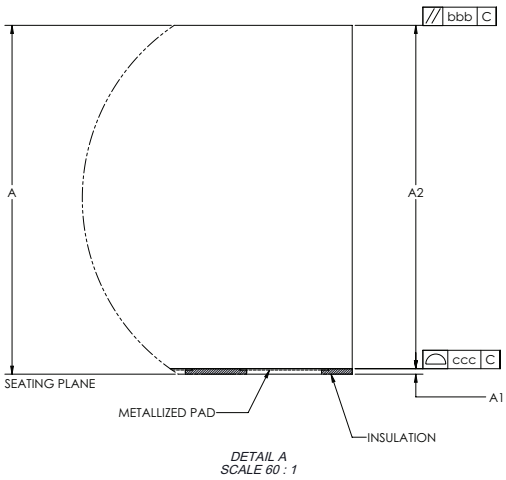
Recommended receiving footprint for PI3527-65 10mm x 14mm package. All pads should have a final copper size of 0.55mm x 0.55mm, whether they are solder-mask defined or copper defined, on a 1mm x 1mm grid. All stencil openings are 0.45mm when using either a 5mil or 6mil stencil.

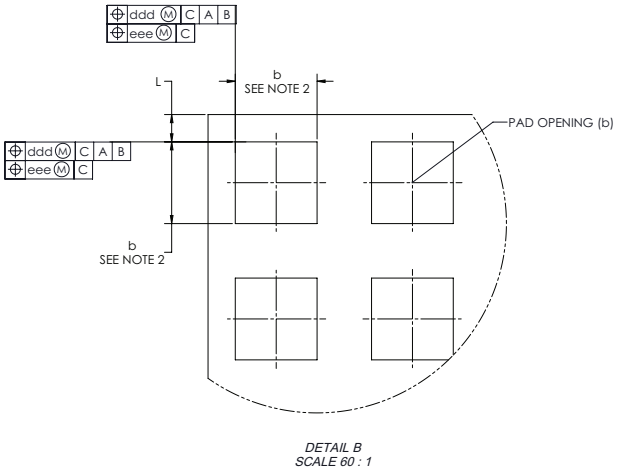
Package Drawings











PI332x			
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	2.49	2.56	2.63
A1	--	--	0.04
A2	--	--	2.59
b	0.50	0.55	0.60
D		14.00 BSC	
E		10.00 BSC	
D1		13.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	
L	0.175	0.225	0.275

PI332x	
DIMENSIONAL REFERENCES	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.10
bbb	0.10
ccc	0.08
ddd	0.10
eee	0.08

NOTES:
1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE
4. EXPOSED METALLIZED PADS ARE Cu PADS WITH SURFACE FINISH PROTECTION.
5. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
6. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.

Revision History

Revision	Date	Description	Page Number(s)
1.0	10/23/17	Initial release	n/a
1.1	08/11/20	Updated terminology	22

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