End of Life

ZVS Regulators

PI3302-00-BGIZ

8 – 36V_{IN} ZVS Buck Regulator

Product Description

The PI3302-00 is a high efficiency, wide input range DC-DC ZVS-Buck regulator integrating controller, power switches, and support components all within a high density System-in-Package (SiP). The integration of a high performance Zero-Voltage Switching (ZVS) topology increases point of load performance providing best in class power efficiency. The PI3302-00 requires only an external inductor and minimal capacitors to form a complete DC-DC switching mode Buck Regulator.

Device	Output Voltage		I_{OUT} Max
	Set	Range	
PI3302-00	5.0V	3.3 to 6.5V	10A

The ZVS architecture also enables high frequency operation while minimizing switching losses and maximizing efficiency. The high switching frequency operation reduces the size of the external filtering components, improves power density, and enables very fast dynamic response to line and load transients. The PI3302-00 sustains high switching frequency all the way up to the rated input voltage without sacrificing efficiency and, with its 20ns minimum on-time, supports large step down conversions up to 36V_{IN}.

Features & Benefits

- High Efficiency ZVS-Buck Topology
- Wide input voltage range of 8V to 36V
- Very-Fast transient response
- High accuracy pre-trimmed output voltage
- User adjustable soft-start & tracking
- Power-up into pre-biased load (select versions)
- Parallel capable with single wire current sharing
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- –40 to 125°C operating range (T_J)

Applications

- High-efficiency systems
- High-voltage battery operation

Package Information

- 10.5 x 14.5 x 2.6mm BGA SiP

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Order Information

Part Number	Output Range		I_{OUT} Max	Package	Transport Media
	Set	Range			
PI3302-00-BGIZ	5.0V	3.3 – 6.5V	10A	10.5mm x 14.5mm BGA	TRAY

Absolute Maximum Ratings [a]

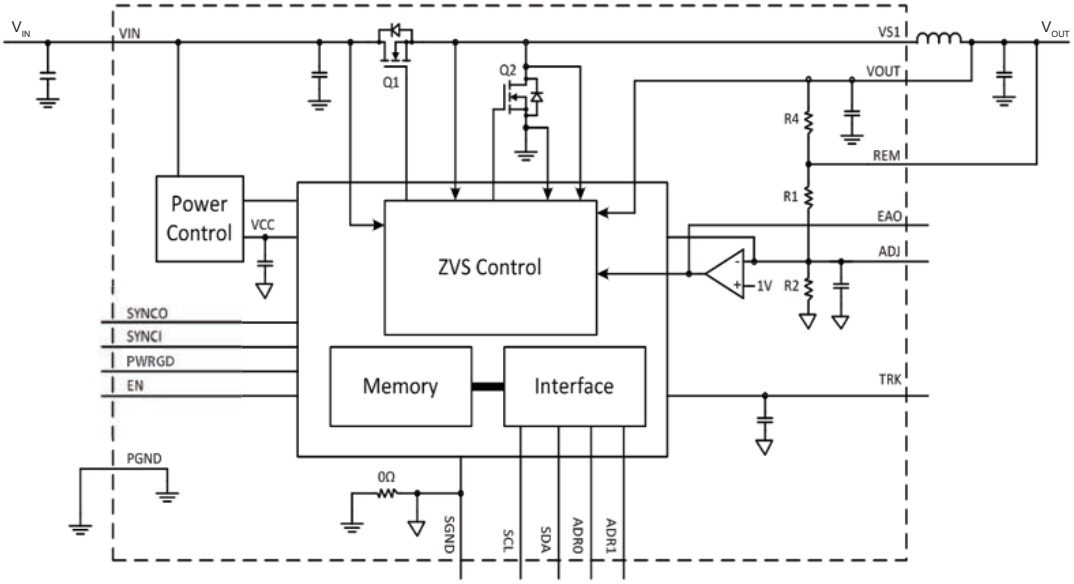
Name	Rating
VIN	–0.7 to 36V
VS1	–0.7 to 36V_{DC}, –11V for ≤5ns operating [b]. [c]
SGND	100mA
PWRGD, SYNCO, SYNCI, EN, EAO, ADJ, TRK, ADR1, ADR2, SCL, SDA	–0.3 to 5.5V / 5mA
VOUT, REM	–1.5 to 21V
Storage Temperature	–65 to 150°C
Operating Junction Temperature	–40 to 125°C
Soldering Temperature for 20 seconds	245°C
ESD Rating	2kV HBM

[a] At 25°C ambient temperature. Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted. Test conditions are per the specifications within the individual product electrical characteristics.

[b] Operating is defined as steady state 10A load with recommended 200nH inductor ±10% when measured with 50Ω, 7.5GHz transmission line probe LeCroy PP066 or equivalent.

[c] Transient peak operating conditions occurring for less than 1ms such as power cycling, short circuit and overload are guaranteed by design.

Functional Block Diagram

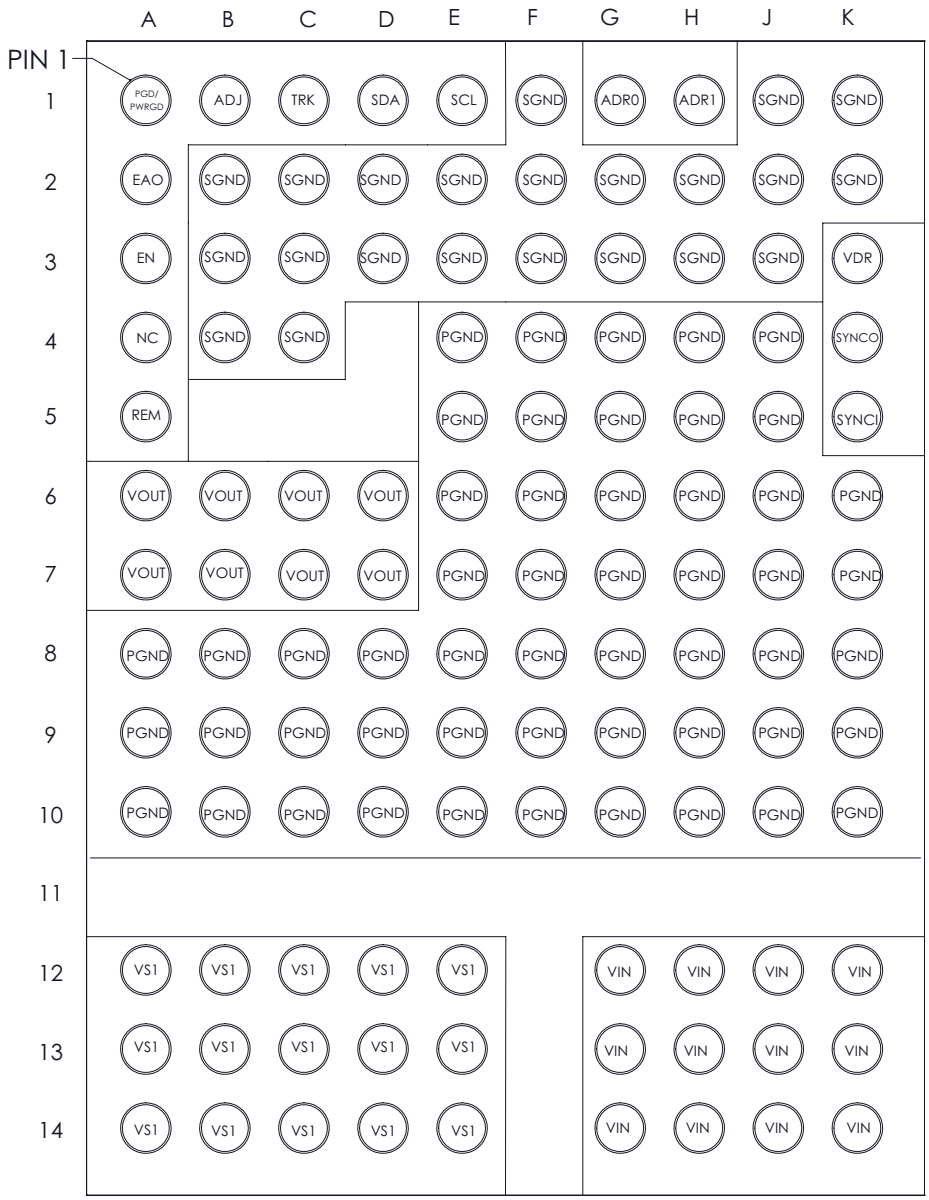


Simplified block diagram

Pin Description

Pin Name	Number	Description
SGND	Block 1	**Signal Ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO and ADJ communication returns. SGND and PGND are star connected within the regulator package.
PGND	Block 2	**Power Ground:** V_{IN} and V_{OUT} power returns.
VIN	Block 3	**Input Voltage:** and sense for UVLO, OVLO and feed forward ramp.
VOUT	Block 5	**Output Voltage:** and sense for power switches and feed-forward ramp.
VS1	Block 4	**Switching Node**: and ZVS sense for power switches.
PWRGD	A1	**Power Good:** High impedance when regulator is operating and V_{OUT} is in regulation. Otherwise pulls to SGND. Also can be used for parallel timing management intended for lead regulator.
EAO	A2	**Error Amp Output:** External connection for additional compensation and current sharing.
EN	A3	**Enable Input:** Regulator enable control. Asserted high or left floating – regulator enabled; Asserted low, regulator output disabled.
REM	A5	**Remote Sense:** High side connection. Connect to output regulation point.
ADJ	B1	**Adjust Input:** An external resistor may be connected between ADJ pin and SGND or VOUT to trim the output voltage up or down.
TRK	C1	**Soft-start and Track Input:** An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft-start.
NC	A4	**No Connect:** Leave pins floating.
VDR	K3	VDR can only be used for ADR0 and ADR1 pull up reference voltage. No other external loading is permitted
SYNCO	K4	**Synchronization Output:** Outputs a low signal for ½ of the minimum period for synchronization of other converters.
SYNCI	K5	**Synchronization Input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use.
SDA	D1	**Data Line:** Connect to SGND.
SCL	E1	**Clock Line:** Connect to SGND.
ADR1	H1	**Tri-state Address:** No connect.
ADR0	G1	**Tri-state Address:** No connect.

Package Pinout



10.5 x 14.5mm SiP
TOP VIEW THROUGH THE PRODUCT

Pin Block Name	Group of pins
SGND	B2-4, C2-4, D2-3, E2-3, F1-3, G2-3, H2-3, J1-3, K1-2
PGND	A8-10, B8-10, C8-10, D8-10, E4-10, F4-10, G4-10, H4-10, J4-10, K6-10
VIN	G12-14, H12-14, J12-14, K12-14
VS1	A12-14, B12-14, C12-14, D12-14, E12-14
VOUT	A6-7, B6-7, C6-7, D6-7

PI3302-00-BGIZ ($5.0V_{OUT}$) Electrical Characteristics

Unless otherwise specified: –40°C < T_J < 125°C, V_{IN} = 24V, L1 = 200nH [d]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}	[k]	8	24	36	V
Input Current	I_{IN_DC}	V_{IN} = 24V, T_C = 25°C, I_{OUT} = 10A		2.23		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	[e]			20	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		2.0		mA
		Enabled (no load)		2.5		mA
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	[e]	4.93	5.00	5.07	V
Output Voltage Trim Range	V_{OUT_DC}	[f] [k]	3.3		6.5	V
Line Regulation	ΔV_{OUT} (ΔV_{IN})	At 25°C, 8V < V_{IN} < 36V		0.10		%
Load Regulation	ΔV_{OUT} (ΔI_{OUT})	At 25°C, 0.5A < I_{OUT} < 10A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 5A, C_{OUT} = 4 x 47µF, 20MHz BW [g]		30		mV_{P-P}
Continuous Output Current Range	I_{OUT_DC}	[h] [k]			10	A
Current Limit	I_{OUT_CL}			12		A
Protection						
V_{IN} UVLO Start Threshold	V_{UVLO_START}		7.10	7.60	8.00	V
V_{IN} UVLO Stop Threshold	V_{UVLO_STOP}		6.80	7.25	7.60	V
V_{IN} UVLO Hysteresis	V_{UVLO_HYS}			0.33		V
V_{IN} OVLO Start Threshold	V_{OVLO_START}		36.1			V
V_{IN} OVLO Stop Threshold	V_{OVLO_STOP}		37.0	38.4		V
V_{IN} OVLO Hysteresis	V_{OVLO_HYS}			0.77		V
V_{IN} UVLO/OVLO Response Time	t_f			500		ns
Output Overvoltage Protection	V_{OVP}	Above V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}		130	135	140	°C
Overtemperature Restart Hysteresis	T_{OTP_HYS}			30		°C

[d] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI3302-00 evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[e] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.
[f] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.
[g] Refer to Output Ripple plots.
[h] Refer to Load Current vs. Ambient Temperature curves.
[j] Refer to Switching Frequency vs. Load current curves.
[k] Minimum 5V between V_{IN} – V_{OUT} must be maintained or a minimum load of 1mA required.

PI3302-00-BGIZ ($5.0V_{OUT}$) Electrical Characteristics (Cont.)

Unless otherwise specified: –40°C < T_J < 125°C, V_{IN} = 24V, L1 = 200nH [d]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_S	[j]		1.0		MHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [f]	50		110	%
SYNCI Threshold	V_{SYNCI}			2.5		V
SYNCI Input Impedance	Z_{SYNCI}			100		kΩ
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}		0		1.04	V
TRK Max Output Voltage				1.2		V
TRK Disable Threshold	V_{TRK_OV}		20	40	60	mV
Charge Current (Soft – Start)	I_{TRK}		70	50	30	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		6.8		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0µF		2.2		ms
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (Floating)	V_{EN_PU}	With positive logic EN polarity		2		V
Enable Pull-Down Voltage (Floating)	V_{EN_PD}	With negative logic EN polarity		0		V
Source Current	I_{EN_SO}	With positive logic EN polarity		50		µA
Sink Current	I_{EN_SK}	With negative logic EN polarity		50		µA

[d] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI3302-00 evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[e] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.
[f] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.
[g] Refer to Output Ripple plots.
[h] Refer to Load Current vs. Ambient Temperature curves.
[j] Refer to Switching Frequency vs. Load current curves.
[k] Minimum 5V between V_{IN} – V_{OUT} must be maintained or a minimum load of 1mA required.

PI3302-00-BGIZ ($5.0V_{OUT}$) Electrical Characteristics (Cont.)

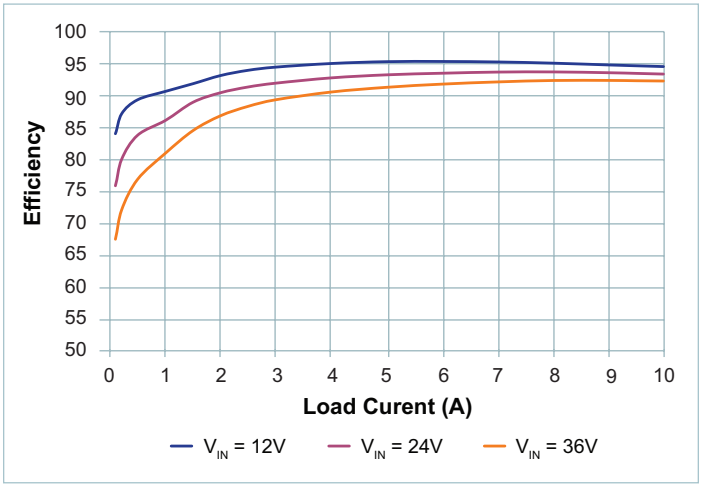


Figure 1 — *Efficiency at 25°C*

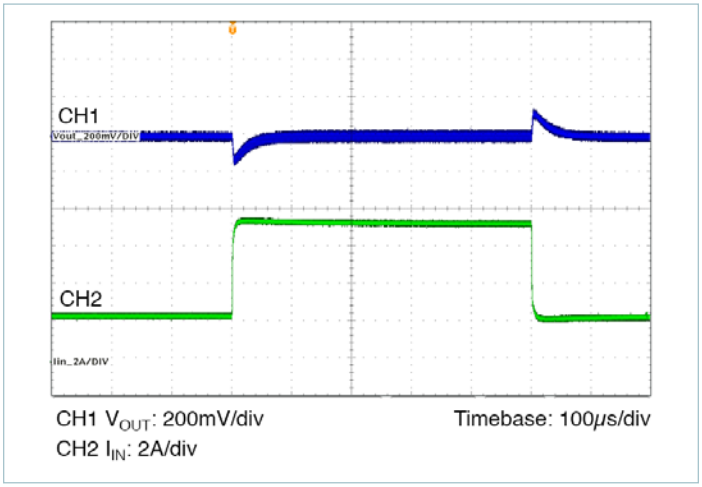


Figure 4 — *Transient response 2A to 7A, at 5A/µs*

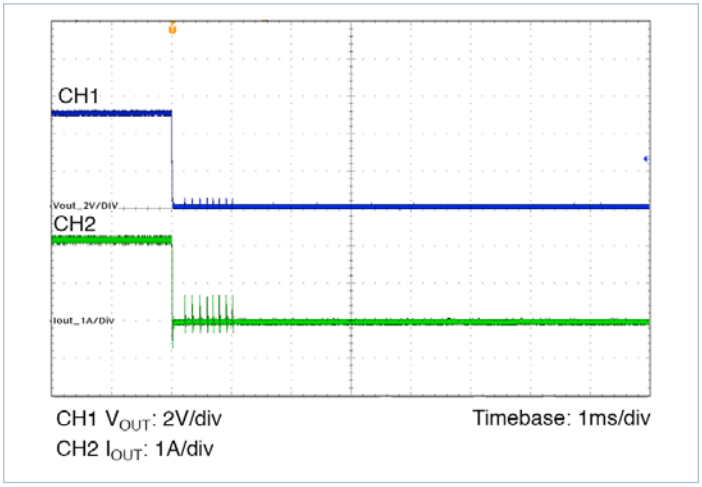


Figure 2 — *Short circuit test*

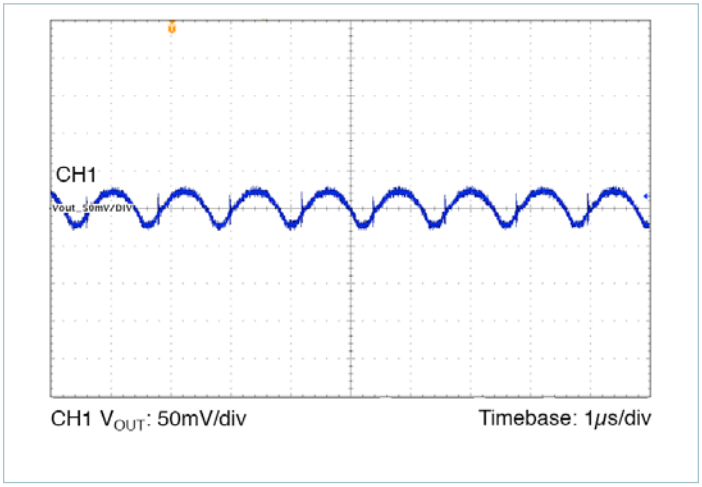


Figure 5 — *Output ripple $24V_{IN}$, $5.0V_{OUT}$ at 10A*

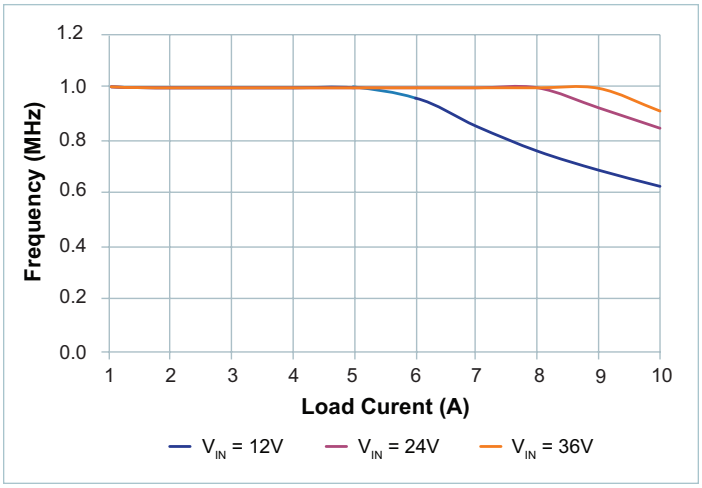


Figure 3 — *Switching frequency vs. load current*

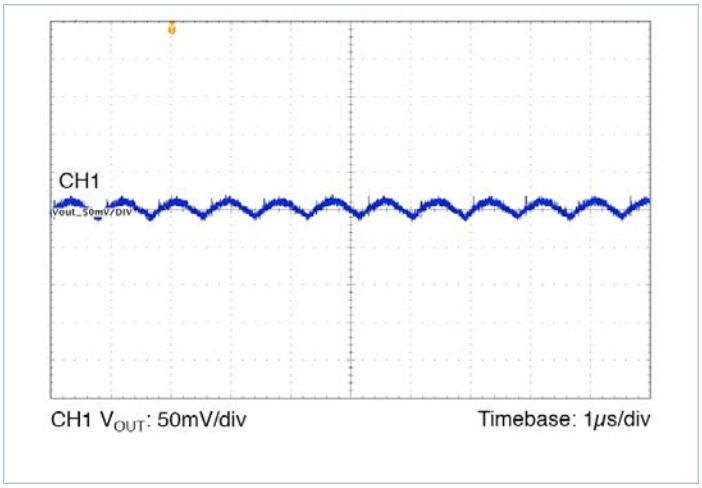


Figure 6 — *Output ripple $24V_{IN}$, $5.0V_{OUT}$ at 5A*

PI3302-00-BGIZ ($5.0V_{OUT}$) Electrical Characteristics (Cont.)

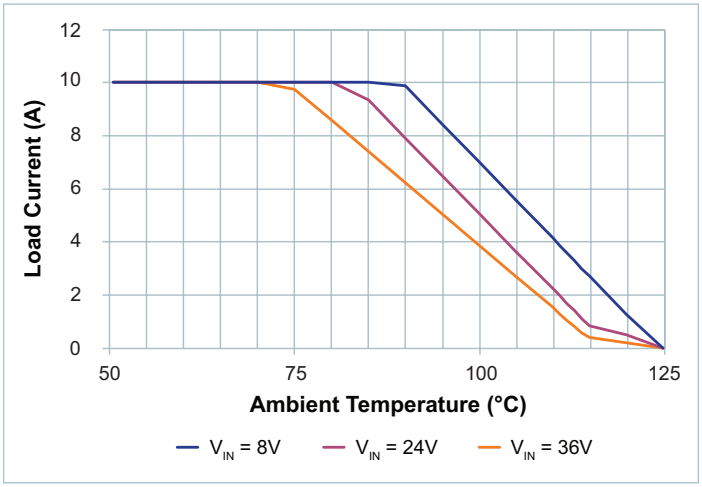


Figure 7 — *Load current vs. ambient temperature, 0LFM*

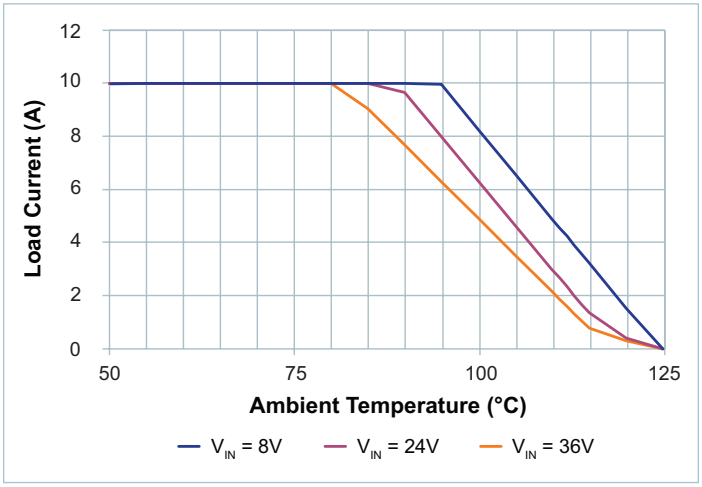


Figure 8 — *Load current vs. ambient temperature, 200LFM*

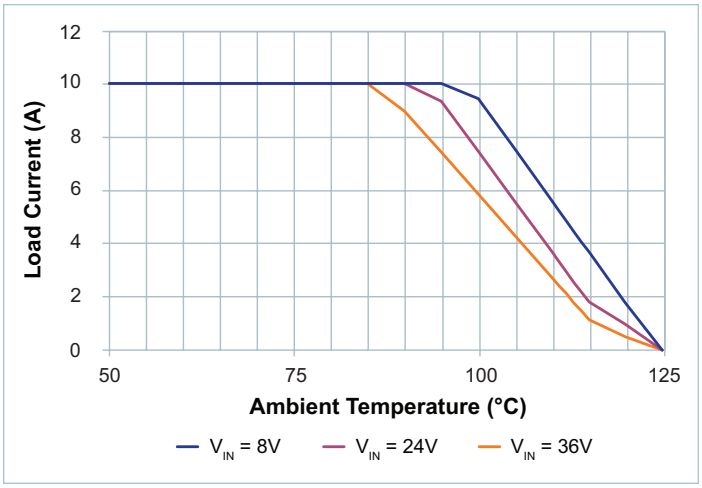


Figure 9 — *Load current vs. ambient temperature, 400LFM*

Functional Description

The PI3302-00 is a highly integrated ZVS buck regulator. The PI3302-00 has a set output voltage that is trimmable within a prescribed range shown in Table 1. Performance and maximum output current are characterized with a specific external power inductor (see Table 4).

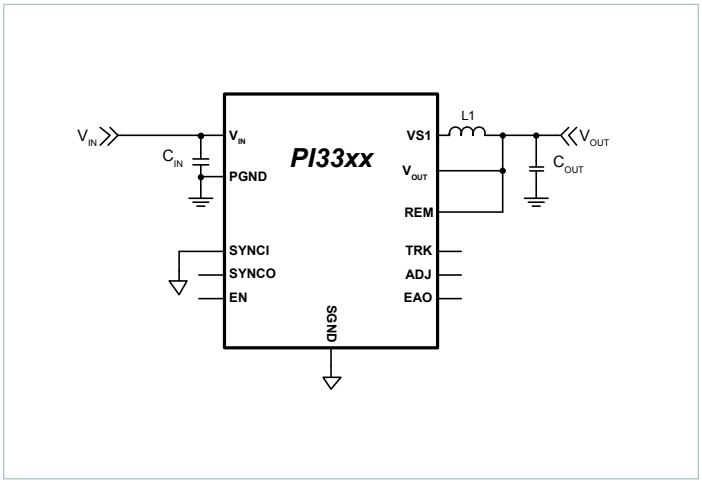


Figure 10 — *ZVS buck with required components*

For basic operation, Figure 10 shows the connections and components required. No additional design or settings are required.

ENABLE (EN)

EN is the enable pin of the converter. The EN Pin is referenced to SGND and permits the user to turn the regulator on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below $0.8V_{DC}$ with respect to SGND will disable the regulator output.

When the EN pin polarity is programmed for negative logic assertion; and if the EN pin is left floating, the regulator output is enabled. Pulling the EN pin above $1.0V_{DC}$ with respect to SGND, will disable the regulator output.

Remote Sensing

An internal 100Ω resistor is connected between REM pin and V_{OUT} pin to provide regulation when the REM connection is broken. Referring to Figure 10, it is important to note that L1 and C_{OUT} are the output filter and the local sense point for the power supply output. As such, the REM pin should be connected at C_{OUT} as the default local sense connection unless remote sensing to compensate additional distribution losses in the system. The REM pin should not be left floating.

Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency by an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency (f_S).

The PI3302-00 default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI3302-00 devices without the need for further user programming or external sync clock circuitry.

When using the internal oscillator, the SYNCO pin provides a 5V clock that can be used to sync other regulators. Therefore, one PI3302-00 can act as the lead regulator and have additional PI3302-00s running in parallel and interleaved.

Soft-Start

The PI3302-00 includes an internal soft-start capacitor to ramp the output voltage in 2ms from 0V to full output voltage. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, "Soft Start Adjustment and Track," in the Applications Description section for more details.

Output Voltage Trim

The PI3302-00 output voltage can be trimmed up from the preset output by connecting a resistor from ADJ pin to SGND and can be trimmed down by connecting a resistor from ADJ pin to VOUT. Table 1 defines the voltage range for PI3302-00.

Device	Output Voltage	
	Set	Range
PI3302-00-BGIZ	5.0V	3.3 – 6.5V

Table 1 — *PI3302-00-BGIZ output voltage range*

Output Current Limit Protection

PI3302-00 has two methods implemented to protect from output short or overcurrent condition.

Slow Current Limit protection: prevents the output load from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for 1024µs, a slow current limit fault is initiated and the regulator is shutdown which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: PI3302-00 monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current due to sudden low impedance short (50A Typical). If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching until Fault Restart Delay ends and then initiate a soft-start cycle.

Input Undervoltage Lockout

If V_{IN} falls below the input Undervoltage Lockout (UVLO) threshold, but remains high enough to power the internal bias supply, the PI3302-00 will complete the current cycle, stop switching, enter a low power state and initiate a fault. The system will restart once the input voltage is reestablished and after the Fault Restart Delay.

Input Overvoltage Lockout

If V_{IN} exceeds the input Overvoltage Lockout (OVLO) threshold (V_{OVLO}), while the controller is running, the PI3302-00 will complete the current cycle, stop switching, enter a low power state and set an OVLO fault. The system will resume operation when the input voltage falls below 98% of the OVLO threshold and after the Fault Restart Delay.

Output Overvoltage Protection

The PI3302-00 is equipped with output Overvoltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds 20% of its set regulated value, the regulator will complete the current cycle, stop switching and issue an OVP fault. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

Overtemperature Protection

The internal package temperature is monitored to prevent internal components from reaching their thermal maximum. If the Overtemperature Protection Threshold (OTP) is exceeded (T_{OTP}), the regulator will complete the current switching cycle, enter a low power mode, set a fault flag, and will soft-start when the internal temperature falls below Overtemperature Restart Hysteresis (T_{OTP_HYS}).

Pulse Skip Mode (PSM)

PI3302-00 features a PSM to achieve high efficiency at light loads. The regulators are setup to skip pulses if EAO falls below a PSM threshold. Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Skip Mode threshold.

Variable Frequency Operation

Each PI3302-00 is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 4), to operate at peak efficiency across line and load variations. At low line and high load applications, the base frequency will decrease to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

Parallel Operation

Paralleling modules can be used to increase the output current capability of a single power rail and reduce output voltage ripple.

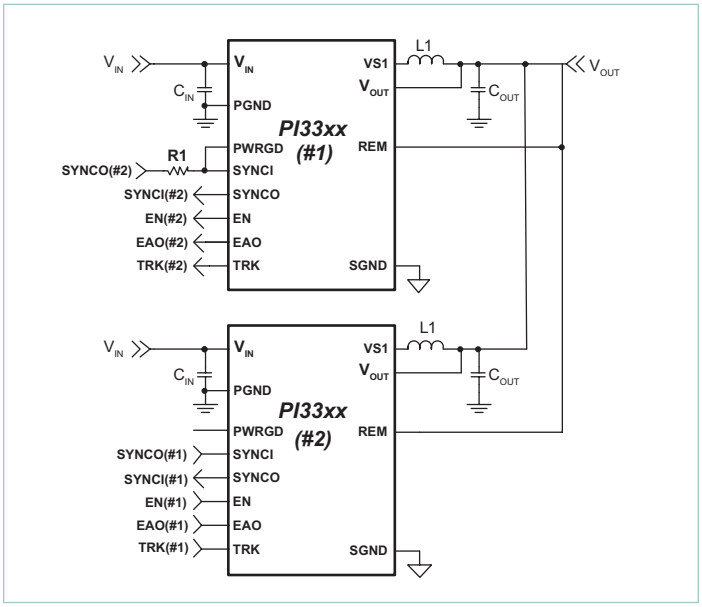


Figure 11 — *PI3302-00-BGIZ parallel operation*

The PI3302-00 default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI3302-00 devices without the need for further user programming or external sync clock circuitry.

By connecting the EAO pins and SGND pins of each module together the units will share the current equally. When the TRK pins of each unit are connected together, the units will track each other during soft-start and all unit EN pins have to be released to allow the units to start (See Figure 11). Also, any fault event in any regulator will disable the other regulators. The two regulators will be out of phase with each other reducing output ripple (refer to Switching Frequency Synchronization).

To provide synchronization between regulators over the entire operational frequency range, the Power Good (PWRGD) pin must be connected to the lead regulator's (#1) SYNCI pin and a 2.5kΩ Resistor, R1, must be placed between SYNCO (#2) return and the lead regulator's SYNCI (#1) pin, as shown in Figure 11. In this configuration, at system soft-start, the PWRGD pin pulls SYNCI low forcing the lead regulator to initialize the open-loop startup synchronization. Once the regulators reach regulation, SYNCI is released and the system is now synchronized in a closed-loop configuration which allows the system to adjust, on the fly, when any of the individual regulators begin to enter variable frequency mode in the loop.

Application Description

Output Voltage Trim

A post-package trim step is implemented to offset any resistor divider network errors ensuring maximum output accuracy. With a single resistor connected from the ADJ pin to SGND or REM, each device's output can be varied above or below the nominal set voltage.

Device	Output Voltage	
	Set	Range
PI3302-00-BGIZ	5.0V	3.3 – 6.5V

Table 2 — *PI3302-00 output voltage range*

The remote pin (REM) should always be connected to the V_{OUT} pin, if not used, to prevent an output voltage offset. Figure 12 shows the internal feedback voltage divider network.

R1, R2, and R4 are all internal 1.0% resistors and R_{HIGH} and R_{HIGH} are external resistors for which the designer can add to modify V_{OUT} to a desired output. The internal resistor value for each regulator is listed below in Table 3.

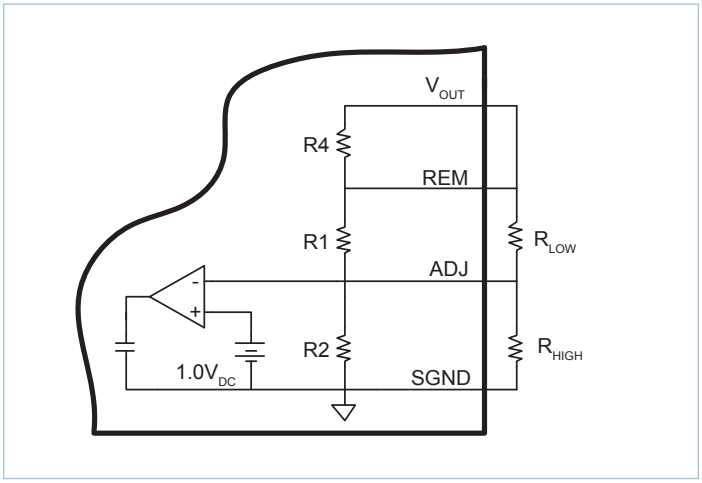


Figure 12 — *Internal resistor divider network*

Device	R1	R2	R4
PI3302-00-BGIZ	4.53kΩ	1.13kΩ	100Ω

Table 3 — *PI3302-00 internal divider values*

By choosing an output voltage value within the ranges stated in Table 2, V_{OUT} can simply be adjusted up or down by selecting the proper R_{HIGH} or R_{LOW} value, respectively. The following equations can be used to calculate R_{HIGH} and R_{LOW} values:

$$R_{HIGH} = \frac{1}{\left(\frac{V_{OUT} - 1}{R1}\right) - \left(\frac{1}{R2}\right)} \quad (1)$$

$$R_{LOW} = \frac{1}{\frac{1}{R2(V_{OUT} - 1)} - \left(\frac{1}{R1}\right)} \quad (2)$$

If, for example, a 4.0V output is needed, the user should choose the regulator with a trim range covering 4.0V from Table 2. For this example, the PI3302 is selected (5.0V set voltage). First step would be to use Equation 1 to calculate R_{HIGH} since the required output voltage is higher than the regulator set voltage. The resistor-divider network values for the PI3302 can be found in Table 3 and are R1 = 2.61kΩ and R2 = 1.13kΩ. Inserting these values in to Equation 1, R_{HIGH} is calculated as follows:

$$3.78k\Omega = \frac{1}{\left(\frac{4.0 - 1}{2.61k\Omega}\right) - \left(\frac{1}{1.13k\Omega}\right)} \quad (3)$$

Resistor R_{HIGH} should be connected as shown in Figure 12 to achieve the desired 4.0V regulator output. No external R_{LOW} resistor is need in this design example since the trim is above the regulator set voltage. The PI3302-00 output voltage can only be trimmed higher than the factory 1V setting.

Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal 100nF and a fixed charge current to provide a minimum startup time of 2ms (typical) for all PI3302-00 regulators. By adding an additional external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = (t_{TRK} \bullet I_{TRK}) - 100 \bullet 10^{-9} \quad (4)$$

Where t_{TRK} is the soft-start time and I_{TRK} is a 50µA internal charge current (see Electrical Characteristics for limits).

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at startup, simply connect all devices TRK pins together. This type of tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 13(a)).

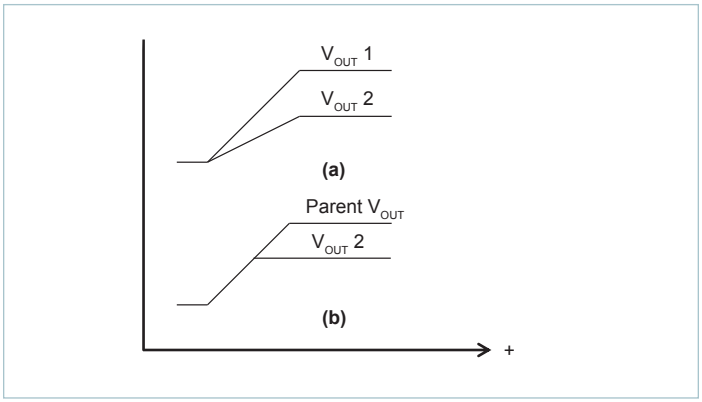


Figure 13 — *PI3302-00 tracking methods*

For Direct Tracking, choose the regulator with the highest output voltage as the parent and connect the parent to the TRK pin of the other regulators through a divider (Figure 14) with the same ratio as the child's feedback divider (see Table 3 for values).

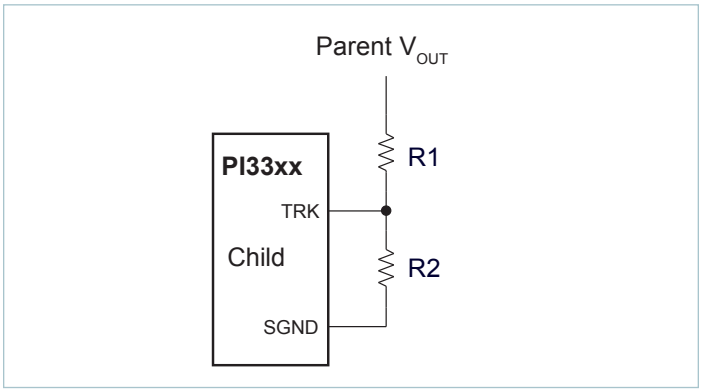


Figure 14 — *Voltage divider connections for direct tracking*

All connected regulators' soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 13(b). All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI3302-00 utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 4 details the specific inductor value and part number utilized for each PI3302-00 device which are available from Coiltronics and Eaton. Data sheets are available at:

http://www.cooperindustries.com

Device	Inductor [nH]	Inductor Part Number	Manufacturer
PI3302-00-BGIZ	200	FPT705-200-R	Coiltronics

Table 4 — *PI3302-00 inductor pairing*

Thermal De-Rating

Thermal de-rating curves are provided that are based on component temperature changes versus load current, input voltage and air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire system and are inclusive to both the PI3302-00 regulator and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions.

Thermal measurements were made using a standard PI3302-00 Evaluation board which is 3 x 4 inches in area and uses 4-layer, 2oz copper. Thermal measurements were made on the three main power devices, the two internal MOSFETs and the external inductor, with air flows of 0, 200, and 400LFM.

Filter Considerations

The PI3302-00 requires input bulk storage capacitance as well as low impedance ceramic X5R input capacitors to ensure proper start up and high frequency decoupling for the power stage. The PI3302-00 will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET is conducting. During the time the high side MOSFET is off, they are replenished from the bulk capacitor. If the input impedance is high at the switching frequency of the converter, the bulk capacitor must supply all of the average current into the converter, including replenishing the ceramic capacitors. This value has been chosen to be 100µF so that the PI3302-00 can start up into a full resistive load and supply the output capacitive load with the default minimum soft start capacitor when the input source impedance is 50Ω at 1MHz. The ESR for this capacitor should be approximately 20mΩ. The RMS ripple current in this capacitor is small, so it should not be a concern if the input recommended ceramic capacitors are used. Table 5 shows the recommended input and output capacitors to be used for the various models as well as expected transient response, RMS ripple currents per capacitor, and input and output ripple voltages. Table 6 includes the recommended input and output ceramic capacitors.

Device	V_{IN} (V)	I_{LOAD} (A)	C_{INPUT} Ceramic X5R	C_{INPUT} Bulk Elec.	C_{OUTPUT} Ceramic X5R	C_{INPUT} Ripple Current (I_{RMS})	C_{OUTPUT} Ripple Current (I_{RMS})	Input Ripple (mVpp)	Output Ripple (mVpp)	Output Ripple (mVpp)	Recovery Time (µs)	Load Step (A) (Slew/µs)
PI3302	24	10	4 x 4.7µF	100µF 50V	4 X 47µF 2 X 1µF 1 X 0.1µF	1.2	1.5	220	50	±170	30	5 (5A/µs)
		5						140	30			

Table 5 — *Recommended input and output capacitance*

Murata Part Number	Description
GRM188R71C105KA12D	1µF 16V 0603 X7R
GRM319R71H104KA01D	0.1µF 50V 1206 X7R
GRM31CR71H475KA12K	4.7µF 50V 1206 X7R
GRM31CR61A476ME15L	47µF 10V 1206 X5R

Table 6 — *Capacitor manufacturer part numbers*

Layout Guidelines

To optimize maximum efficiency and low noise performance from a PI3302-00 design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 15. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

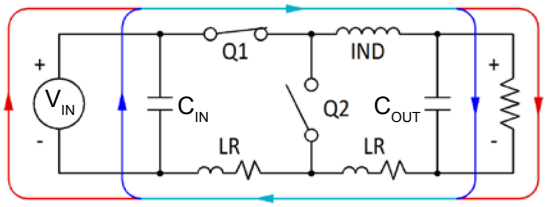


Figure 15 — *Typical buck converter*

The path between the C_{OUT} and C_{IN} capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on.

Figure 16, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI3302-00 performance.

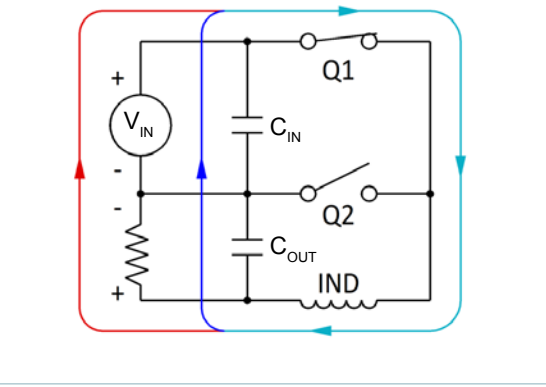


Figure 16 — *Current flow: Q1 closed*

When Q1 is on and Q2 is off, the majority of $C_{IN's}$ current is used to satisfy the output load and to recharge the C_{OUT} capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the C_{OUT} capacitor as shown in Figure 17. During this period C_{IN} is also being recharged by the V_{IN}. Minimizing C_{IN} loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the C_{IN} loop and C_{OUT} loop is vital to minimize switching and GND noise.

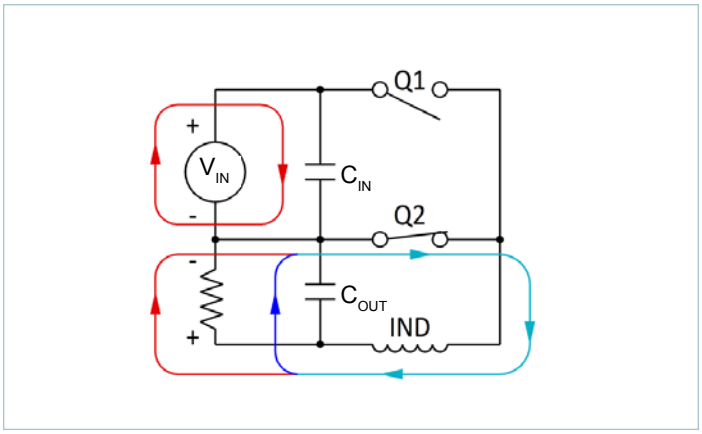


Figure 17 — *Current flow: Q2 closed*

The recommended component placement, shown in Figure 18, illustrates the tight path between C_{IN} and C_{OUT} (and V_{IN} and V_{OUT}) for the high AC return current. This optimized layout is used on the PI3302-00 evaluation board.

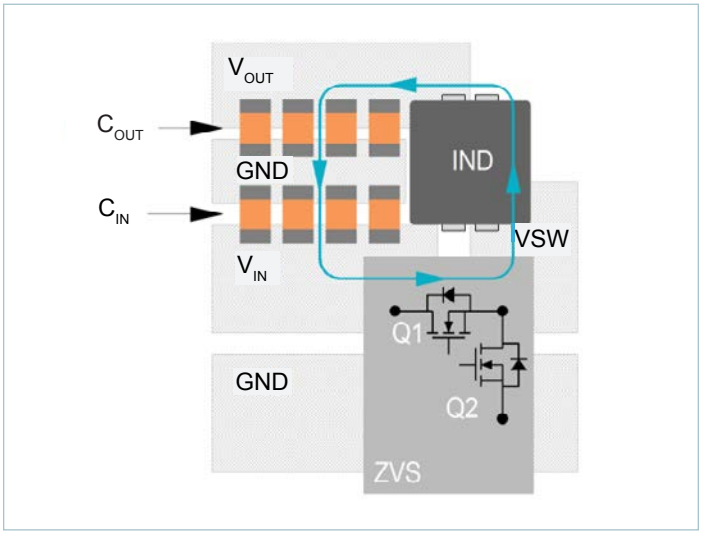
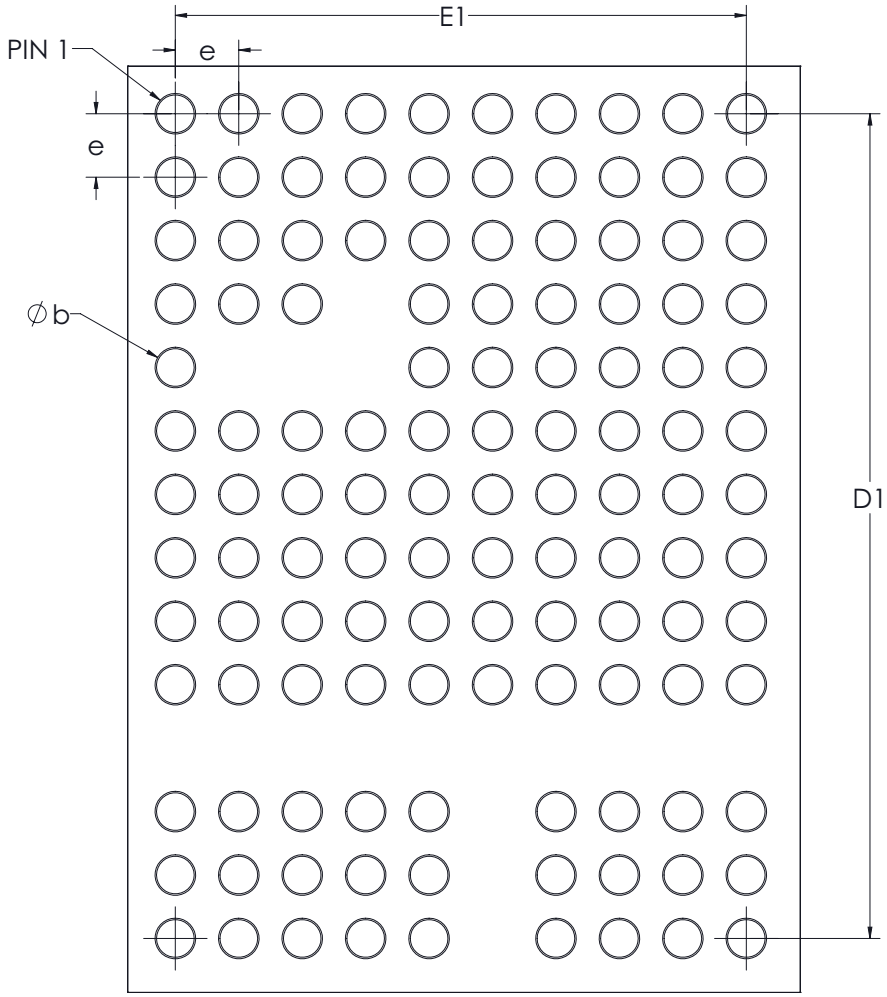


Figure 18 — *Recommended component placement and metal routing*

Recommended PCB Footprint and Stencil

PI33xx ZVS Buck Regulator
(Reference DWG # 50578 Rev #2)

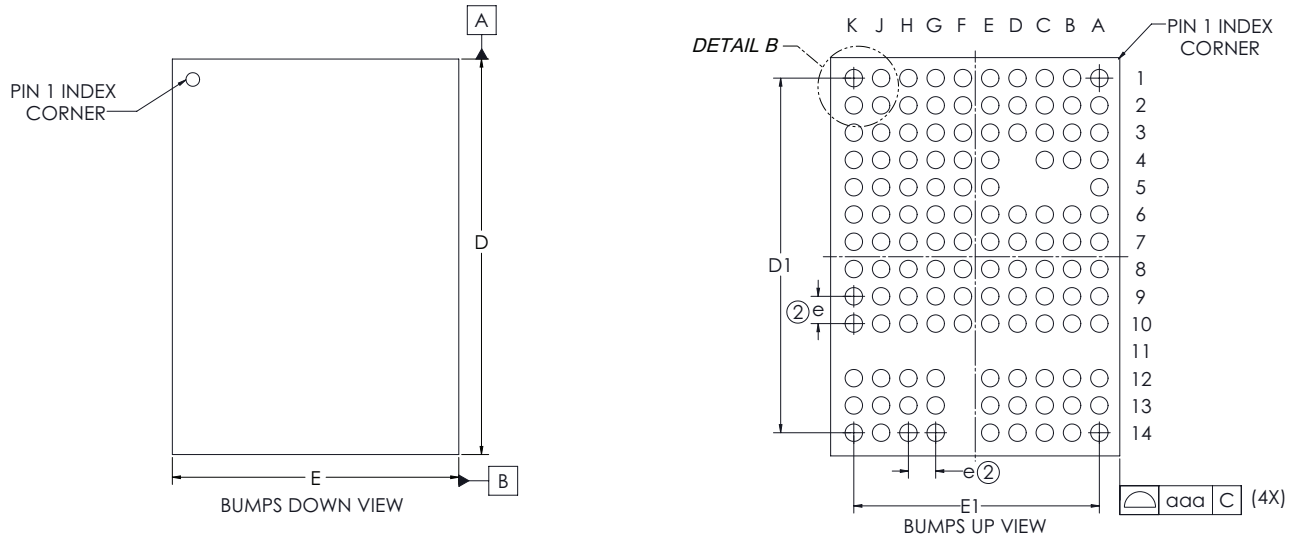


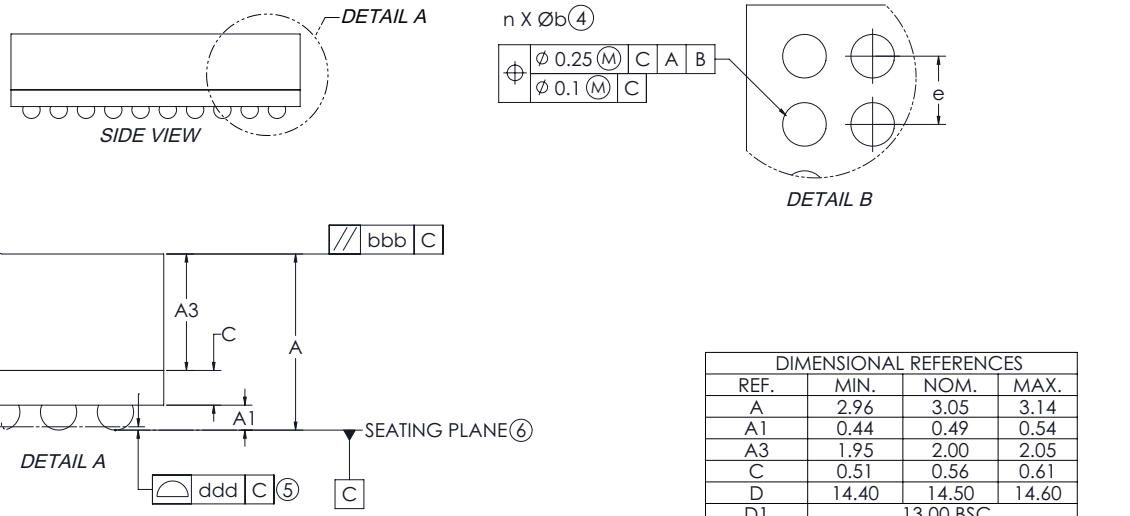
FOR PCB LAND PATTERN
10.5x14.5mm SiP

DIMENSIONSAL REFERENCES			
REF.	MIN.	NOM.	MAX.
b	0.59	0.64	0.69
D1	13.00 BSC.		
E1	9.00 BSC.		
e	1.00 BSC.		

Package Drawing

PI33xx ZVS Buck Regulator
(Reference DWG # 50578 Rev #2)





DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	2.96	3.05	3.14
A1	0.44	0.49	0.54
A3	1.95	2.00	2.05
C	0.51	0.56	0.61
D	14.40	14.50	14.60
D1		13.00 BSC	
E	10.40	10.50	10.60
E1		9.00 BSC	
b	0.59	0.64	0.69
aaa		0.20	
bbb		0.25	
ddd		0.15	
e		1.00 BSC	
MD/ME		14/10	
n		123	

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
② 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE.
AND SYMBOL 'n' IS THE NUMBER OF BALLS AFTER DEPOPULATING.
④ 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER AFTER REFLOW PARALLEL TO PRIMARY DATUM Ⓒ .
⑤ DIMENSION 'ddd' IS MEASURED PARALLEL TO PRIMARY DATUM Ⓒ .
⑥ PRIMARY DATUM Ⓒ AND SEATING PLANE ARE DEFINED BY THE SPERICAL CROWNS OF THE SOLDER BALLS.
7. THE OVERALL PACKAGE THICKNESS "A" ALREADY CONSIDERS COLLAPSE BALLS
8. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
9. REFERENCE TO JEDEC MO-234B.
10. RoHS COMPLIANT PER CST-0001 LATEST REVISION.

Revision History

Revision	Date	Description	Page Number(s)
1.0	05/17/17	Initial release as standalone data sheet	n/a
1.1	10/20/20	Updated terminology	13
1.2	02/05/21	Changed notes from numeric to alpha Updated format of pinout, land and mechanical outline	all 6, 16 – 18

Note 1: PI3302-00-BGIZ part was initially released on 01/06/16. See family data sheet PI33xx-x0, revisions 1.9 – 2.5 for previous iterations of the data for this part number.
Note 2: Page added in Rev 1.2.

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