DCM™
Design Guide

VICOR

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As a part of the modular power system design methodology and to provide a great flexibility to the power system designers to achieve high-performance, cost-effective design of power distribution systems, Vicor introduced the family of DC-DC converter modules (DCM) in a ChiP package (Converter housed in a Package), shown in Figure 1.1. ChiP platform products use advanced magnetic structures that are integrated within high-density interconnect (HDI) substrates, together with power semiconductors, control ASICs and a microcontroller to provide superior electrical and thermal performance.

The DCMs can be used in various applications related to Commercial, Industrial and Military grades. A few examples of Commercial / Industrial-grade applications where DCMs best fit in are battery charging, LED lighting and medical devices. Also, applications such as data centers and telecommunications that require huge amounts of power can implement distributed power architecture using DCMs. This can improve the overall power system efficiency and lower the system and operational costs.

DCMs are well suited in Military grade applications such as ground based vehicular systems, targeting systems, flat panel displays, RF Jammers and airborne applications that require higher power levels and high reliability with size, weight and cost as an additional constraints.

One must be aware of the technical considerations when implementing a high-performance converter into the design of a power system. Therefore, this design guide is intended to provide power system designers with detailed insight to best use ChiP DCMs in a DC distribution power system.

Introduction to DC-DC converter Module (DCM)

The DCM encapsulates isolation, regulation, thermal management and fault monitoring in a single module. The DCM operates on a high-frequency, double-clamped zero voltage switching (DC-ZVS) topology. As a result of high-frequency operation, the size of the magnetics and energy storage elements are reduced. In turn, a revolutionary increase in density is achieved, with the power density up to 1244W/in^3. As a result of double-clamped zero voltage switching (DC-ZVS) topology, high efficiency is achieved with efficiencies of up to 93% compared to other DC-DC converter solutions.

The DCM can operate from an unregulated, wide-range input voltage to provide an isolated and regulated output voltage with regulation of up to ±1%. These are available in various regulated output voltages in the range of Safety Extra Low Voltage (SELV) from 3 – 53V. Specific details are described in the Figure 1.2. The DCM is capable of delivering high power levels of up to 600W in its standalone operation. In applications that call for more power than can be delivered by a single DCM, multiple DCMs can be used in parallel.

The DCMs are available in three package sizes with their respective specifications shown below:

- 2322 through-hole ChiP package
  - 0.978 x 0.898 x 0.284in [24.84 x 22.8 x 7.21mm]
  - Low input voltage range of 9 – 154V
  - Maximum power up to 120W
  - Input to output isolation of 3,000V_{DC} (2,121V_{RMS})
- 3623 through-hole ChiP package
  - 1.524 x 0.898 x 0.284in [38.72 x 22.8 x 7.21mm]
  - Low input voltage range of 9 – 154V
  - Maximum power up to 320W
  - Input to output isolation of 2,250V_{DC} (1,800V_{RMS})
  - Input to output isolation of 3,000V_{DC} (2,121V_{RMS})
    Note: Applicable only for 43 – 154V input voltage range products.
- 4623 through-hole ChiP package
  - 1.886 x 0.898 x 0.284in [47.91 x 22.8 x 7.21mm]
  - High input voltage range of 120 – 420V
  - Maximum power up to 600W
  - Input to output isolation of 4,242V_{DC} (3,000V_{RMS})

Figure 1.1 — *Through-hole ChiP DCM*

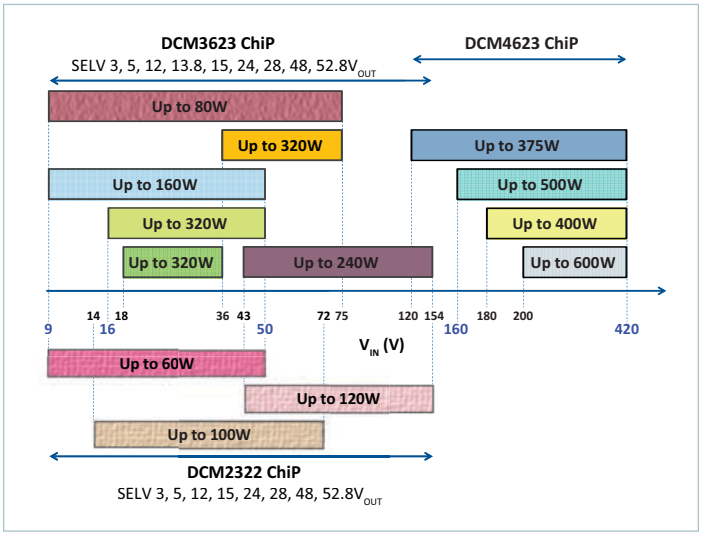


Figure 1.2 — *Electrical characteristics of DC-DC converter module (DCM), MIL-COTS range is shown in blue*

Apart from the previous electrical characteristics, other important features of the DCMs are:

- Droop share characteristics, which allows DCMs to be used in parallel operation for increasing power outputs without any requirement of external-control circuitry.
- Output voltage trimming typical trim range is –40% to +10% of the nominal output voltage.
- Fully operational current limit
- Enable / Disable control
- Various fault protections, it includes:
  - Input undervoltage lockout (V_{IN_UVLO})
  - Input overvoltage lockout (V_{IN_OVLO})
  - Overtemperature
  - Output overvoltage
  - Overcurrent
  - Short circuit

Useful Links

- DCM Family Page
- See individual product pages for accessories:
  - Heat sinks
  - U-shaped heat spreaders
- Environmental Qualification Test Reports
- Test data of the specific model with a specific serial number can be obtained from entering the model and serial number in the "Final Test Data" section of the Vicor Quality page.

DCMs use a thermally-adept ChiP packaging technology which provides flexible thermal management. The ChiP's top and bottom sides are molded with an optimized thermal compound material that has low thermal impedance. This allows the internally-generated heat to evenly distribute across the surfaces of the ChiP and also enhances thermal pathways to the smooth, flat ChiP exterior. The majority of the heat can be removed using single- or dual-sided cooling using heat sinks or coldplates with some heat transfer through the leads of the package.

To help power system designers to fully leverage the electrical and thermal performance characteristics of the ChiP DCMs, Vicor offers following online design tools:

- PowerBench™ Whiteboard*
- Product Simulators™
- DCM™ Trim Calculator

* Available on Internet Explorer and Chrome browsers only.

1. Source and Source Impedance

A. Consider source impedance L_{IN}, R_{IN} in total source impedance calculations, refer to the General Notes A.

2. Input Line Impedance

A. Take input line impedance L_D, R_D into consideration while calculating the total source impedance. Follow guidelines per General Notes A.

3. Decoupling Capacitor

A. Select an optimum value of decoupling capacitor to compensate for source impedance and input line impedance (Z_{SOURCE} point gives Thevenin's equivalent impedance looking back into the source and line).

B. $R_{ESR\_DECOUPLE}$ must be properly selected to provide optimum damping. The requirements of $R_{ESR\_DECOUPLE}$ can be satisfied by electing an Aluminum Electrolytic capacitor with an ESR value close to the desired value, this eliminates the need for an external damping resistor.

4. Safety

A. In case of failure of the DCM such as input short circuit, a fuse must be used to mitigate the risk of fire and board damage.

B. Select recommended fuse from the Safety Approvals section of the DCM product family page.

5. Differential Mode Input Filter

A. Switching converters are a source of the differential-mode noise; use a differential-mode filter network to attenuate differential-mode noise.

B. Select the cutoff frequency of the input filter much lower than the DCM crossover frequency (20kHz).

C. Input filter must be well damped to avoid ringing of the input voltage. The impedance of the input filter looking back into the input filtering network from Z_{OUT_FILTER} must be at least ten times lower than the input impedance of the DCM (Z_{IN_DCM}). Please refer to the filter design tool to analyze the filter response.

6. Slew Rate

A. Input voltage slew rate at the DCM input leads (+IN, –IN) must be less than 1V/µs.

7. Common-Mode Filter Network

A. Switching converters are a source of common-mode noise; to attenuate common-mode noise Y-capacitors (C_{Y3_6}) must be placed from +IN, –IN, +OUT, –OUT to earth/chassis ground.

B. Y-capacitors must be placed as close as possible to the input and output pins of the module.

C. Y-capacitor selection must meet application safety standards. Y2 sub-classification Y-capacitors are recommended with a typical capacitance value of 4700pF, with an appropriate peak voltage rating.

D. **Optional EMI Filter:** To meet EMI requirements or for better common-mode noise attenuation, use a common-mode choke T1 along with the Y-capacitors (C_{Y1_4}) on input of the DCM. Similar common-mode filtering network can be used on the output of the DCM to meet EMI requirements on the output side. See Common-Mode Input Filter Design considerations, page 36.

8. Output Capacitor

A. For control-loop stability, the output capacitor must be within the Min / Max range of C_{OUT_EXT} data sheet specifications, with a minimum $R_{ESR\_OUT\_EXT}$ of 10mΩ.

- The requirement of $R_{ESR\_OUT\_EXT}$ can be satisfied by selecting an aluminum electrolytic capacitor with an ESR of at least 10mΩ.

B. C_{OUT_EXT} must be placed physically near the output pins of the module.

C. While choosing the output capacitor, operating / environmental temperature must be taken into consideration.

9. Differential-Mode Output Filter (Optional)

A. To attenuate differential-mode noise generated by switching converter, use a differential-mode filter network.

B. Select the cutoff frequency of the output filter at least ten times lower than the switching frequency.

C. Output filter must be well damped to avoid ringing in the output voltage.

D. For high-frequency noise attenuation, use multiple low-ESR valued capacitors, such as ceramic capacitors, at C3.

10. Output Line Impedance

A. Load regulation degrades due to excessive output line impedance. For better regulation at the load, keep the output line impedance as low as possible or consult app note AN:035 "Achieving High Accuracy Voltage (or Current) Regulation with the DCM up to ±1% regulation."

11. Control Pin Circuitry

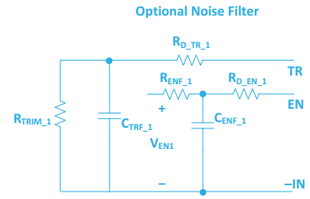
A. Circuit on control pins, TR, EN, FT, must be referenced directly to –IN at the module input pin using a Kelvin connection.

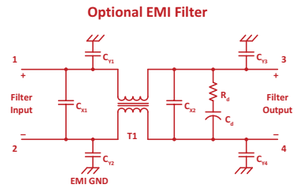
B. **Optional Noise Filter:** For protection from external noise the TR and EN pins may need an RCR filter network. $R_{D\_TR\_1}$, $R_{D\_EN\_1}$ are provided for attenuating noise caused by the external lead inductance.

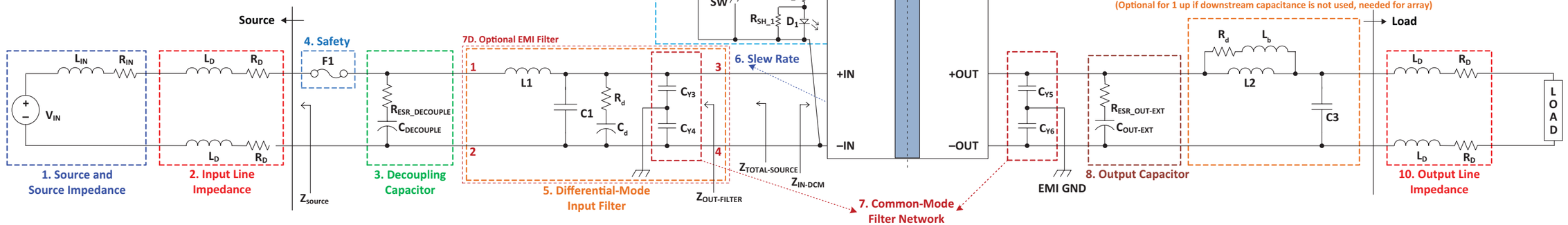
C. Please refer to the DCM Trim Calculator to find the R_{TRIM_1} value.

D. Minimum loading of R_{SH_1} = 50kΩ on FT pin is required for fault status indication. FT pin can provide a maximum current of 4mA, select a series resistor R_{SE_1} to limit the current.

E. If control / monitor functions are not required, signal pins can be left unconnected.







GENERAL NOTES:

A. Source Impedance and Its Effect on Stability

- Interaction between the total source impedance and input impedance of the DCM will cause stability issues. To avoid interactions, total impedance looking back into the source (Z_{TOTAL_SOURCE}) must be at least ten times lower than the input impedance of the DCM (Z_{IN_DCM}) over a frequency range of 0Hz to maximum control loop bandwidth:
  $Z_{TOTAL\_SOURCE} \le (Z_{IN\_DCM} / 10)$ for all F[0 : 20kHz].

B. Environmental Conditions

- Converters must be protected from environmental conditions such as moisture, dust, explosive or hazardous atmosphere. The DCM must be enclosed for safety during potentially higher operating temperature and voltage.
- Excessive heat, cold and thermal shock can cause damage of the ChiP.
- DCM should not be exposed to condensation.

C. Soldering the ChiP

- Follow the app note AN:031 "Through-Hole ChiP package soldering guidelines."
- Clean the PC board after the soldering process of the ChiP to remove the flux residues.

D. Thermal Management of the ChiP

- Heat can be removed from the ChiP top and bottom surfaces, as well as through the leads.
- For more information, refer to app note AN:039 "Thermal Management for VIA™ and ChiP Modules."

E. Mechanical Compressive Force of Heat Sinks

- Excessive z-axis compressive force on the ChiP will cause a shift in electrical parameters and mechanical deformation of the leads.
- Maximum compressive force on the ChiP must be kept below 20psi. For more information, consult app note AN:036 "Recommendations for Maximum Compressive Force of Heat Sinks."

F. Product Simulator

- Use the Product Simulator for conducting thermal, start-up, steady-state, V_{IN}-step and load-step simulations.

Note: Click any numbered heading on this page to jump to the related section of this Design Guide for more information.

Safety Considerations

Fusing

To provide flexibility in designing a power system, the DCM converter is not internally fused. To meet safety standards, specific fuse recommendations are provided in the agency certifications. Fusing provides protection in case of a system or component failure such as an input short circuit and it will help mitigate the risk or spread of fire and board damage.

Safety approvals should always be consulted for the latest fusing requirements. Please refer to the Safety Approvals section of the DCM product family page.

A fuse must also be used for applications that do not require agency certifications. When selecting a fuse for these applications, the following characteristics should be taken into consideration:

- Voltage rating
  - The device voltage rating should be greater than the maximum possible input voltage
- Current rating
  - The device current rating should be greater than the DCM converter's maximum input current
- Interrupting rating, very important for low-impedance sources
- Temperature de-rating
- Melting integral (I^2t)

Acceptable Fuse Types and Current Rating for the DCM ChiP Family of Converters

Input Voltage Range (Volts)	Output Voltage (Volts)	Output Power (Watts)	ChiP Model Number	Recommended Fuse
DCM2322				
30 (9 – 50)	12	60	DCM2322x50T1360y6z	Littelfuse 487 10A EATON ABC 10A
	15	60	DCM2322x50T1760y6z	
	24	60	DCM2322x50T2660y6z	
	28	60	DCM2322x50T3160y6z	
	48	60	DCM2322x50T5360y6z	
43 (14 – 72)	3.3	35	DCM2322x72S0435y6z	Littelfuse 487 8A EATON ABC 8A
	5	50	DCM2322x72S0650y6z	
	12	100	DCM2322x72S13A0y6z	Littelfuse 487 12.5A EATON ABC 12A
	15	100	DCM2322x72S17A0y6z	
	24	100	DCM2322x72S26A0y6z	
	28	100	DCM2322x72S31A0y6z	
	48	100	DCM2322x72S53A0y6z	
100 (43 – 154)	3.3	40	DCM2322xA5N0440y6z	EATON BK/PCE-5-R
	5	60	DCM2322xA5N0660y6z	
	12	120	DCM2322xA5N13A2y6z	
	15	120	DCM2322xA5N17A2y6z	
	24	120	DCM2322xA5N26A2y6z	
	28	120	DCM2322xA5N31A2y6z	
	48	120	DCM2322xA5N53A2y6z	
DCM3623				
30 (9 – 50)	3.3	80	DCM3623x50T0480yzz	Bussmann ABC-15-R Littelfuse 456 20A
	5	80	DCM3623x50T0680yzz	
	12	160	DCM3623x50T13A6yzz	Bussmann ABC-30-R Littelfuse 456 30A
	15	160	DCM3623x50T17A6yzz	
	24	160	DCM3623x50T26A6yzz	
	28	160	DCM3623x50T31A6yzz	
	48	160	DCM3623x50T53A6yzz	

Acceptable Fuse Types and Current Rating for the DCM ChiP Family of Converters (Cont.)				
Input Voltage Range (Volts)	**Output Voltage (Volts)**	**Output Power (Watts)**	**ChiP Model Number**	**Recommended Fuse**
DCM3623 (Cont.)				
24 (18 – 36)	5	180	DCM3623x36G06A8yzz	Bussmann ABC-15-R
	12	320	DCM3623x36G13C2yzz	Bussmann ABC-30-R
	15	320	DCM3623x36G17C2yzz	
	24	320	DCM3623x36G26C2yzz	
	28	320	DCM3623x36G31C2yzz	
	36	320	DCM3623x36G40C2yzz	
	48	320	DCM3623x36G53C2yzz	
42 (9 – 75)	12	80	DCM3623x75X1380yzz	Littelfuse 487 15A Bussmann ABC-15-R
	15	80	DCM3623x75X1780yzz	
	24	80	DCM3623x75X2680yzz	
	28	80	DCM3623x75X3180yzz	
	48	80	DCM3623x75X5380yzz	
28 (16 – 50)	3.3	120	DCM3623x50M04A2yzz	Bussmann ABC-12-R
	5	180	DCM3623x50M06A8yzz	Bussmann ABC-18-R
	12	320	DCM3623x50M13C2yzz	Bussmann ABC-30-R Littelfuse 456 30A
	15	320	DCM3623x50M17C2yzz	
	24	320	DCM3623x50M26C2yzz	
	28	320	DCM3623x50M31C2yzz	
	48	320	DCM3623x50M53C2yzz	
48 (36 – 75)	5	160	DCM3623x75H06A6yzz	Bussmann ABC-7-R
	12	320	DCM3623x75H13C2yzz	Bussmann ABC-15-R
	15	320	DCM3623x75H17C2yzz	
	24	320	DCM3623x75H26C2yzz	
	28	320	DCM3623x75H31C2yzz	
	36	320	DCM3623x75H40C2yzz	
	48	320	DCM3623x75H53C2yzz	
100 (43 – 154)	3.3	80	DCM3623xA5N0480yzz	Littelfuse 487 8A Cooper Bussman PC-Tron PCB-3-R, PCB-4-R, PCD-5-R
	5	120	DCM3623xA5N06A2yzz	Littelfuse 487 8A Bussman PC-Tron PCD-5-R
	12	240	DCM3623xA5N13B4yzz	Littelfuse 487 8A Bussmann ABC-10-R
	15	240	DCM3623xA5N17B4yzz	
	24	240	DCM3623xA5N26B4yzz	
	28	240	DCM3623xA5N31B4yzz	
	48	240	DCM3623xA5N53B4yzz	

Acceptable Fuse Types and Current Rating for the DCM ChiP Family of Converters (Cont.)				
Input Voltage Range (Volts)	**Output Voltage (Volts)**	**Output Power (Watts)**	**ChiP Model Number**	**Recommended Fuse**
DCM4623				
275 (120 – 420)	3.3	110	DCM4623xD2N04A1yzz	Bussmann PC-Tron PCB-3-R
	5	190	DCM4623xD2N06A9yzz	
	12	375	DCM4623xD2N13C8yzz	Bussmann PC-Tron PCD-5-R
	15	375	DCM4623xD2N17C8yzz	
	24	375	DCM4623xD2N26C8yzz	
	28	375	DCM4623xD2N31C8yzz	
	48	375	DCM4623xD2N53C8yzz	
270 (160 – 420)	3.3	150	DCM4623xD2K04A5yzz	Bussmann PC-Tron PCB-3-R
	5	250	DCM4623xD2K06B5yzz	Bussmann PC-Tron PCB-3-R
	12	500	DCM4623xD2K13E0yzz	Bussmann PC-Tron PCD-5-R
	15	500	DCM4623xD2K17E0yzz	
	24	500	DCM4623xD2K26E0yzz	
	28	500	DCM4623xD2K31E0yzz	
	48	500	DCM4623xD2K53E0yzz	
300 (180 – 420)	12	400	DCM4623xD2J13D0yzz	Bussmann PC-Tron PCB-5-R
290 (160 – 420)	13.8	600	DCM4623xC8G16F0yzz	Bussmann PC-Tron PCD-5-R
300 (200 – 420)	24	600	DCM4623xD2H26F0yzz	Bussmann PC-Tron PCD-5-R
	13.8	500	DCM4623xD2H15E0yzz	Bussmann PC-Tron PCD-5-R
	28	500	DCM4623xD2H31E0yzz	
	48	500	DCM4623xD2H53E0yzz	

DCM Output Capacitor

To ensure proper operation of the DCM, the capacitance of the load must be within the limits that are defined in the data sheet by $C_{OUT-EXT}$ for normal operation. The maximum limit is required to avoid excessive start-up time, which could trigger output undervoltage fault protection. The minimum limit for $C_{OUT-EXT}$, as well as the minimum ESR of the external capacitor, $R_{COUT-EXT}$, are needed to ensure control loop stability.

For applications where the DCM sees very light loading, certain DCM models have increased minimum required external output capacitor values. The higher values depend on the load transients and the trim transients that the application imposes on the DCM. During Light-Load Boosting, a sudden change in the load – for instance, a step increase from a light load condition – may not be tracked by the control loop, as explained above. If there is not enough capacitance on the output, this could cause the output voltage to drop below the undervoltage fault protection threshold $V_{OUT-UVP}$, causing shut down. (See Output Undervoltage Fault Protection (UVP) in the Fault Handling sub-section of the Standalone Operation section on page 43.)

To prevent this from happening, the minimum allowed output capacitance value must be increased so that it falls in the range given by $C_{OUT-EXT-TRANS}$. This effect is amplified for applications which dynamically trim the DCM output at the same time these load transients are occurring. In this case, the minimum allowed output capacitance must be further increased, per the limits of $C_{OUT-EXT-TRANS-TRIM}$, to prevent the load transient and dynamic trim event from triggering fault protection.

Location of Output Capacitor

Any additional impedance between the DCM output pins and output capacitor may lead to control loop stability issue. Therefore, the output capacitor must be placed physically near the output pins of the DCM module as shown in Figure 2.1.

NOTE: While choosing the output capacitor, operating / environmental temperature must be taken into consideration.

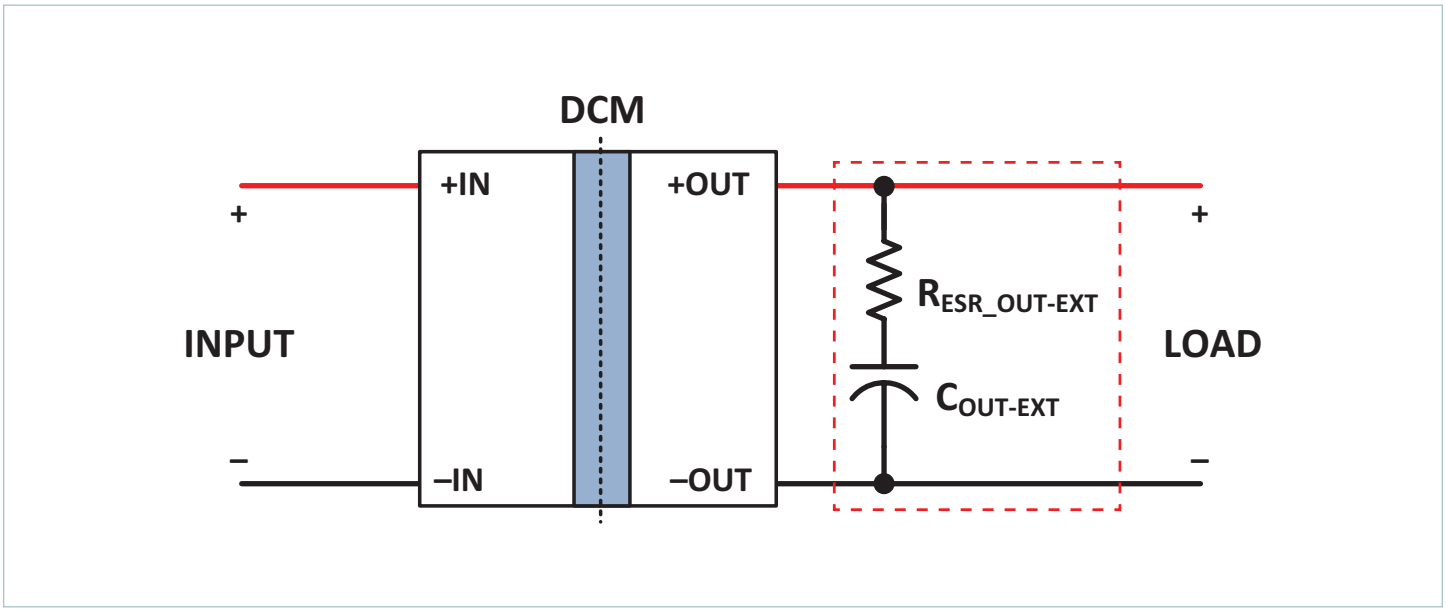


Figure 2.1 — *Location of external output capacitor*

Referencing of Input and Output Terminals

The input and output leads of the DCM should be referenced to the EMI ground plane at some point to avoid stray voltages. For offline applications the input leads are often referenced to earth ground at the AC source ahead of the bridge rectifier. Either + or –Output terminal may be referenced to earth ground. "Floating" inputs or outputs should at a minimum have a high-resistance divider to bleed off stray charges to avoid damage to the insulation system.

Filtering Guidelines Introduction

This section of the design guide is divided into three sub-sections, each sub-section provides guidelines on the following topics.

- *Source Impedance and its Effects on Performance of the Switching Converters*
  The focus of this sub-section is to provide design guidelines and simulations on selecting an optimum value of decoupling capacitor and its equivalent series resistance (ESR) for reducing the source impedance.
- *Input Filter Design and Simulation*
  This sub-section focuses on the design and simulation of a typical differential-mode input filter network using the spice simulation tool and also provides actual measurements of the noise current of the DCM with and without input filters. In addition, Vicor also offers the Filter Design Tool, an online calculator that allows users to analyze the performance characteristics of various filtering network topologies with user defined filtering component values. Please refer to the following link:
  https://app2.vicorpower.com/filterDesign/intiFilter.do
- *Common-Mode Input Filter Design*
  This sub-section provides information on common-mode noise sources, noise-mitigation techniques and focuses on the design of the common-mode noise filter.

Aforementioned sub-sections 1, 2 are general methodologies used in power system designs to reduce the effect of source impedance and to mitigate the differential mode noise generated by the switching converters. Sub-section 3 is a common method used to mitigate the common mode noise generated by the switching converters. Information presented on the common mode input filter design is confined to theoretical aspects of common mode noise filtering, if the system have to meet a particular EMI standards (such as MIL-STD, EN etc.), Vicor offers EMI filter solutions specifically designed to DCM product line; please contact Applications Engineering for more details.

Source Impedance and its Effects on Performance of the Switching Converters

Typically switching power converters, including the DCM, are well designed to exhibit good stability margins and certain performance characteristics in their standalone operation.However, when a single or multiple converters are designed into a DC distribution system, illustrated in Figure 2.2, the interactions between the negative incremental input impedances of the converter(s) and the total output impedance of the source will alter the dynamic performance characteristics of the switching converters and also causes system-level instabilities. The interaction of the impedances is shown in Figure 2.6. These issues are a consequence of:

a. Constant power loads (regulated converters) existing throughout the DC distribution system

b. Interactions among the several converter feedback control loops tied at the DC bus

Note: The total output impedance of the source viewed from the $Z_{TOTAL\text{-}SOURCE}$ point , shown in Figure 2.2, is Thevenin equivalent impedance of source, distribution line and input filter impedances.

System instability can be avoided by keeping the total output impedance of the source ($Z_{TOTAL\text{-}SOURCE}$) at least ten times lower than the input impedance ($Z_{IN\text{-}DCM}$) of the DCM over a frequency range of DC to the maximum control loop bandwidth:

$$Z_{TOTAL\text{-}SOURCE} \leq (Z_{IN\text{-}DCM}/10) \text{ for all } F[0 : 20kHz].$$

This can be achieved by choosing the optimum value of the decoupling capacitor network along with proper design of the input filtering network.

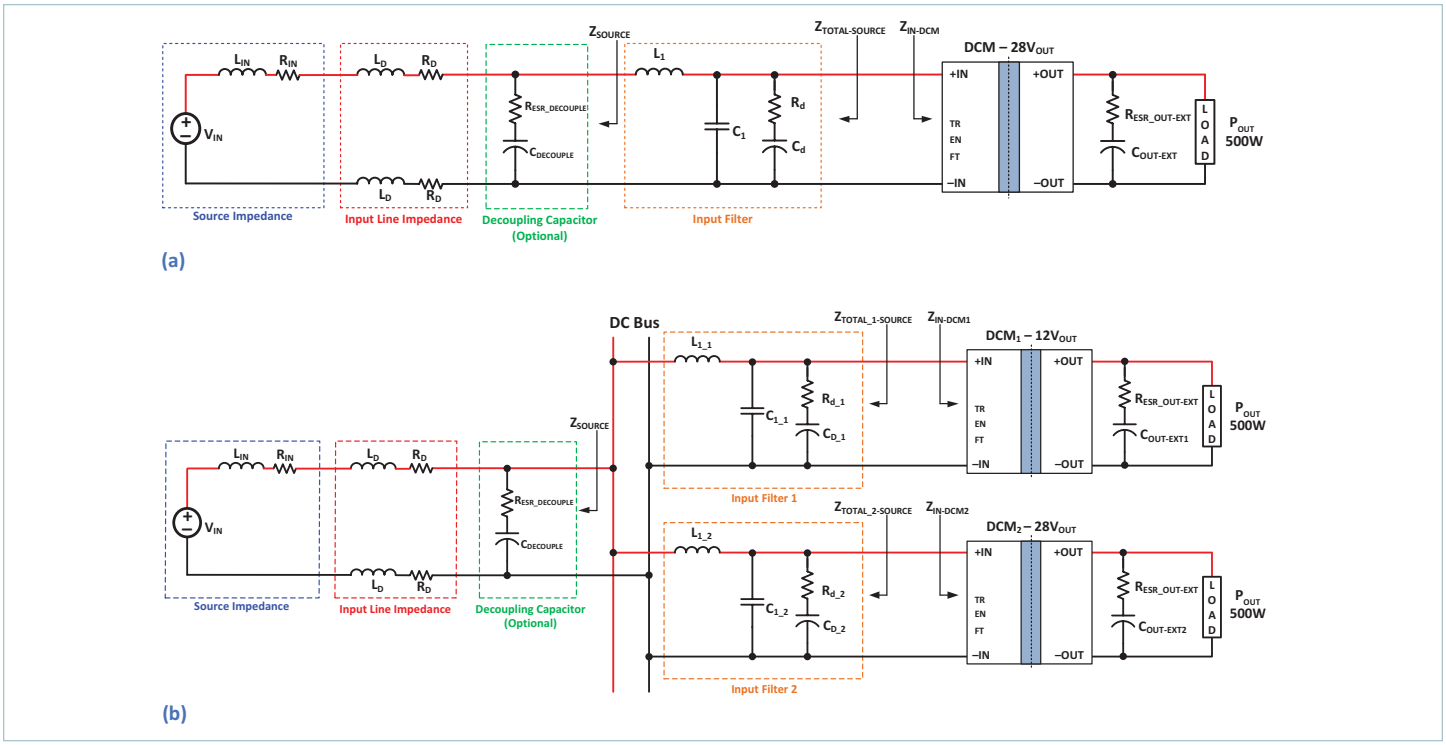


Figure 2.2 — *Typical DC-DC distribution system using DCMs: (a) single converter system, (b) multiple converter system*

As a common practice, a high value of the decoupling capacitor network is placed on the DC bus, as shown in Figure 2.2. However, placing a large, bulk decoupling capacitor may not effectively reduce the effect of source impedance, but will adversely increase the required printed circuit board area. Therefore, the decoupling capacitor must be optimally selected based on the source impedance and distribution line impedance. In the cases where the source impedance and distribution line impedance are not significant enough to cause interaction with the input impedance of the switching converter, an adequately damped input filter may only enough to keep the $Z_{TOTAL\text{-}SOURCE}$ lower than the $Z_{IN\text{-}DCM}$.

For quick reference only: Follow these steps to select an optimum value of decoupling capacitor and its ESR:

Step 1: Calculate the negative incremental input impedance ($Z_{IN\text{-}DCM}$) of the DCM using Equation 2.1.

Step 2: Identify the source and line impedances. Represent the system in simpler way by separating the system into source and load subsystems.

Step 3: Plot the impedances vs. frequency using spice simulation tool. Identify the interaction.

Step 4: Select resonant frequency (f_{SOURCE}) much lower than the DCM control loop bandwidth (20kHz). Calculate the decoupling capacitor using the Equation 2.2.

Step 5: Calculate the required ESR of decoupling capacitor using the Equation 2.3.

Step 6: Plot the impedance vs. frequency response in spice by modifying the Step 3 simulation model.

Verify there is no interaction between the impedances.

Negative Incremental Input Impedance (Z_{IN-DCM})

The DCM, as a feedback controlled switching converter, generates a regulated, isolated DC output voltage for a given range of input voltage and load current. Therefore, for a given load, the output power is constant irrespective of input voltage. This means that the input power is also constant such that as the input voltage is increased, the corresponding input current decreases and vice-versa, shown in Figure 2.3. Thus, the DCM behaves as a constant power load at its input terminals up to the control loop bandwidth; the DCM presents a negative incremental impedance (Z_{IN-DCM}) at its input terminals and when interacting with the Thevenin equivalent source impedance ($Z_{TOTAL-SOURCE}$), may result in system-level stability issues.

At any Quiescent operating point, the system can be considered linear and the slope of the resulting linear input current curve is negative, shown in Figure 2.3; thus, the Z_{IN-DCM} is negative. Theoretically, the negative incremental impedance magnitude can be calculated using the Equation 2.1. For more detailed mathematical analysis on the input impedance and its effects on system stability and performance, please refer to the article below:

https://www.vicorpower.com/documents/whitepapers/wp-input-source-impedance-DC-DC-VICOR.pdf

Where:

$$Z_{IN\text{-}DCM} = -\frac{V_I^2}{P_I} \quad or \quad -\frac{\Delta V_I}{\Delta I_I} \quad for\ all\ F\ [0 : 20kHz] \qquad 2.1$$

Z_{IN-DCM} = Negative incremental impedance of the DCM

V_I = Input voltage to the DCM

I_I = Input current of the DCM

P_I = Input power of the DCM

ΔV_I = Change in the input voltage of the DCM

ΔI_I = Change in the input current of the DCM

F = Control loop bandwidth of the DCM

As an example, DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) with a constant output power of 500W is considered. The input power, accounting for operational power dissipation is calculated to be 533W. For an input voltage range of 160 to 420V, the worst case value of Z_{IN-DCM} is at the low line. The input current drawn by the DCM is 3.33A and the resulting negative incremental impedance is:

$$Z_{IN\text{-}DCM} = -\frac{160V}{3.33A} \quad or \quad -\frac{(160V)^2}{533W} = -48\Omega$$

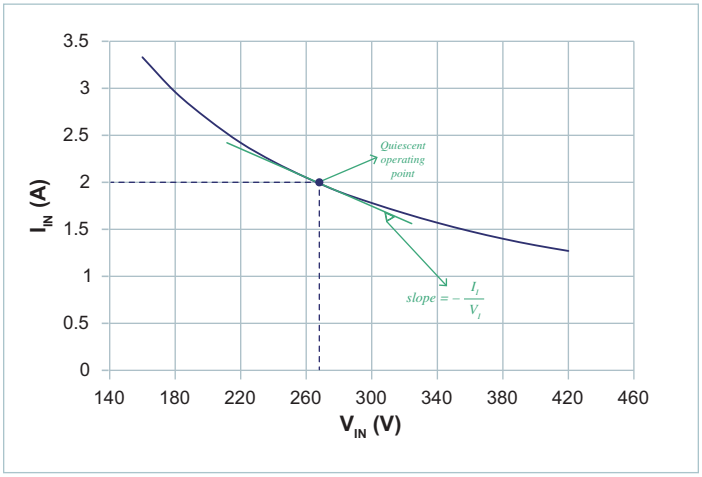


Figure 2.3 — *V_{IN} vs. I_{IN} characteristics at the DCM input terminals, with constant P_{OUT}*

Note that the Z_{IN-DCM} above the range of control loop bandwidth (F) of the DCM will be same as the open loop input impedance of the DCM. For the sake of simplicity, Z_{IN-DCM} is assumed to be constant over the entire frequency range of interest, as shown in Figure 2.6.

Stability Analysis

To conduct system stability analysis on a complex DC distribution system, shown in Figure 2.2, a simpler representation is first constructed by separating the system into source and load subsystems connected at an arbitrary interface as illustrated in Figure 2.4.

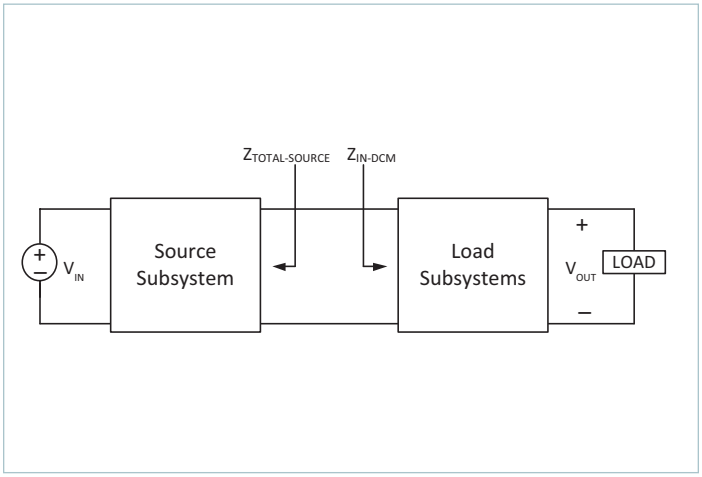


Figure 2.4 — *Block diagram representation of interacting source and load subsystems*

To demonstrate the interaction, an spice simulation model, shown in Figure 2.5, is designed and analyzed with a 0.01Ω output resistance (R_{IN}), 0.1µH output inductance (L_{IN}) power source and a 12-gauge, 15ft length distribution line. Using the commonly available online tools for wire impedance calculations, the parallel wire distribution line inductance (L_D) and line resistance (R_D) are calculated based on the assumption that the center-to-center distance between the parallel wires is 2cm.

NOTE: The internal capacitance of the DCM (C_{IN}) is considered in these simulations (for the value of internal capacitance, please refer to the Figure "Effective internal input capacitance vs. applied voltage" in the DCM4623TD2K31E0T00 data sheet (copied in Figure 2.7).

From the simulation results, shown in Figure 2.6, it can be observed that there is an interaction between Z_{SOURCE} and Z_{IN-DCM} at 65kHz. As mentioned above, to avoid interactions, the source and distribution line impedance must be at least ten times lower than the input impedance of the DCM over a frequency range of DC to the maximum control loop bandwidth (20kHz).

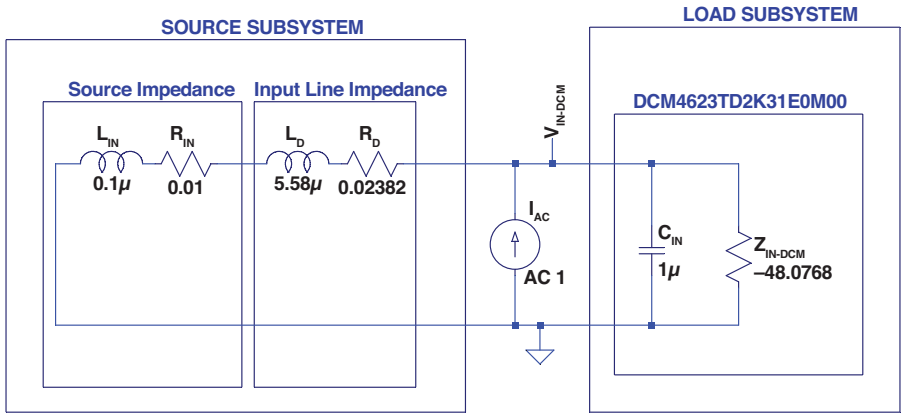


Figure 2.5 — *Example source and load subsystems without decoupling capacitor, input filter*

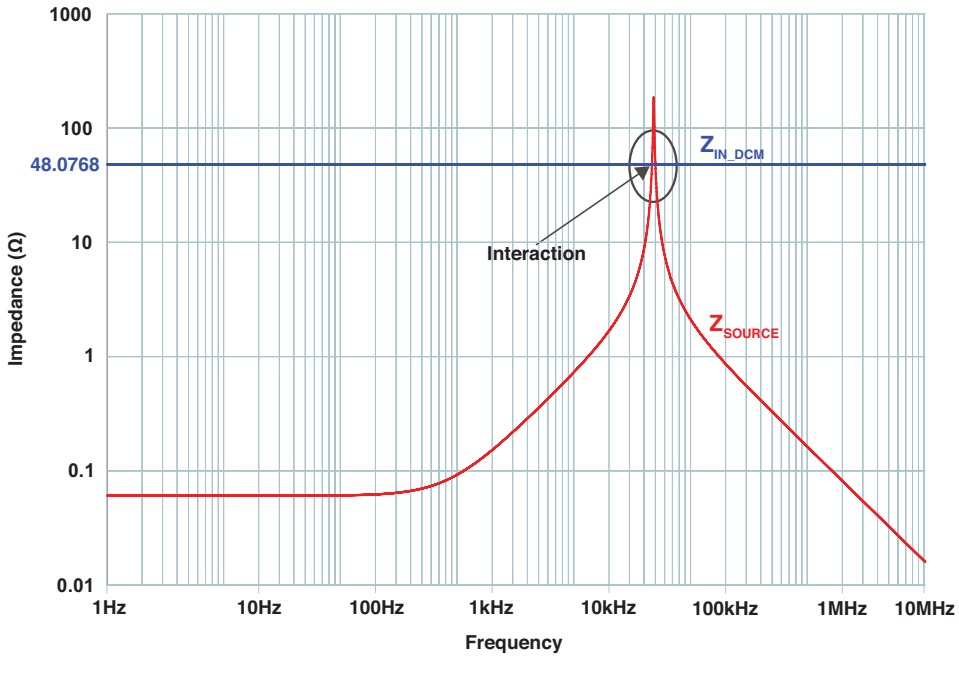


Figure 2.6 — *Interaction between the output impedance of the source and the input impedance of the DCM*

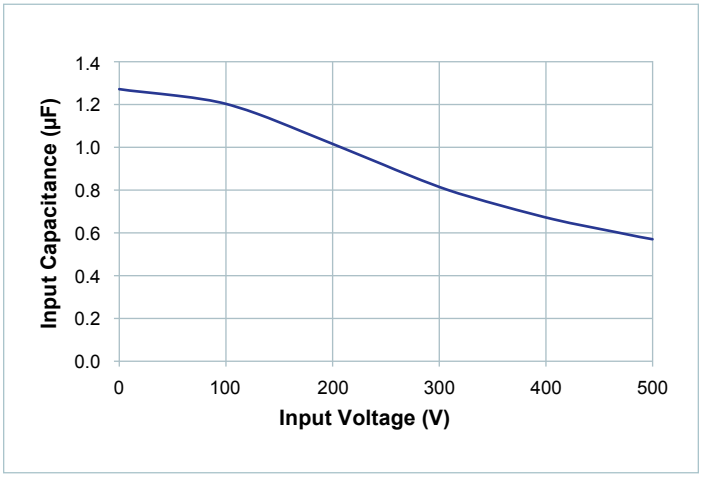


Figure 2.7 — *Effective internal input capacitance vs. applied voltage*

Optimum Value of Decoupling Capacitor

The interactions can be avoided and the stability of the system can be ensured by placing a decoupling capacitor network after the source and input line impedances. This is effectively an LC filter network when viewed from Z_{SOURCE} point, refer to Figure 2.2. The source, line inductor and decoupling capacitor impedance asymptotes intersect at the LC filter resonant frequency (f_{SOURCE}) and by placing the pole at the desired frequency, the optimum value of decoupling capacitor can be determined, which is given in the Equation 2.2:

$$f_{SOURCE} = \frac{1}{2\pi\sqrt{(L_{EQ})\,(C_{DECOUPLE})}} \qquad 2.2$$

Where:

$L_{EQ} = L_D + L_{IN}$, and

L_{EQ} = Equivalent source inductance,

L_D = Distribution line inductance,

L_{IN} = Power source output inductance.

The required ESR of the decoupling capacitor can be determined using the characteristic impedance of the source LC filter network. The characteristic impedance is given in the Equation 2.3:

$$R_{O_{SOURCE}} = \sqrt{\frac{L_{EQ}}{C_{DECOUPLE}}} \qquad 2.3$$

For the above example, the peak output impedance of the source must be kept below the DCM control loop bandwidth. Thus, to find the optimum value of decoupling capacitor, fsource is chosen to be 8kHz. By substituting the values of L_{EQ} and fsource in Equation 2.2, the value of $C_{DECOUPLE}$ is calculated as 69.68µF. By substituting the values of L_{EQ} and $C_{DECOUPLE}$ in Equation 2.3, the ESR value is calculated as 0.285Ω. The simulation of the system with an additional decoupling capacitor is shown in Figure 2.8.

Figure 2.9 shows the source output impedance and the input impedance of the DCM, this clearly shows that the source output impedance is well damped. Since there is a large separation between the source output impedance and the input impedance of the DCM, no interaction is expected.

Another approach for reducing the effect of source impedance is adding a well damped input filter. Additional advantages of using an input filter are that it attenuates the conducted electromagnetic interference (EMI) and it provides input voltage noise rejection. Input filters are discussed in detail in the next section of the design guide. The simulations shown in Figure 2.10 include the input filter. The impedance simulation results illustrated in Figure 2.11 shows a large separation between the total output impedance ($Z_{TOTAL\text{-}SOURCE}$) and the input impedance of the DCM; therefore, no interaction is expected.

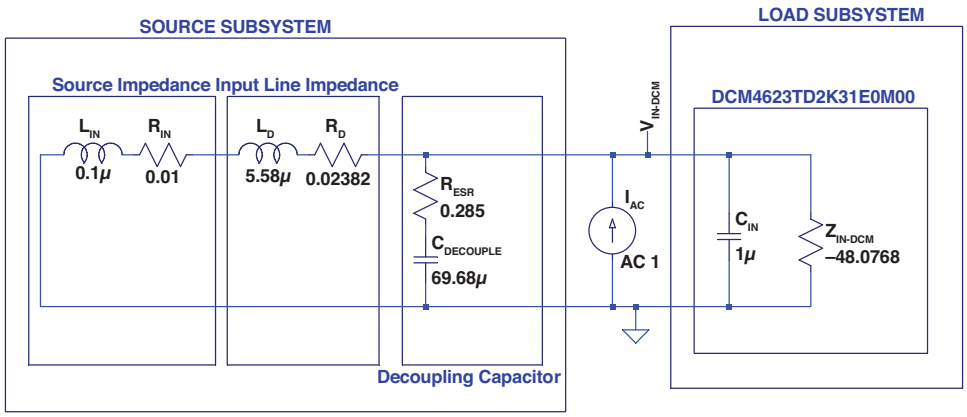


Figure 2.8 — *Example source and load subsystems with decoupling capacitor*

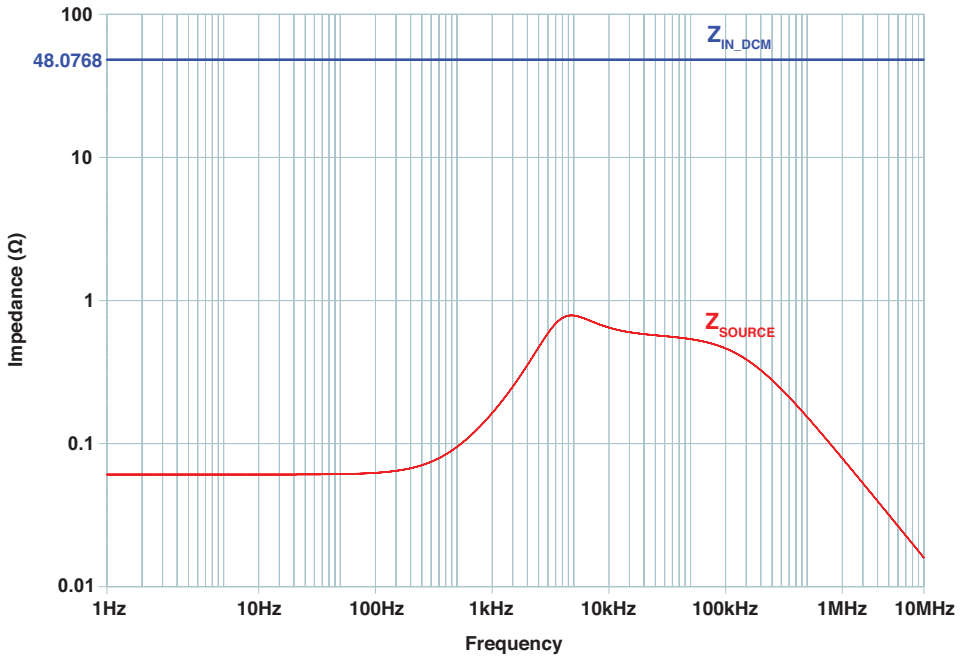


Figure 2.9 — *Output impedance of the source and the input impedance of the DCM, with a decoupling capacitor*

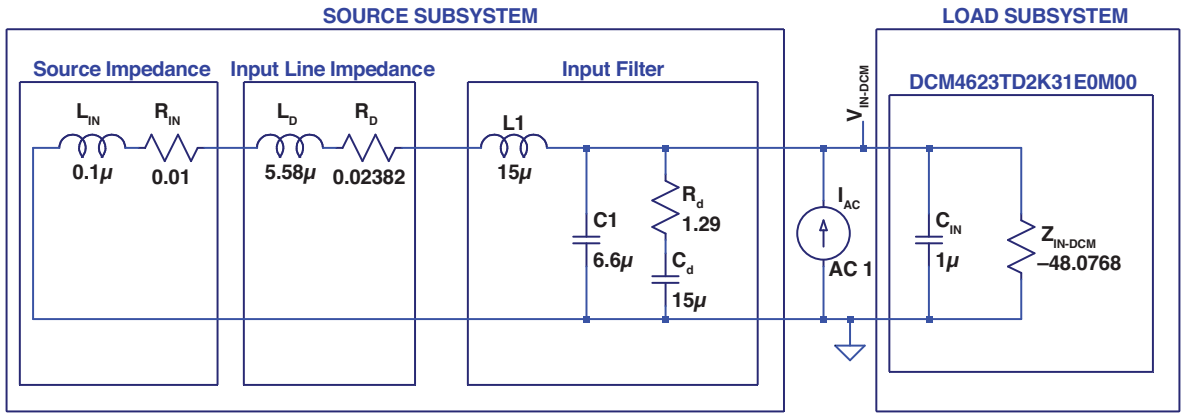


Figure 2.10 — *Example source and load subsystems with an input filter*

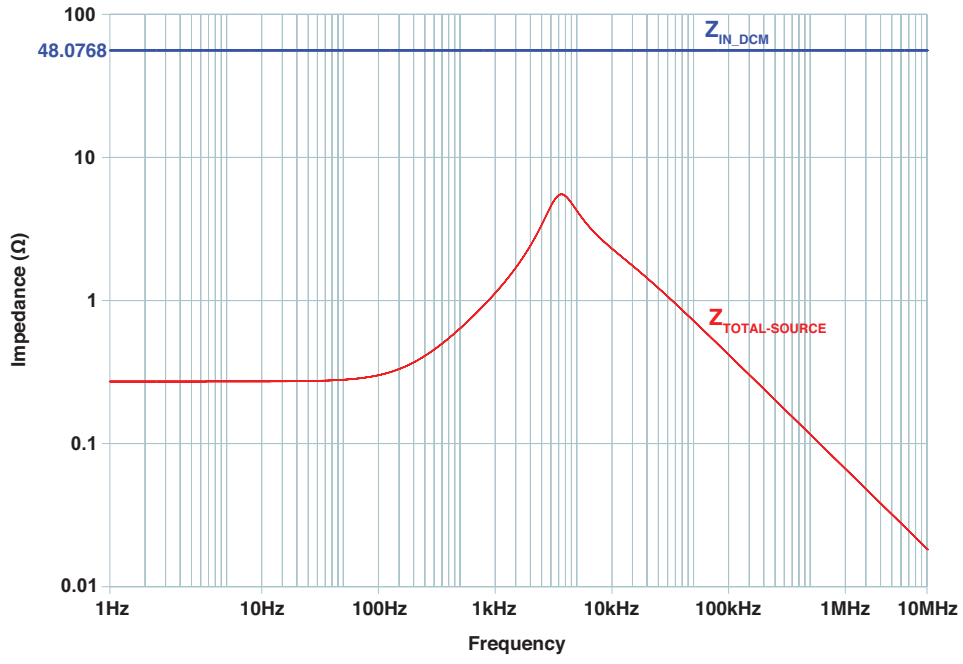


Figure 2.11 — *Output impedance of the source and the input impedance of the DCM, with an input filter*

Stability Analysis of a Multiple Converter System

To analyze the stability of a multiple converter system, which is shown in Figure 2.2 (b), a simulation model is created in spice. The simulation model, shown in Figure 2.12 consists of a common source and line impedances connected to a DC bus and multiple DCMs supplying the independent loads. DCM1 has a constant output power of 400W and DCM2 has a constant output power of 500W. The corresponding input power consumed by DCM1 and DCM2, including the losses is 430W, 533W, respectively. By using the Equation 2.1, the negative incremental input impedances $Z_{IN\text{-}DCM1}$ and $Z_{IN\text{-}DCM2}$ are calculated.

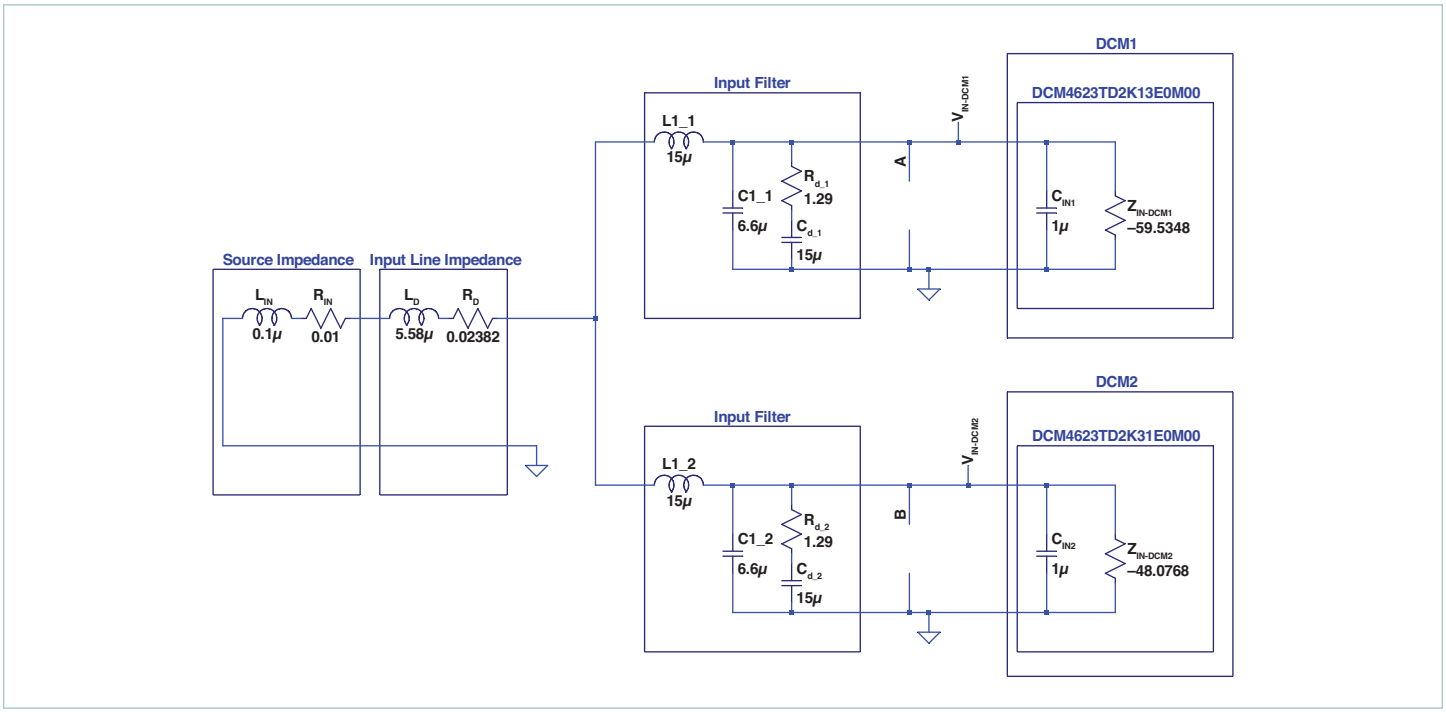


Figure 2.12 — *Example multiple converter system with an individual input filter*

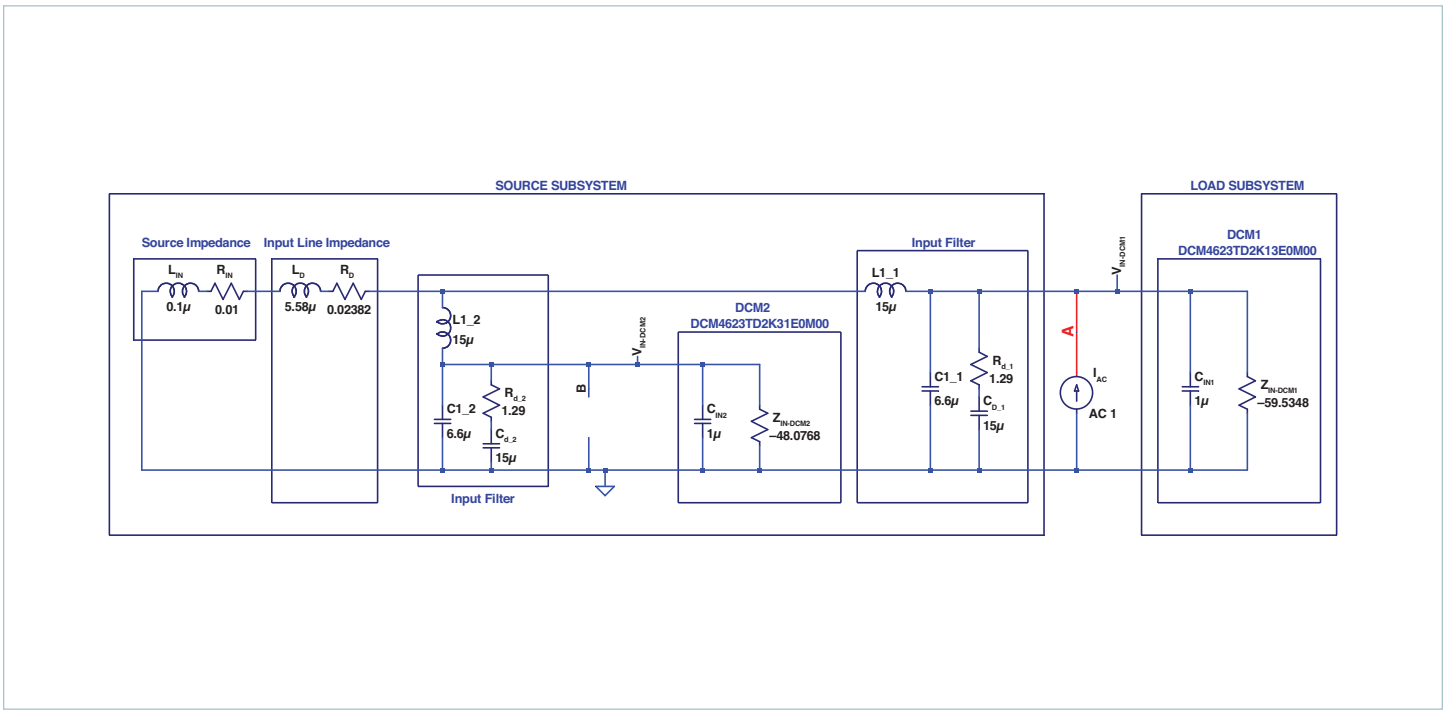


Figure 2.13 — *Equivalent source viewed from node A, multiple converter system separated into source and load subsystems*

Figure 2.12 is redrawn to represent the complex multiple converter system in a much simpler way by separating into the source and load subsystems. The equivalent circuit is depicted in Figure 2.13 and shows an equivalent source ($Z_{TOTAL\_1\text{-}SOURCE}$) viewed from node A. The shunt branch consisting of L_{1_2}, C_{1_2}, R_{d_2}, C_{d_2}, C_{IN2} and $Z_{IN\text{-}DCM2}$ is the impedance of DCM2 and its input filter viewed from the DC bus. The simulation results shown in Figure 2.14 are the comparison of the input impedance of the DCM1 ($Z_{IN\text{-}DCM1}$) and the total output impedance of the source ($Z_{TOTAL\_1\text{-}SOURCE}$) viewed from node A. The results clearly show that the impedances are well separated and no interaction is expected over the frequency range of interest.

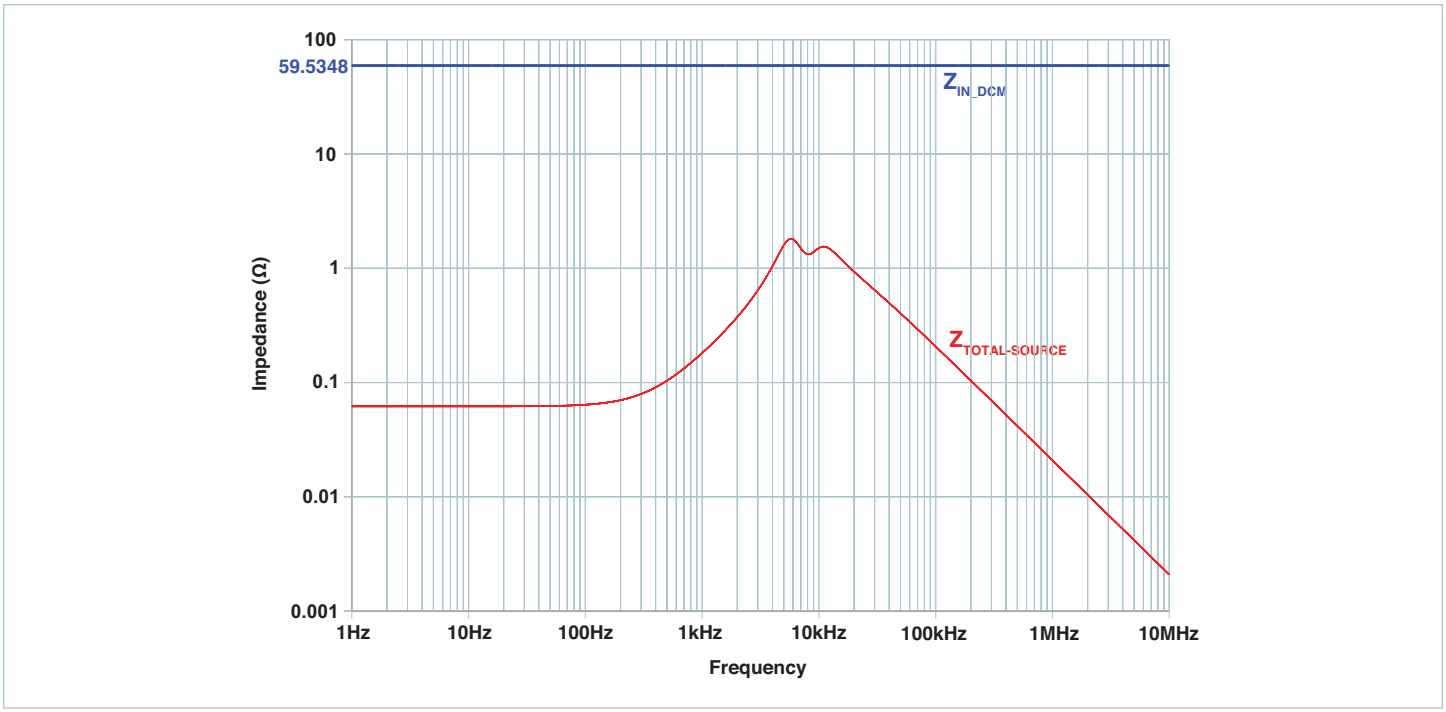


Figure 2.14 — *Total output impedance of the source and the input impedance of the DCM1 viewed from node A*

Figure 2.12 is redrawn in similar fashion as explained earlier, when viewed from the node B. The circuit shown in Figure 2.15 is an equivalent source ($Z_{TOTAL\_2\text{-}SOURCE}$) viewed from node B. The shunt branch consisting of L_{1_1}, C_{1_1}, R_{d_1}, C_{d_1}, C_{IN1} and $Z_{IN\text{-}DCM1}$ is the impedance of DCM1 and its input filter viewed from the DC bus. The simulation results, shown in Figure 2.15, clearly show that the input impedance of the DCM2 ($Z_{IN\text{-}DCM2}$) and the total output impedance of the source ($Z_{TOTAL\_2\text{-}SOURCE}$) viewed from node B are well separated and no interaction is expected over the frequency range of interest. Therefore, no stability problems are expected in the multiple converter system.

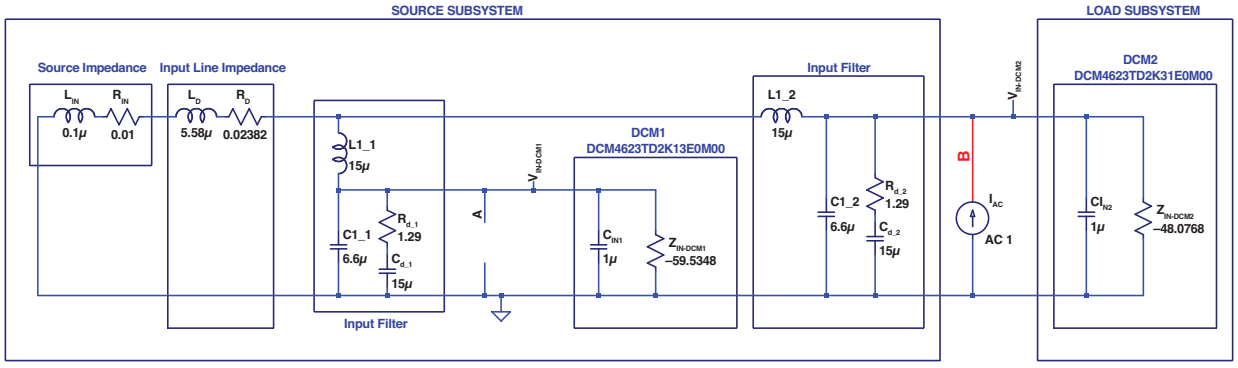


Figure 2.15 — *Equivalent source viewed from node B, multiple converter system separated into source and load subsystems*

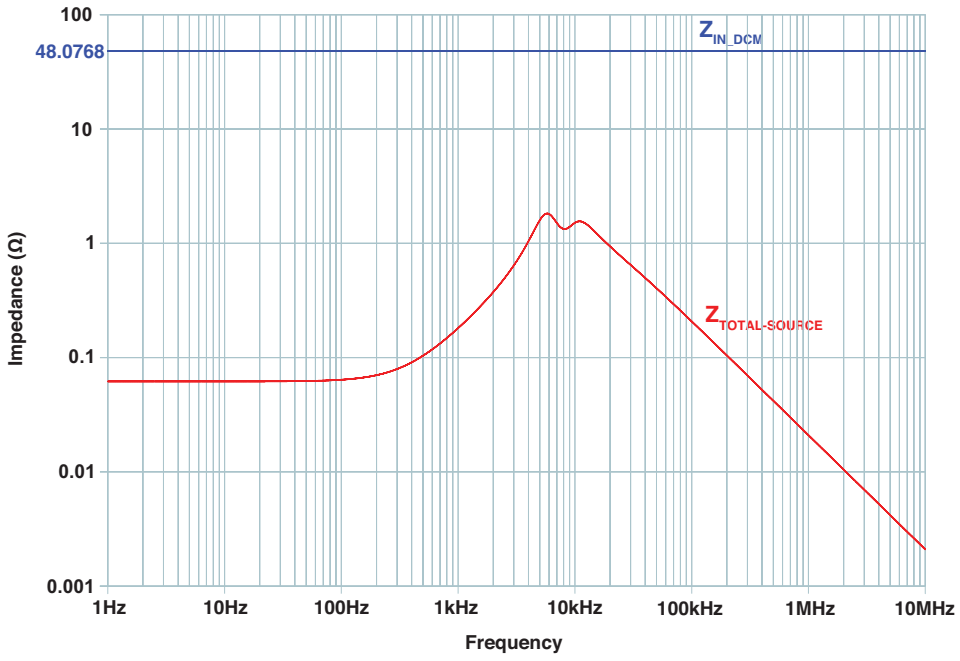


Figure 2.16 — *Total output impedance of the source and the input impedance of the DCM2 viewed from node B*

Input Filter Design and Simulation

Introduction

Switching power converters, including the DCM, generate noise currents at the switching frequency and its higher-order harmonics. The noise currents are of two types, common mode and differential mode and will propagate from the DCM back to the power source along the interconnecting conductors.

This noise may interfere with the power source operation and other systems sharing the same connection. Therefore, an input filter is often used between the power source and the switching converter to lower the conducted electromagnetic interference (EMI) and to provide input voltage noise rejection.

Differential-Mode Input Filter Design and Simulation

The differential-mode noise currents are result of normal operation of the circuit. The differential mode noise current path of a representative switching converter and the power source is shown in Figure 2.17.

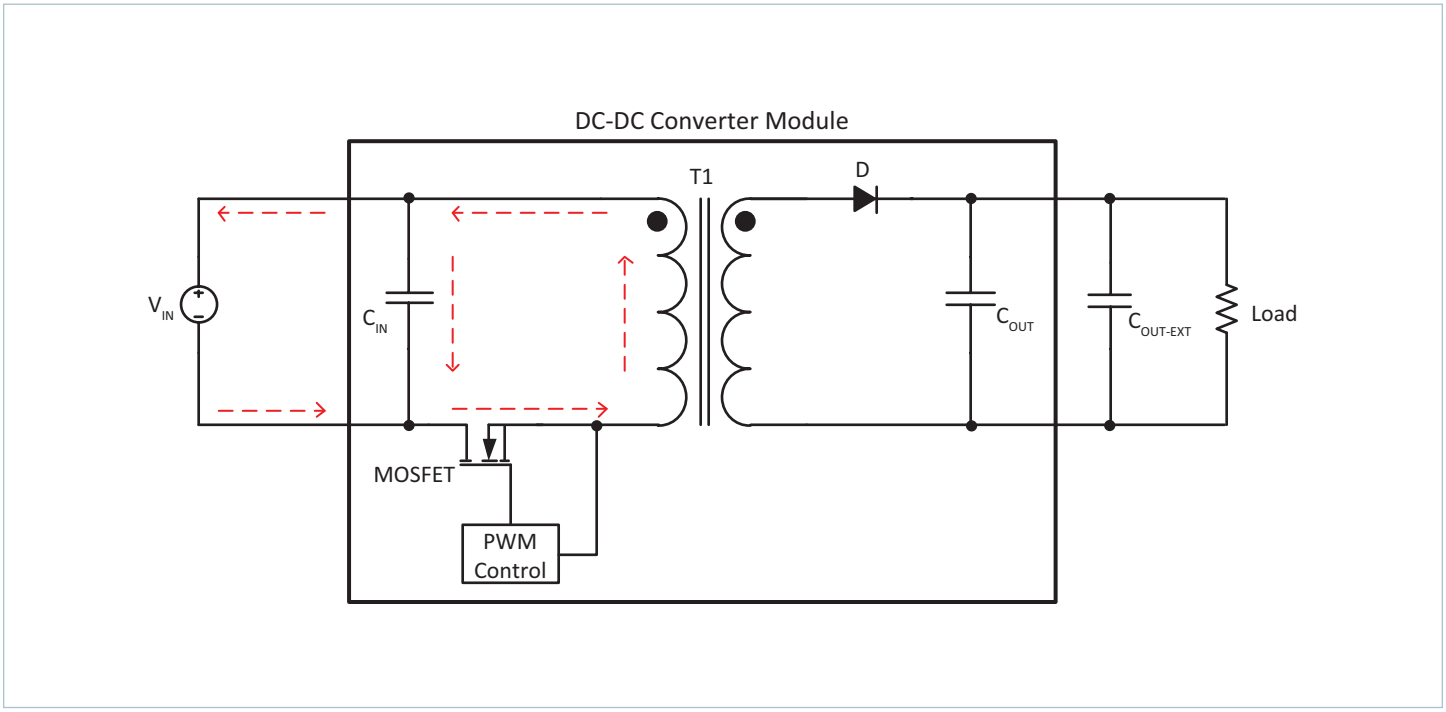


Figure 2.17 — *Differential-mode noise currents path*

Problems Associated with Addition of Input Filters:

Introducing a filter at the input of a DCM without considering its impact on the switching converter dynamics can lead to system-level stability issues. The DCM, as a feedback controlled switching converter, behaves as a constant power load at the input terminals; the DCM presents a negative incremental impedance at its input terminals, plotted in blue in Figure 2.18. The output impedance of an example undamped input filter is also plotted in red in Figure 2.18. The interaction between the input filter's output impedance and the DCM input impedance will often result in control loop instability of the DCM and degradation of dynamic performance. This, in turn, will cause large oscillations in the input voltage and output voltage during start up, load steps, and other transient events. These issues can be eliminated by appropriately damping the input filter. Various filter damping techniques are discussed in this section. Further details on switching converter system stability analysis are located in the section on source impedance and its effects on system stability.

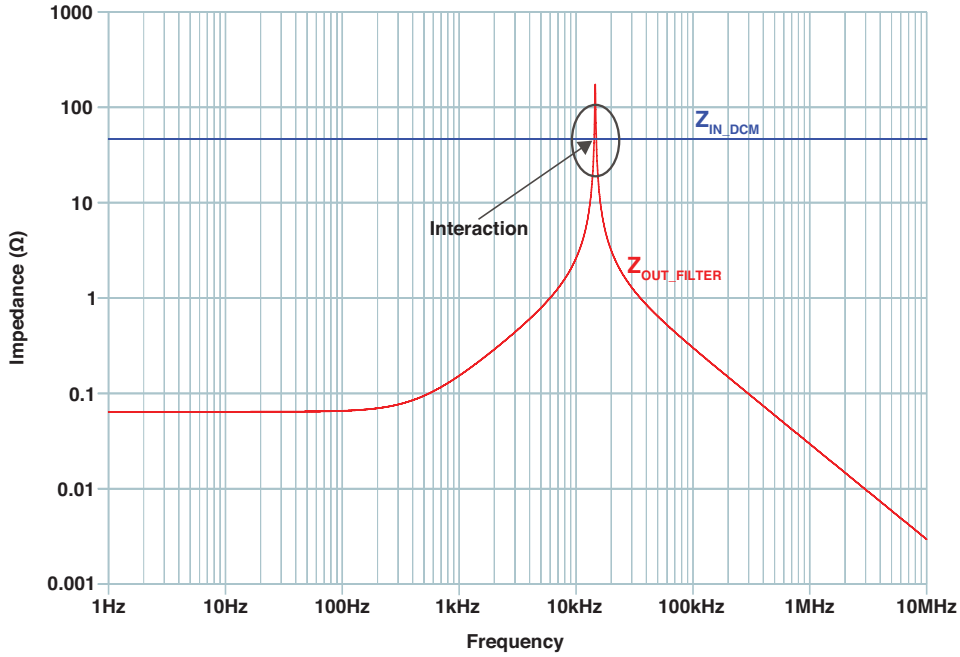


Figure 2.18 — *Filter output impedance interaction with DCM input impedance*

Input Filter Design

Before diving into the design of the input filter, the designer must gather information on the following:

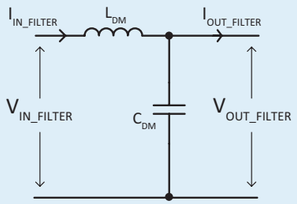
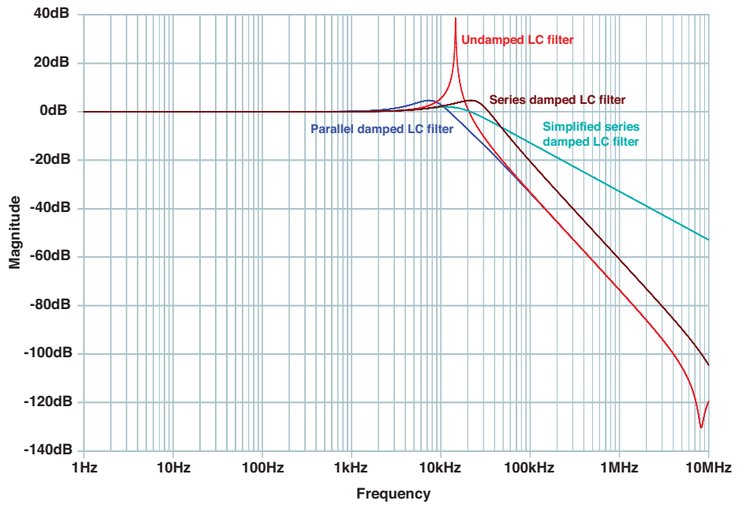
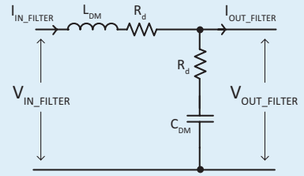
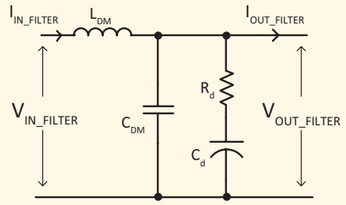
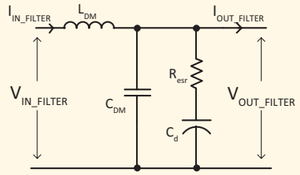
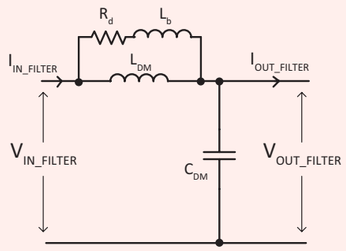
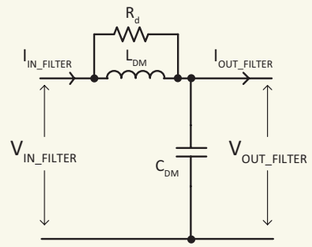
1. Identify the noise spectrum of the DCM from the actual measurements or from the data sheet of the DCM.
2. Identify the operating point and plot the input impedance of the DCM using spice simulation tool. For mathematical analysis, please refer to the the section on source impedance and its effects on system stability.
3. Identify the filtering requirements.
4. Select an appropriate filter network to meet the filtering requirements.

Commonly used differential mode input filtering network topologies for switching power converters are as follows:

1. Undamped LC filter
2. Parallel damping
   a. Simplified parallel damping
3. Series damping
4. Simplified series damping

In order to see the differences in the performance of above mentioned filter network topologies, an example of designing an input filter network for DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) using the spice simulation tool is considered. The aim of this filter design is to obtain at least –40dB attenuation at the switching frequency (1MHz).

To achieve this aim, an undamped LC filter network topology is initially used. This topology is a second order system that provides a roll-off of –40dB/decade. Therefore, as a rule of thumb, the cutoff frequency must be at least ten times lower than the converter switching frequency.

Filter Topology & Common Notes		Equations and Notes	Advantages	Disadvantages
Undamped LC filter 	**Frequency Response Plot (Voltage / Current Transfer Function)** According to the duality property, the voltage transfer function viewed from the input side is same as the current transfer function viewed from the output side. $TF = \frac{V_{OUT\_FILTER}}{V_{IN\_FILTER}} = \frac{I_{IN\_FILTER}}{I_{OUT\_FILTER}}$ 	• Q-factor of ideal components in spice models at the resonant frequency is infinite. • Damping can be achieved using series resistors as shown below: **Damped LC filter** 	• Least component count. • Size of the filter is small. • Cost is lower.	• Peaking at resonant frequency. • A damping resistor in series with inductor L_{DM} degrades the efficiency and a damping resistor in series with capacitor C_{DM} degrades the attenuation characteristics of the filter..
Parallel-damped LC filter 		The value of blocking capacitor: $C_d = nC_{DM}$ The value of peak output impedance: $\lvert Z_{OUT\text{-}FLTER}\rvert = R_O \frac{\sqrt{2(2+n)}}{n}$ The value of damping resistance: $R_d(optimum) = R_O \sqrt{\frac{(2+n)\bullet(4+3n)}{2n^2(4+n)}}$	• At the resonant / cutoff frequency, the capacitor C_d must have lower impedance than R_d and a larger impedance than the filter capacitor CDM. • R_d – C_d parallel branch can be replaced with a higher ESR value capacitor type (aluminum electrolytic or tantalum), shown below: 	• Require a high value blocking capacitance C_d. • Size and cost of the filter increase.
Series-damped LC filter 	• Cut-off frequency: $f_c = \frac{1}{2\pi\sqrt{L_{DM}C_{DM}}}\ (Hz)$ [a] Where LDM = Filter Inductor CDM = Filter Capacitor • The cut-off frequency must be below the crossover frequency of the converter. • At resonance $\omega L_{DM} = 1 / \omega C_{DM}$, characteristic impedance: $R_O = \sqrt{\frac{L_{DM}}{C_{DM}}}$ • All the topologies are a second order system that provides a roll-off of –40dB / decade ([a]See specific notes of simplified series-damped LC filter).	The value of blocking inductor: $L_b = nL_{DM}$ The value of peak output impedance: $\lvert Z_{OUT\text{-}FLTER}\rvert = R_O\sqrt{2n(1+2n)}$ The value of damping resistance: $R_d(optimum) = R_O \sqrt{\frac{n(3+4n)(1+2n)}{2(1+4n)}}$	• The inductor L_b must have an impedance magnitude that is sufficiently smaller than R_d at the filter resonant frequency. • Size of the filter is small compared to parallel-damped LC filter. • Cost is lower.	• High-frequency attenuation is degraded.
Simplified series-damped LC filter 		[b] Simplified series-damped LC filter is a second order system, ideally this should provide a roll-off of –40dB / decade, however, due to high-frequency zero ($f_z = R_d / (2\pi L_{DM})$ the roll-off is –20dB / decade.	• Low component count compared to parallel-damped and series-damped filters.	• High-frequency attenuation is degraded.

Design Steps:

1. Select the cut-off frequency below the crossover frequency (20kHz) of the DCM.
2. Choose the inductor L_{DM} based on maximum input current, calculate C_{DM} using Equation [a] above.
3. Select appropriate filter network and calculate the component values based on equations and notes.
   a. Assume peak output impedance $|Z_{OUT\text{-}FILTER}|$ at least ten times lower than input impedance of switching converter.

Component Selection:

1. Choose the self-resonating frequency (SRF) of inductor (L_{DM}) and capacitor (C_{DM}) to be higher than the switching frequency or the converter.
2. Use the multiple ceramic capacitors in parallel for C_{DM}. This, in turn, will effectively attenuates the high-frequency noise.
3. Use low-Q devices, designed for filtering.

1. Undamped LC Filter Network

The undamped input filter circuit shown in Figure 2.19 is a second-order low-pass filter circuit that provides a high-frequency roll-off of –40dB / decade. The resonant frequency of this filter, also known as the cutoff frequency when considering the voltage response is given by the following expression:

$$f_c = \frac{1}{2\pi\sqrt{L_{DM}C_{DM}}}\ (Hz)$$

The peak filter output impedance will occur at this same frequency f_c. The Q-factor for ideal components at the resonant frequency is infinite. However, intrinsic parasitic resistances of the filtering components will limit the peak response. Nonetheless, the output impedance of the undamped LC filter is very large near the resonant frequency. At the resonance condition $\omega L = 1 / \omega C$, the characteristic impedance, R_0 is given by:

$$R_O = \sqrt{\frac{L_{DM}}{C_{DM}}}$$

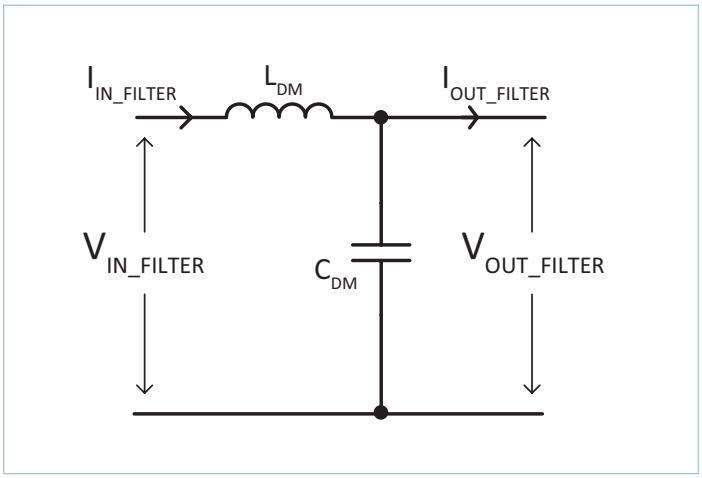


Figure 2.19 — *Undamped LC filter*

Damping the Filter

Parasitic resistances of the inductor and capacitor will provide damping, but may not be sufficient to reduce the resonance peak to acceptable limits. One solution is to provide an additional damping, can be achieved by adding an external resistor in series with the inductor and capacitor, shown in Figure 2.20. However, a damping resistor in series with the inductor will increase the losses and a damping resistor in series with the capacitor will degrade the attenuation characteristics. Therefore, series- / parallel-damping techniques are preferred over the undamped LC filter.

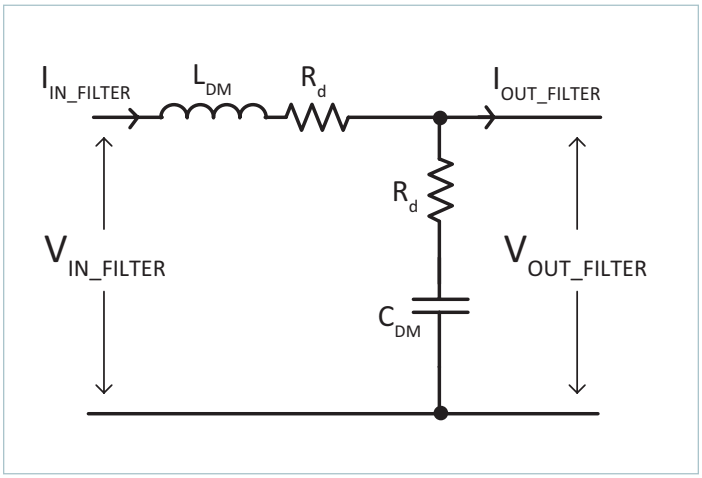


Figure 2.20 — *Damping using series resistors*

Design Example

The DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) with an undamped LC input filter is simulated in spice, as shown in Figure 2.21. To measure the output impedance of the filter, independent input voltage source (V_{DC}) is shorted and an AC current is injected at the output terminals of the filter as in 2.21(a). Filter attenuation characteristics can be obtained by injecting an AC voltage signal at the input terminals of the filter as shown in 2.21(b).

In this design example, the cutoff frequency f_c of the filter is chosen as 15kHz. By choosing the value of inductor L_{DM} = 22µH, the value of C_{DM} is calculated as follows.

$$15kHz = \frac{1}{2\pi\sqrt{22\mu H \bullet C_{DM}}}$$

$$C_{DM} = 5.12\mu F$$

NOTE: The internal capacitance of the DCM (C_{INT_DCM}) is considered in these simulations (for the value of internal capacitance, please refer to the Figure "Effective internal input capacitance vs. applied voltage" in the DCM4623TD2K31E0T00 data sheet copied in Figure 2.7).

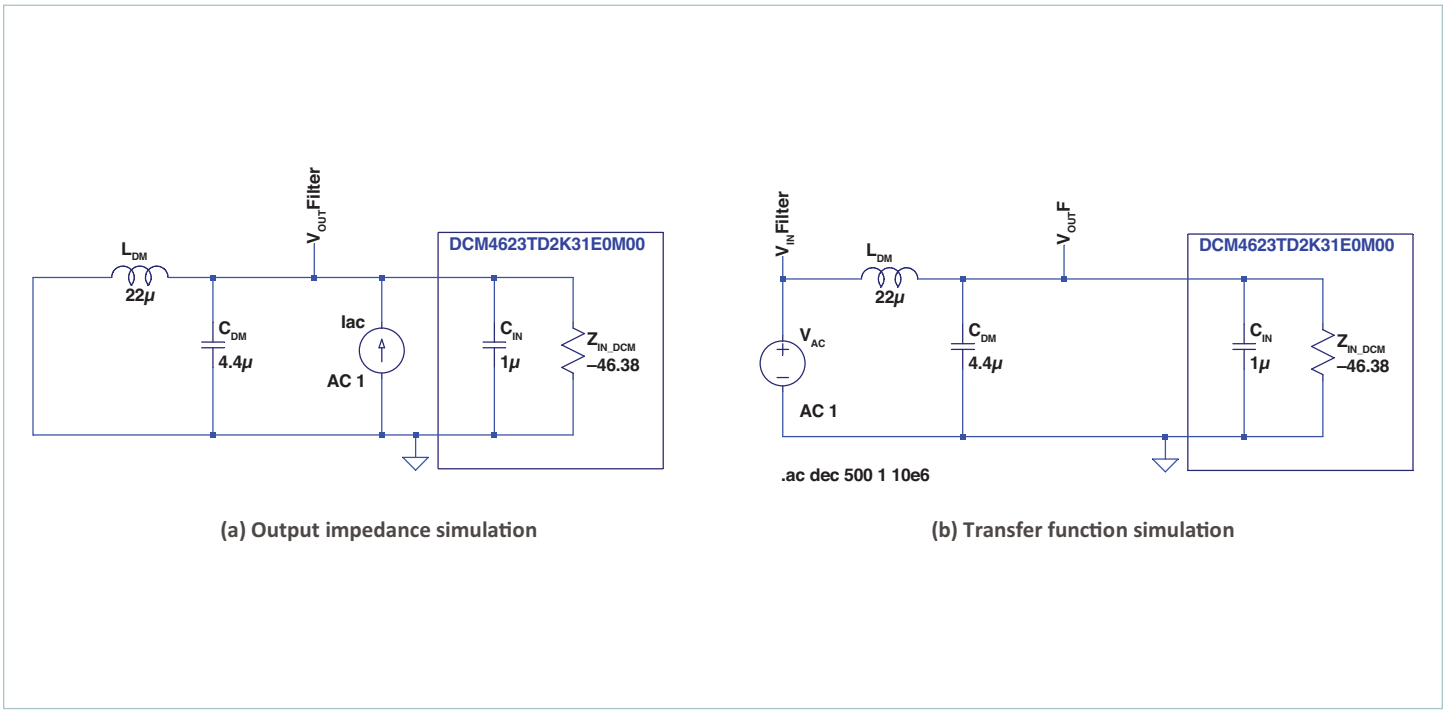


Figure 2.21 — *Undamped LC filter network along with the DCM negative input impedance*

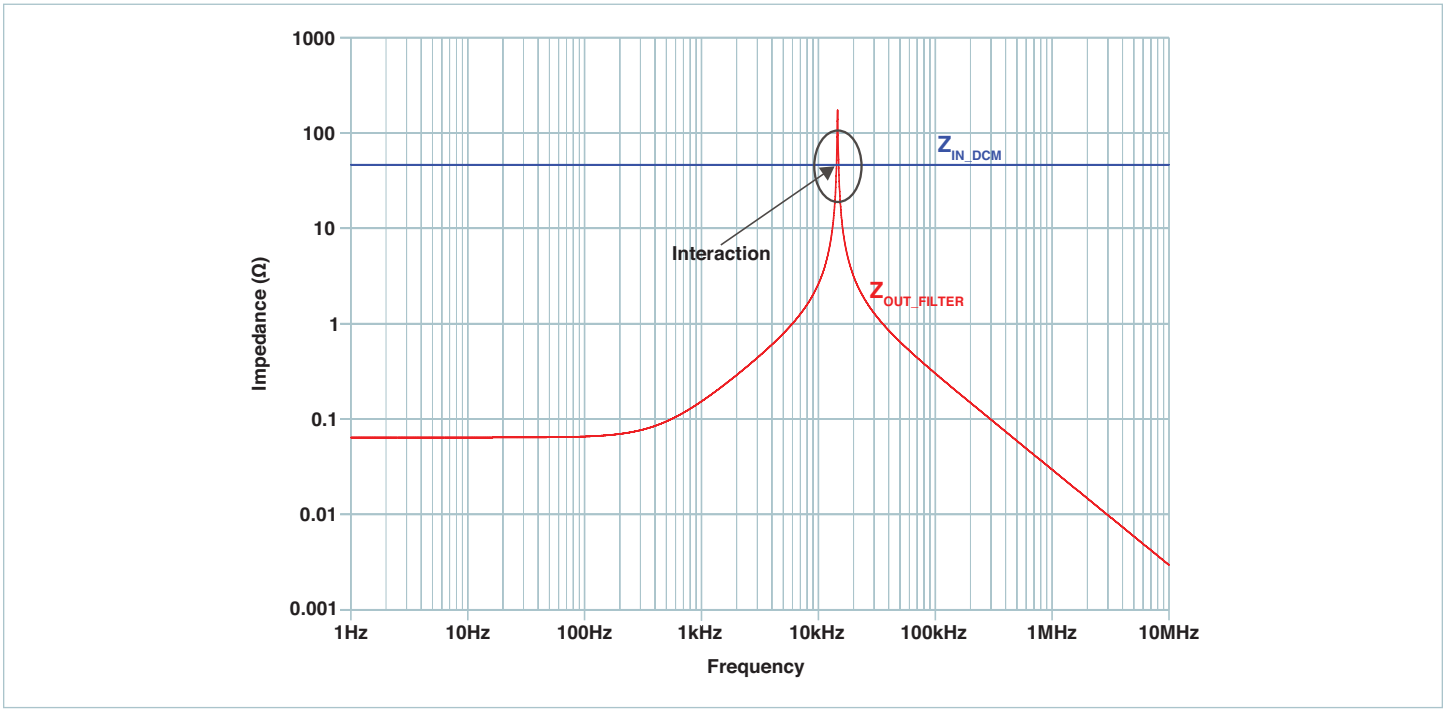


Figure 2.22a — *Output impedance of the undamped LC filter along with the DCM negative incremental input impedance*

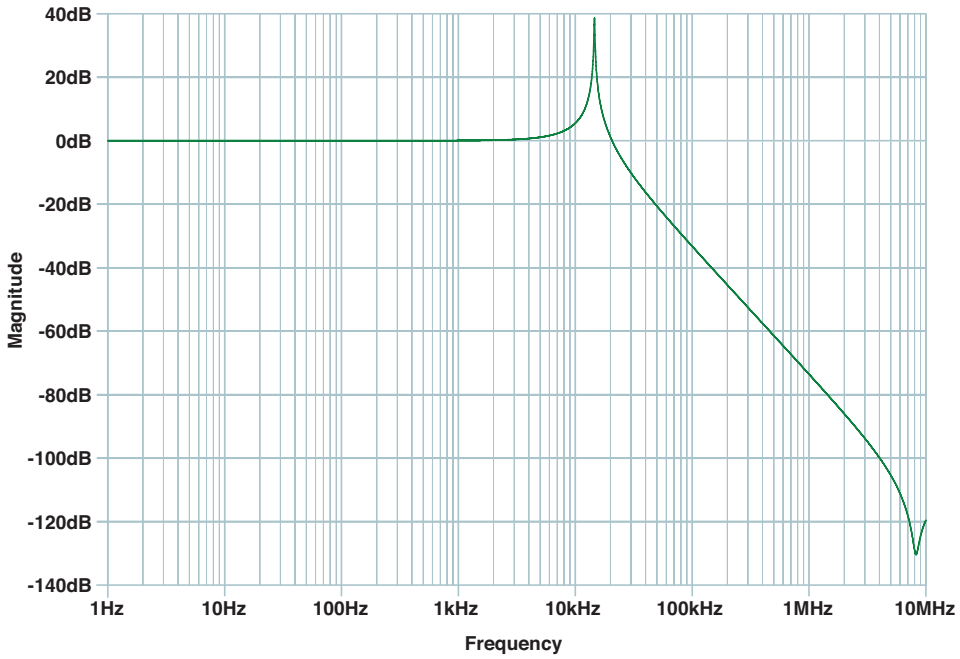


Figure 2.22b — *Voltage transfer function of the undamped LC filter*

According to the frequency response plots, shown in Figure 2.22b, the filter attenuation target is met. However, at the resonance (shown in Figure 2.22a), the output impedance of the input filter is interacting with the input impedance of the DCM. In this case, there could be potential stability issues leading to large oscillations in the input voltage. In order to avoid the instability, the peak magnitude of the output impedance must be at least ten times below the input impedance of the DCM; this can be achieved by using a proper damping scheme.

Note: Since further discussed input filter network topologies are based on the undamped LC filter network, the resonant frequency f_c of damping filter networks and roll-off will remain same.

2. Parallel-Damped Filter Network

A parallel-damped filter is obtained by connecting a parallel branch of a blocking capacitor (C_d) in series with the damping resistor (R_d) to the undamped LC filter network as shown in Figure 2.23.

The resistance R_d reduces the output peak impedance of the filter at the cutoff frequency. The capacitor C_d blocks the DC component of the input voltage, preventing excessive power dissipation from R_d. At the resonant / cutoff frequency, the capacitor C_d must have a significantly lower impedance than both the filter capacitor C_{DM} and R_d so as to not affect the cutoff frequency of the main LC filter. Therefore, the value of the blocking capacitor must be chosen to be larger in comparison to capacitor C_{DM}. The value of blocking capacitor is given by the expression $C_d = nC_{DM}$.

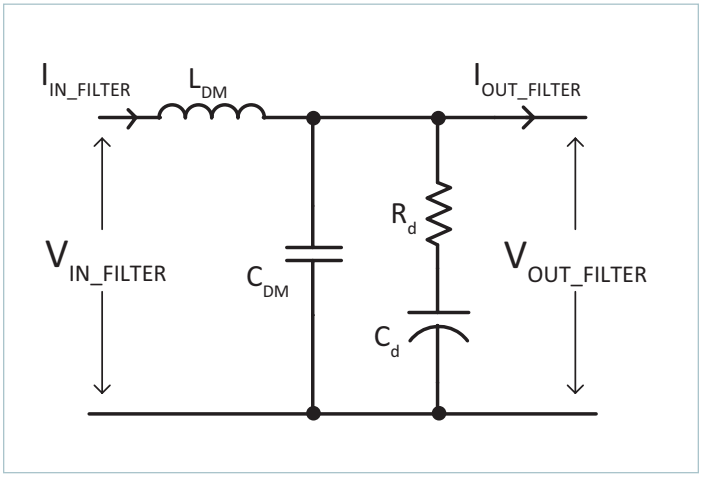


Figure 2.23 — *Damping using series resistors*

To determine the value of n and an optimum value of R_d, the value of the peak output impedance of the filter must be chosen.

The value of peak output impedance for an optimum design is given by:

$$|Z_{OUT\text{-}FLTER}| = R_O \frac{\sqrt{2(2+n)}}{n}$$

Where $R_O = \sqrt{(L_{DM}/C_{DM})}$

The value of damping resistance that leads to the optimum damping is given by:

$$R_d(optimum) = R_O \sqrt{\frac{(2+n) \bullet (4+3n)}{2n^2(4+n)}}$$

Design Example

The same filter requirements as mentioned earlier in undamped LC filter design example are again considered. In addition, the filter is designed to meet the peak output impedance ($|Z_{OUT\text{-}FLTER}|$) of 2Ω, which is more than ten times lower than the input impedance of the DCM.

$$R_O = \sqrt{\frac{22\mu H}{5.4\mu F}} = 2.0$$

$$2\Omega = 2.0 \frac{\sqrt{2(2+n)}}{n}$$

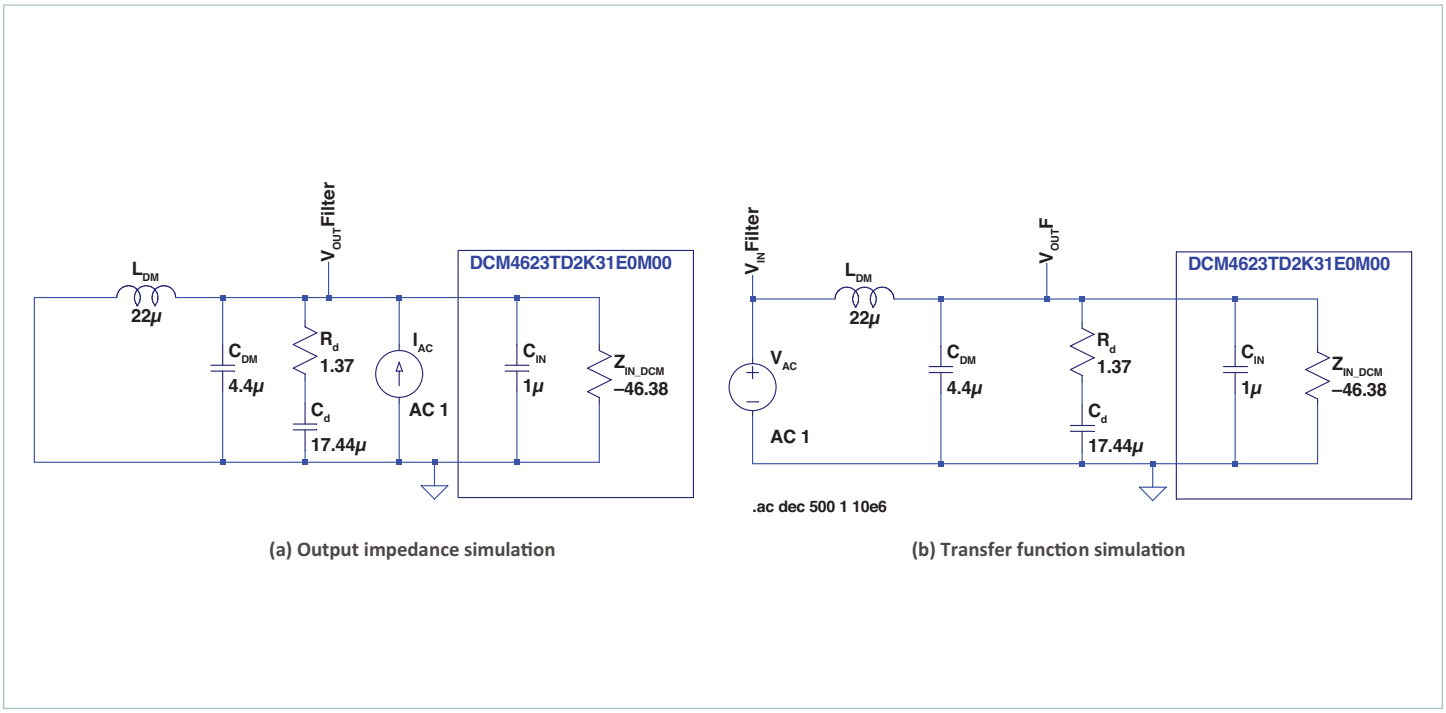
$$n = 3.23$$

Therefore,

R_d (optimum)=1.37,

C_d = 3.23(5.4µF) = 17.44µF

Simulation of the filter has been carried out in spice to verify the filter attenuation characteristics, as shown in Figure 2.24.



(a) Output impedance simulation

(b) Transfer function simulation

Figure 2.24 — *Parallel-damping filter network along with the DCM negative input impedance*

From the frequency response plots, as shown in Figure 2.25b, it can be observed that the output impedance of the filter is more than ten times below the DCM input impedance. The filter has an attenuation characteristics of –70dB at 1MHz with a roll-off of –40dB /decade.

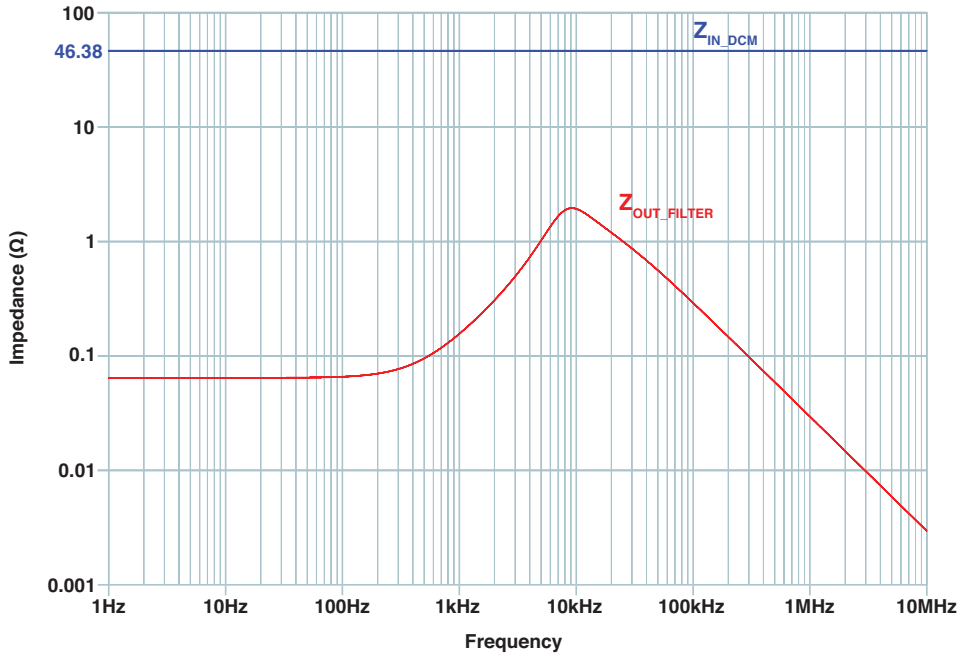


Figure 2.25a — *Output impedance of the parallel-damped filter along with the DCM negative input impedance*

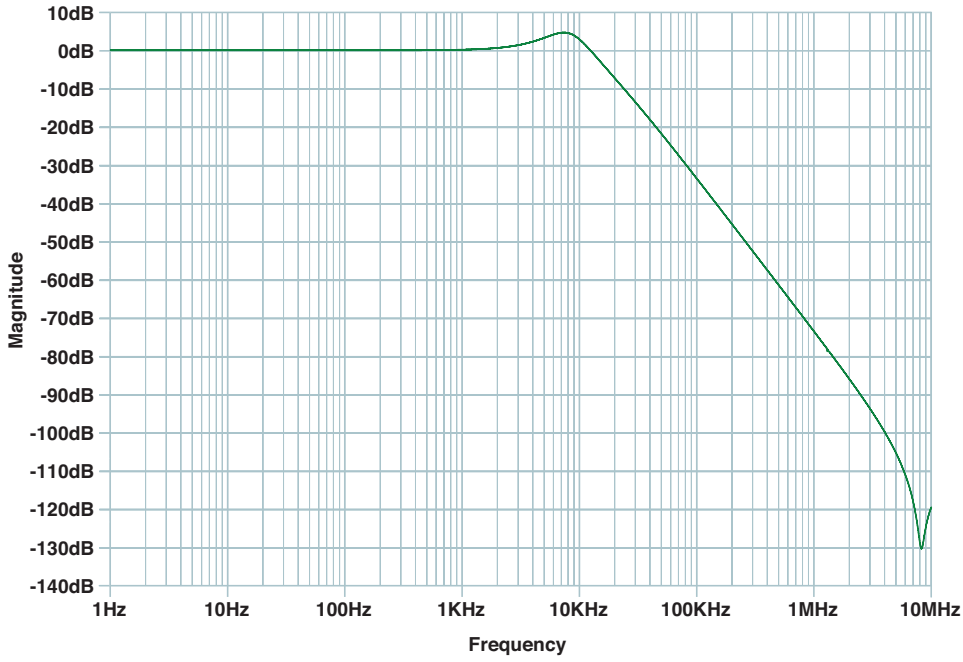


Figure 2.25b — *Voltage transfer function of the parallel-damped filter*

2a. Simplified Parallel-Damping Network

A simplified version of the parallel-damping network is shown in Figure 2.26. In order to reduce the component count of the filter shown in Figure 2.23, blocking capacitor C_d and series resistor R_d can be replaced with a capacitor that has higher value of effective series resistance (ESR). Usually aluminum electrolytic or tantalum capacitor types provide higher ESR. Therefore, the component count is reduced.

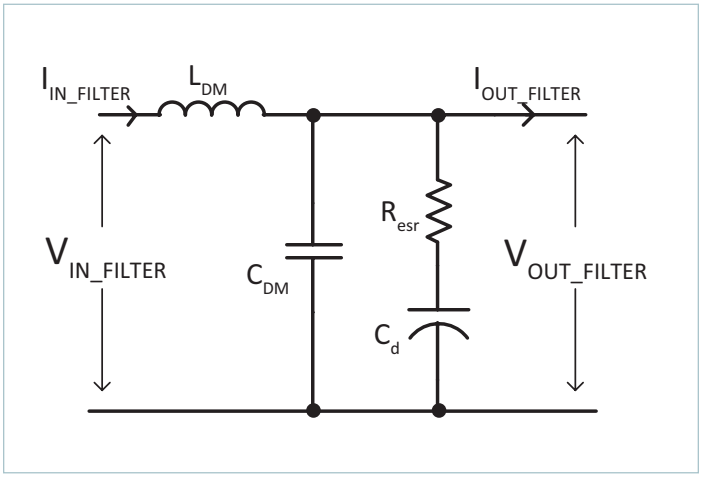


Figure 2.26 — *Simplified parallel-damped input filter network*

3. Series-Damped Filter Network

A series-damped filter is obtained by connecting a parallel branch of blocking inductor (L_b) in series with the damping resistor (R_d) with the filter inductor (L_{DM}) to the undamped LC filter network as shown in Figure 2.27. The inductor L_b causes the filter to exhibit a two-pole attenuation characteristic at high frequency.

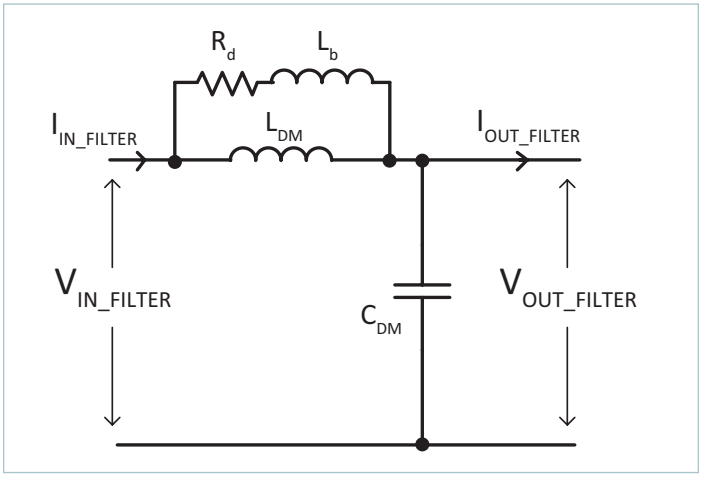


Figure 2.27 — *Series-damped input filter network*

The resistance R_d reduces the output peak impedance of the filter at the resonant frequency. The inductor L_b on the other hand blocks the DC component of the input voltage which prevents power dissipation on R_d. However, in order to allow R_d to damp the filter, the inductor L_b must have an impedance magnitude that is sufficiently smaller than R_d at the filter resonant frequency.

Therefore, the value of the blocking inductor L_b must be chosen to be smaller as in comparison to filter inductor L_{DM}. The value of the blocking inductor is given by the expression $L_b = nL_{DM}$.

The value of peak output impedance for an optimum design is given by:

$$|Z_{OUT\text{-}FLTER}| = R_O\sqrt{2n(1+2n)}$$

Where

$$R_O = \sqrt{(L_{DM}/C_{DM})}$$

The value of damping resistance that leads to the optimum damping is given by:

$$R_d(optimum) = R_O\sqrt{\frac{n(3+4n)(1+2n)}{2(1+4n)}}$$

Design Example

Again, the attenuation characteristics similar to that of design example of undamped LC filter are considered. To determine the value of n and an optimum value of R_d, the value of the peak output impedance ($|Z_{OUT\text{-}FLTER}|$) of the filter is assumed to be 2Ω, which is ten times lower than the input impedance of the DCM.

$$R_O = \sqrt{\frac{22\mu H}{5.4\mu F}} = 2.0$$

$$2\Omega = 2.0\sqrt{2n(1+2n)}$$

$$n = 0.309$$

Therefore,

$R_{d\text{-}optimum}$ = 1.37,

L_b = 0.309(22µH) = 6.798µH

To verify the filter attenuation characteristics, simulation of the filter has been carried out using spice as shown in Figure 2.28.

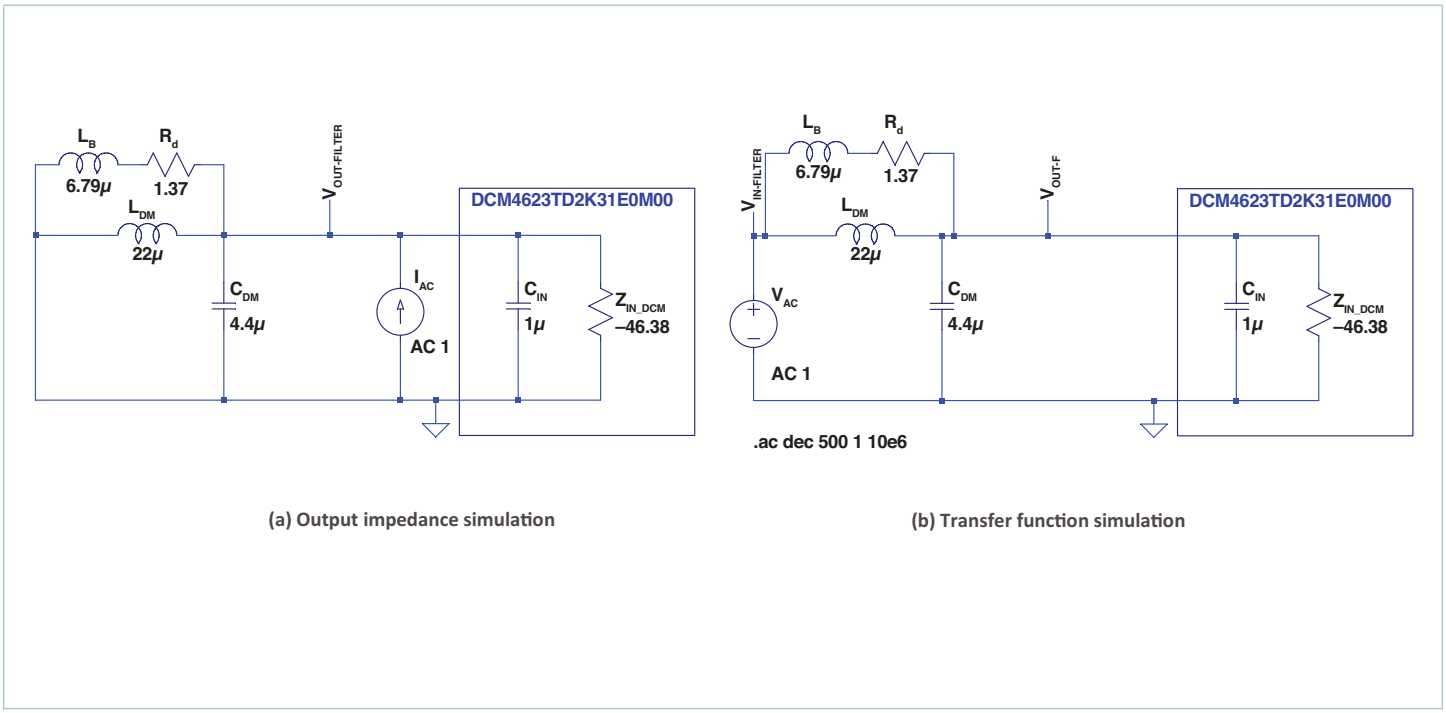


Figure 2.28 — *Series-damping filter network along with the DCM negative input impedance*

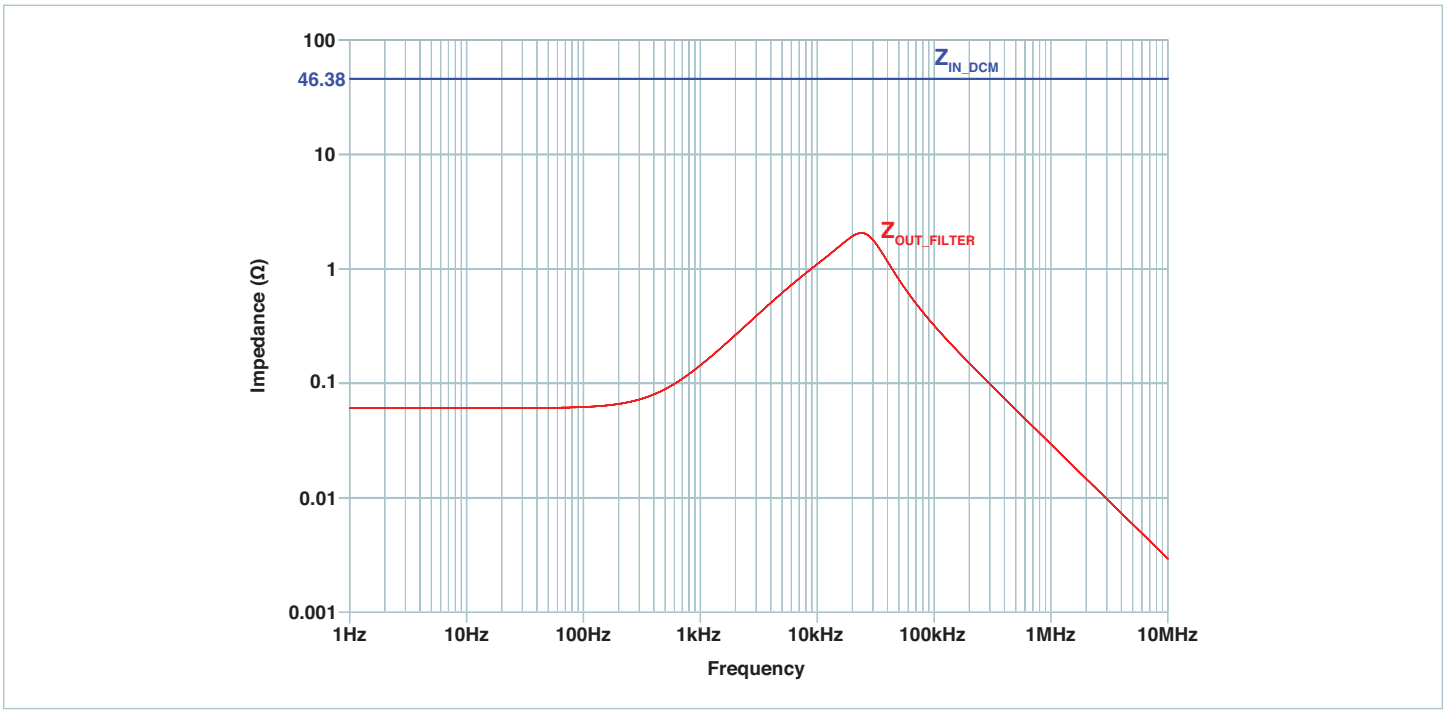


Figure 2.29a — *Output impedance of the series-damped filter along with the DCM negative input impedance*

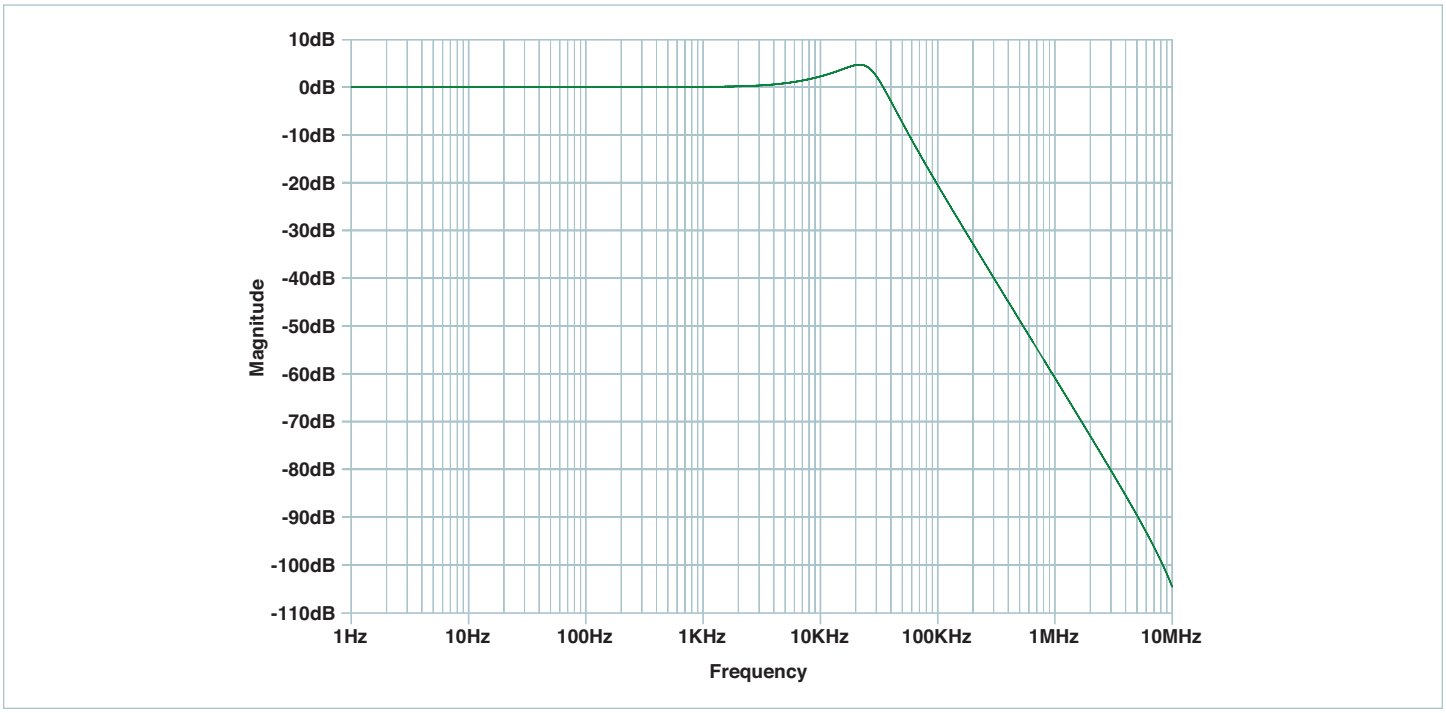


Figure 2.29b — *Voltage transfer function of the series-damped filter*

From the output impedance vs. frequency curve shown in Figure 2.29a, it can be observed that the output impedance of the filter is more than ten times below the DCM input impedance. The filter has an attenuation characteristics of –60dB at 1MHz with a roll-off of –40dB / decade.

4. Simplified Series-Damping Filter Network

A simplified series-damped filter is obtained by connecting a parallel branch of damping resistor (R_d) with the filter inductor (L_{DM}) to the undamped LC filter network as shown in Figure 2.30. Ideally, a simplified series-damped LC filter must provide a second order roll-off of –40dB / decade. However, the problem with this circuit is that its transfer function contains a high-frequency zero $f_z = R_d/(2\pi L_{DM})$. Therefore, addition of damping resistor R_d degrades the slope of the high-frequency asymptote, from –40 dB / decade to –20dB / decade. Hence, this circuit is effectively a single-pole RC low-pass filter with no attenuation provided by inductor L_{DM}.

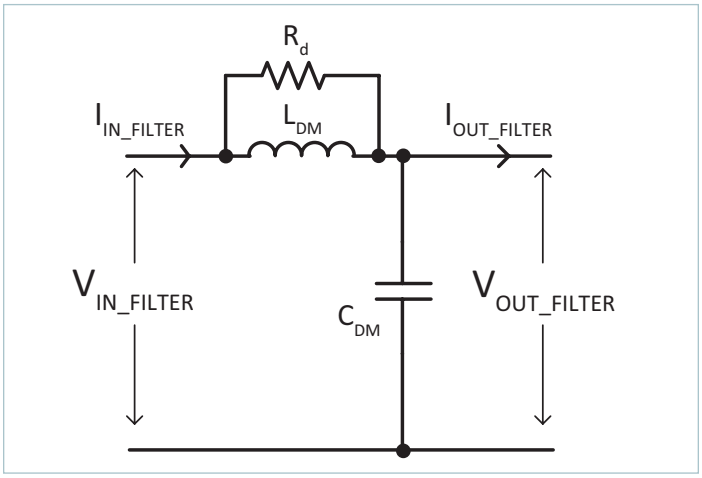


Figure 2.30 — *Simplified series-damped input filter network*

Design example

The attenuation characteristics from the design example of undamped LC filter are again considered. The simulation of simplified series-damped filter has been carried out using spice simulation tool, shown in Figure 2.31. The value of R_d is chosen to be 1.3Ω in order to keep the peak of the filter output impedance less than 2Ω. From the frequency response plots shown in Figure 2.31a. It can be observed that the output impedance of the filter is more than ten times below the DCM input impedance, but due to the presence of high-frequency zero the filter attenuation characteristics are degraded to –33dB at 1MHz with a roll-off of –20dB / decade, shown in Figure 2.32a.

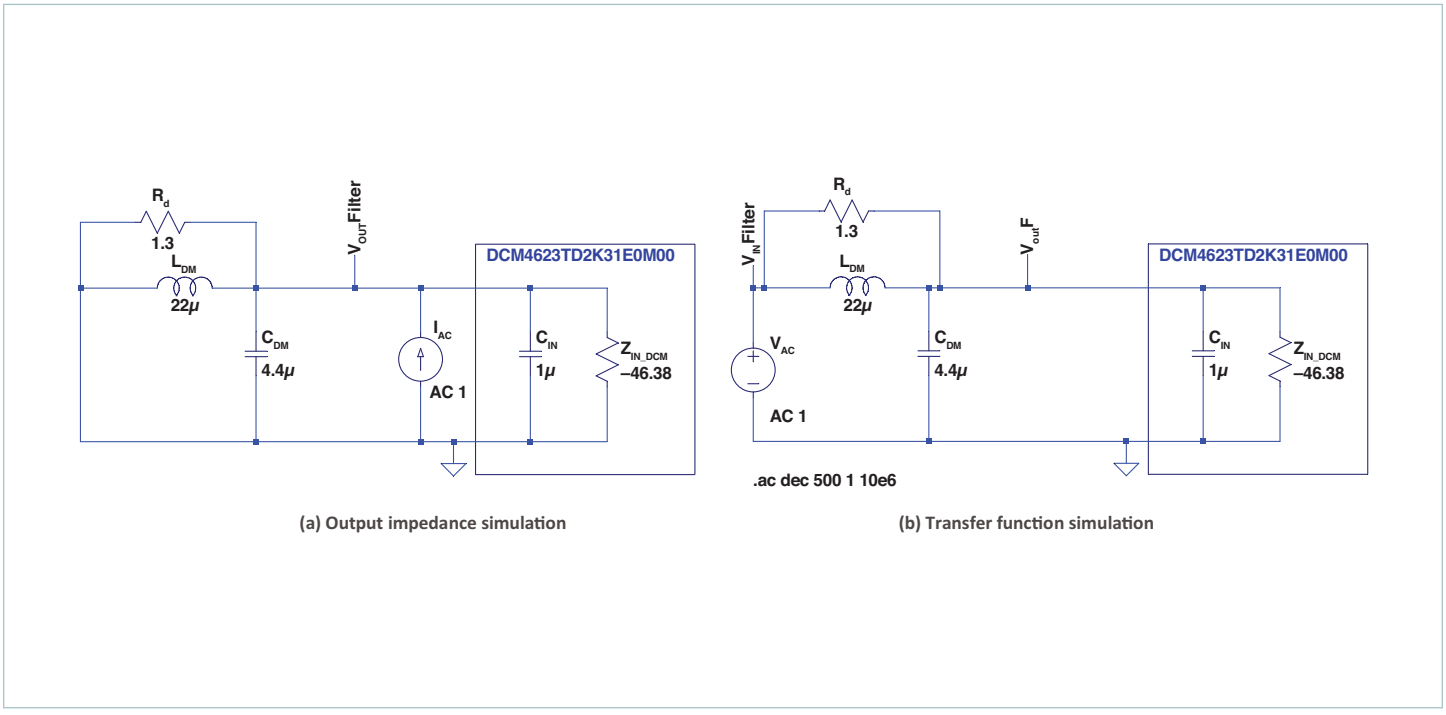


Figure 2.31 — *Simplified series-damping filter network along with the DCM negative input impedance*

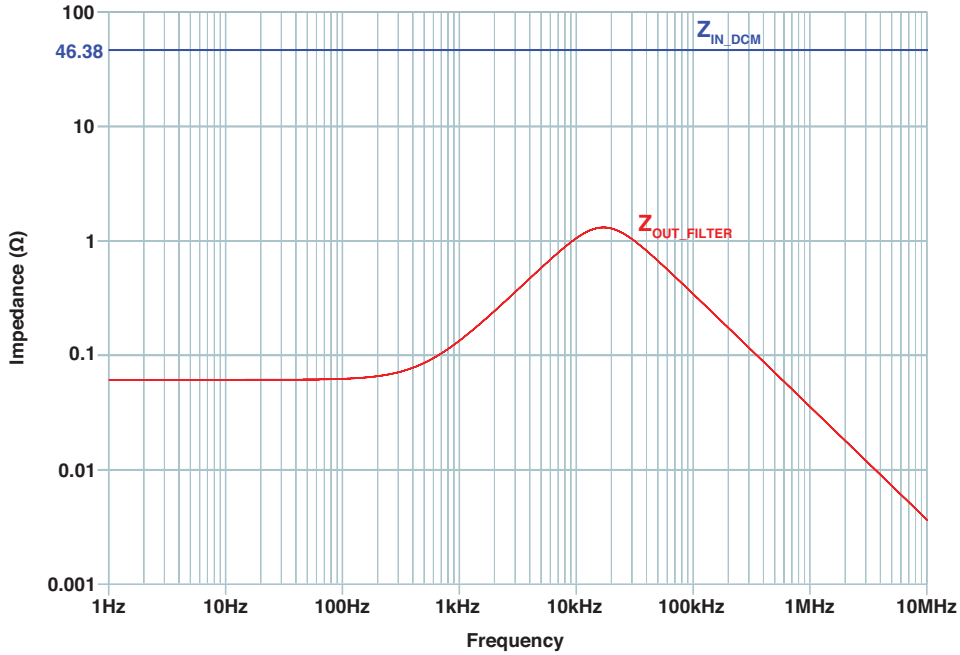


Figure 2.32a — *Output impedance of the simplified series-damped filter along with the DCM negative input impedance*

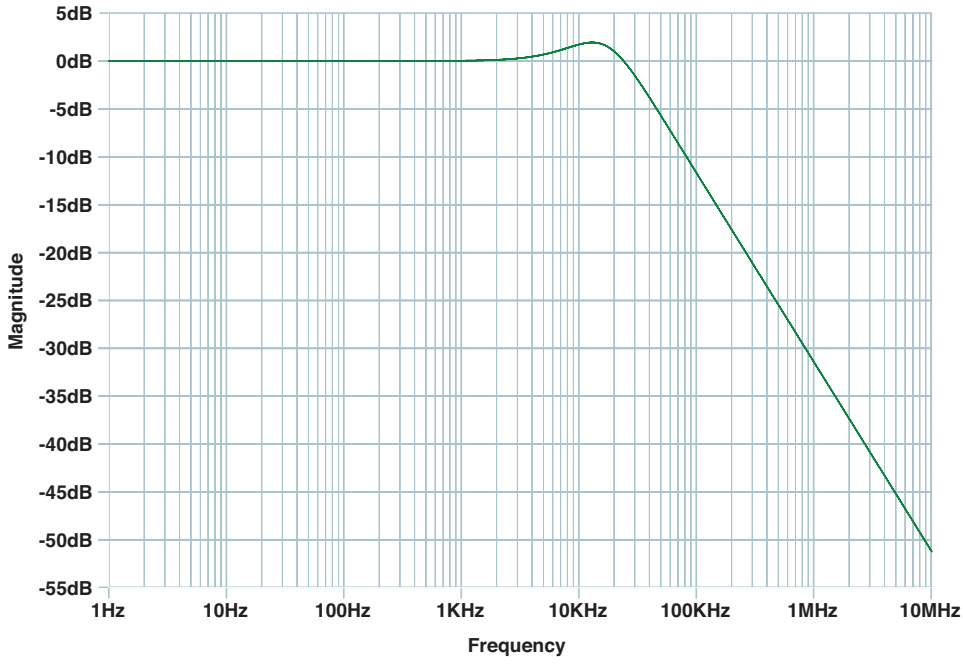


Figure 2.32b — *Voltage transfer function of the simplified series-damped filter*

Application of Filters for Differential-Mode Noise Reduction

To demonstrate the attenuation characteristics of the input filter, a standalone DCM prototype is built and input current of the DCM is measured with and without using the parallel-damped input filter.

Measurement of Input Currents without an Input Filter

A standalone DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) prototype, shown in Figure 2.33 is used to understand the noise signature in the DCM input currents. The current is measured at the input of the DCM (I_{IN_DCM}) at full load (17.86A) with an input voltage of 160V_{DC}.

The measurement of the input current is shown in Figure 2.34, it can be noticed that the DCM is injecting the high-frequency noise currents into the power source , the RMS amplitude of the input noise currents is 131mA. These switching noise currents can interfere with the systems that are connected to the same source, can lead to malfunction of the DCM or the other systems connected to the source V_{IN}; Therefore, an input filter is required to attenuate the switching noise currents.

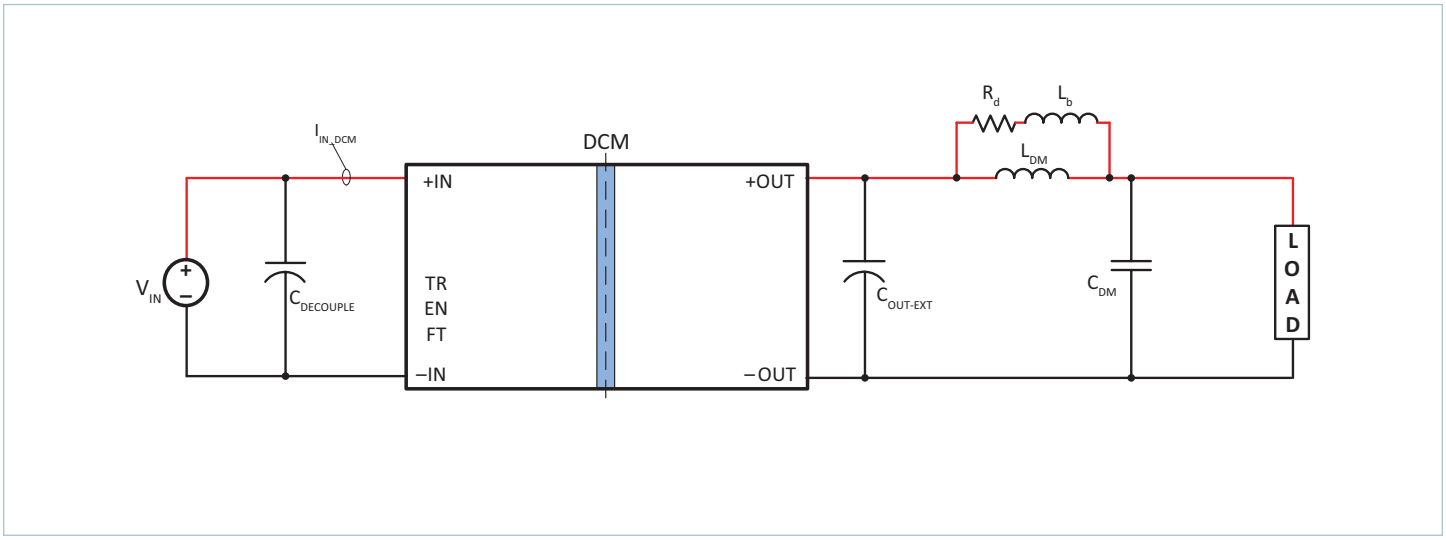


Figure 2.33 — *DCM without an input filter*

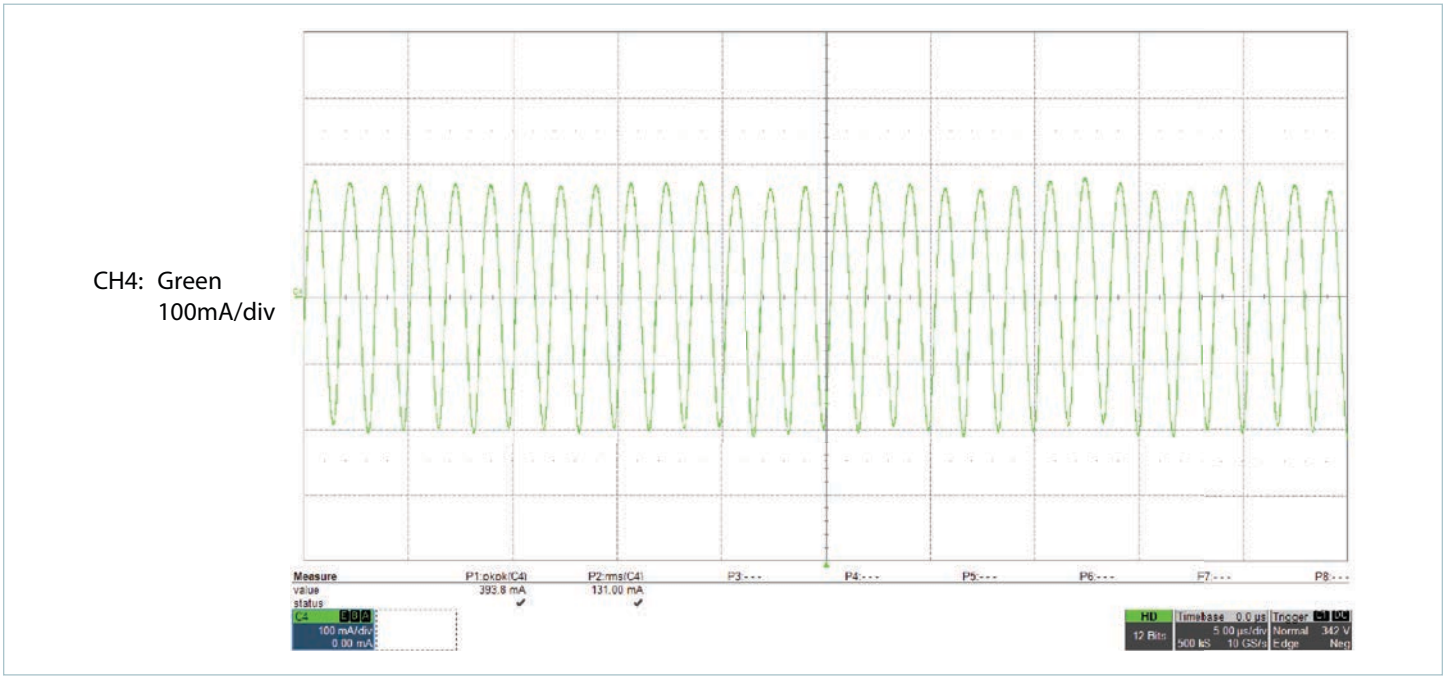


Figure 2.34 — *Input current of the DCM, without an input filter*

Measurement of Input Currents with a Parallel-Damped Input Filter

A standalone DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) prototype, shown in Figure 2.33 is modified by adding the two-stage parallel-damped input filter to demonstrate the attenuation of the input noise currents. The modified circuit is shown in Figure 2.35, the filtering component values used in the prototype are:

L_{DM} = 15µH (PN: SRP1038A-150M),
C_{DM} = 3 • 2.2µF (PN: C5750X6S2W225K250KA),
R_d = 1.2Ω,
C_d = 6 • 2.2µF (PN: C5750X6S2W225K250KA) and
L_{DM_1} = 220nH.

The input currents are measured at the filter input ($I_{IN\_FILTER\_IN\_DCM}$) when DCM is operating at full load (17.86A) with an input voltage of 160V_{DC}.

When an external filter capacitors are placed at the input of the DCM, a tank circuit is created between the filter capacitors and the internal input capacitors, which may cause high-frequency input current and voltage oscillations. High-frequency oscillation currents at the input of the DCM can create high dV/dt at the input leads of the DCM under certain operating conditions (such as transient operating conditions). High-frequency noise currents can also cause stress on the filter capacitor and DCM internal bypass capacitors, which may lead to degradation of life of the capacitors and DCM. Therefore, in order to avoid high-frequency oscillations an inductor L_{DM_1} is added in between the filter capacitor C_{DM} and damping branch R_d-C_d. This is effectively a two stage filter configuration, which reduces the AC ripple currents from changing rapidly over a short period of time. The value of L_{DM_1} is chosen to be a small value of inductance (200nH).

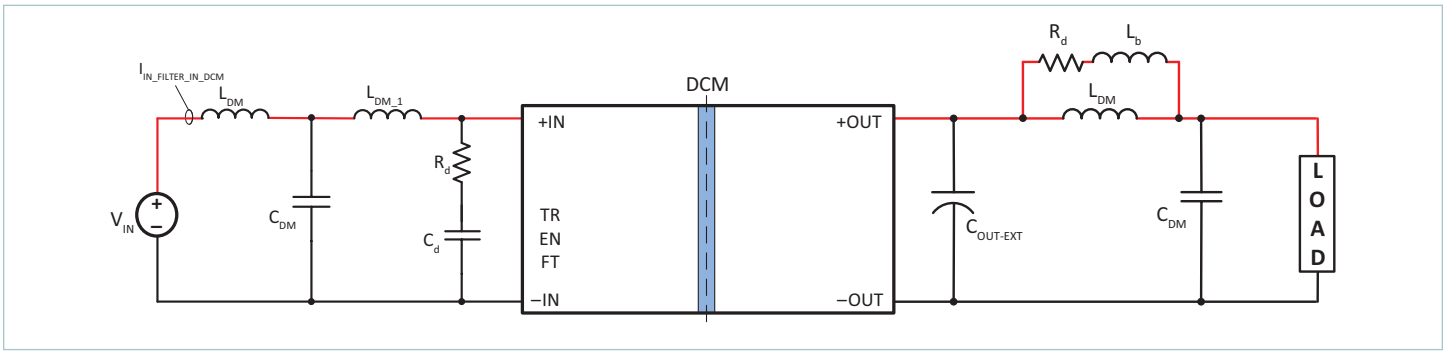


Figure 2.35 — *DCM with a two-stage parallel-damped input filter*

The noise current amplitudes at the input of the EMI filter ($I_{IN\_FILTER\_IN\_DCM}$) are well attenuated using the two-stage input filter, the input current drawn from the power source is smooth , shown in Figure 2.36. The AC ripple current at the filter input is measured as the RMS amplitude of 4.19mA.

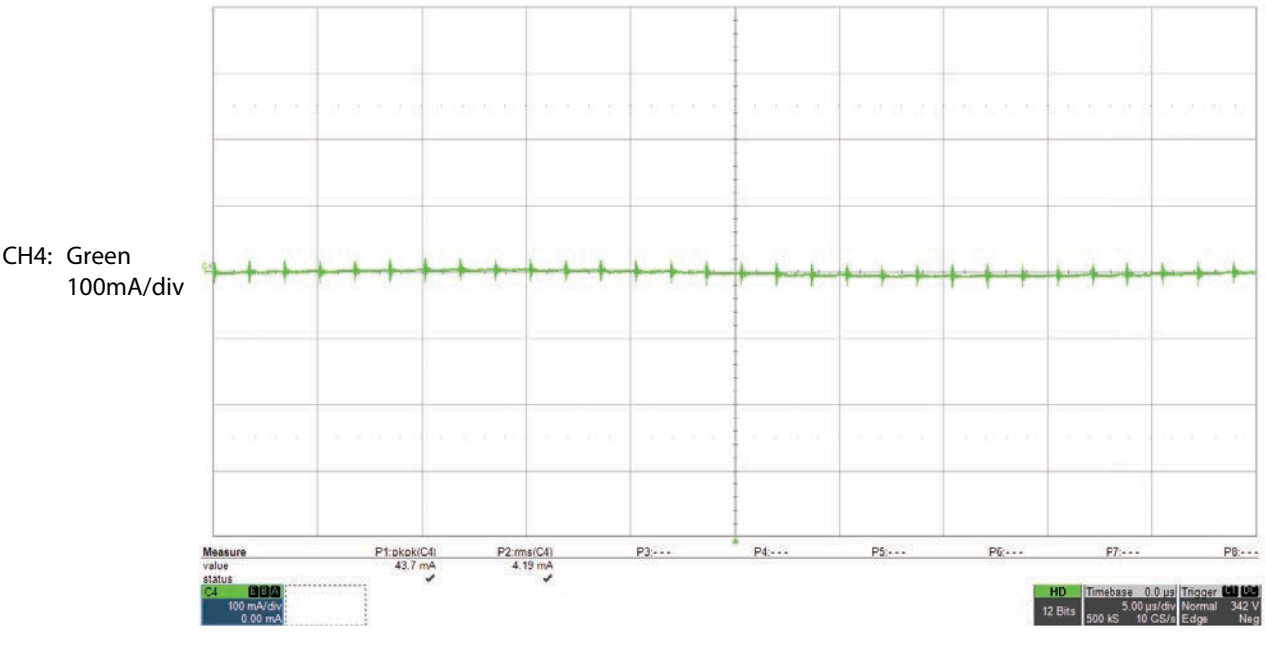


Figure 2.36 — *Input current of the DCM, with an input filter*

Common-Mode Input Filter Design

As discussed in the introduction of the input filter design section, switching power supplies, including the DCM, generate common-mode noise. Common-mode noise currents arise due to the presence of parasitic circuit capacitances, including the capacitance coupling between the primary-side MOSFETs drain to the EMI ground plane or chassis and the transformer primary to secondary winding capacitance. During the switching of the power MOSFETs, a high dV/dt across the parasitic capacitance coupling between the MOSFET drain to the EMI ground plane is generated; this change in voltage injects noise currents into the common-mode path. The common-mode noise currents propagate to the power source through the positive and negative input terminals, closing the loop through the ground plane as shown with red arrows in Figure 2.37. The noise currents are equal in magnitude and in phase with each other.

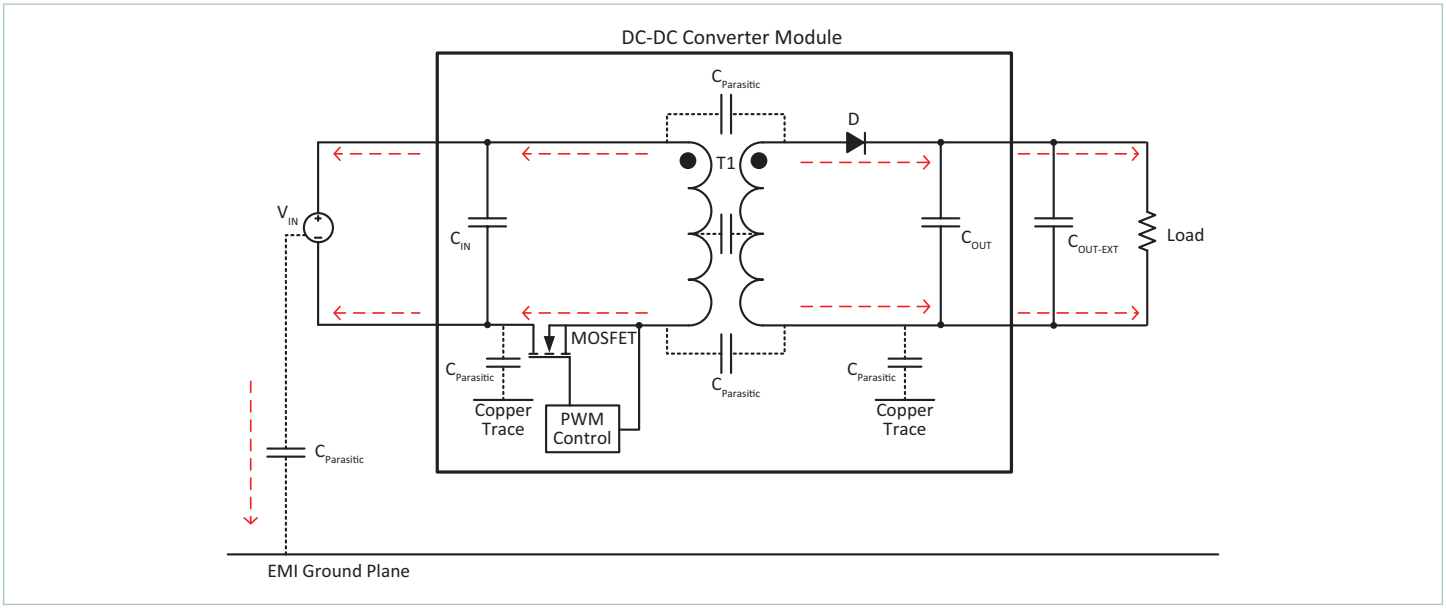


Figure 2.37 — *Common-mode noise currents path*

Noise Mitigation Techniques

Common-mode noise currents can be attenuated by placing a high impedance in series with positive and negative input conductors and a low impedance from each input conductor to the EMI ground.

A typical common-mode input filter is shown in Figure 2.38 and consists of a common-mode choke (T1), Y-capacitors (C_{Y1-4}), X-capacitors ($C_{X1, 2}$) and damping network (R_d, C_d). The filter output is connected to the DCM input and the filter input is connected to the upstream supply, as shown in Figure 2.39. Common-mode choke inductance provides a high impedance path in series to the common-mode noise generated by the DC-DC converter and the Y-capacitors provide a low-impedance path to the EMI ground. Therefore, Y-capacitors must be physically placed close to the input terminals of the DC-DC converter, which minimizes the trace impedance. An ideal common-mode choke provides common-mode inductance as a result of the direction of common-mode noise currents. The differential-mode noise currents are opposite in each winding and all the magnetic flux in the core cancels. However, in practical cases, CM choke presents leakage inductance or differential mode inductance as a result of imperfect coupling between the two windings i.e., the magnetic flux produced by one winding will not couple with the other winding. A typical value of leakage inductance is 1 – 1.5% of common-mode inductance. A differential mode filter network can be formed by using the leakage inductance and the X-capacitor (C_{X2}). As a result, the common-mode filter provides some degree of attenuation to the differential mode noise.

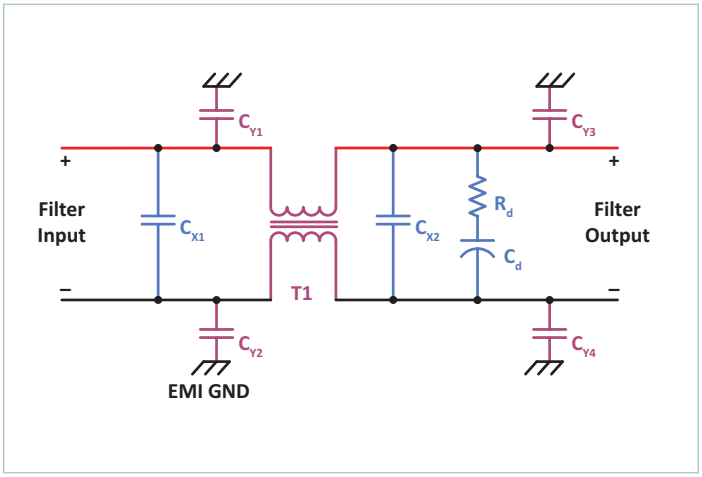


Figure 2.38 — *A typical common-mode noise filter circuit*

Common-Mode Noise Filter Design Steps

1. Determine the AC ripple magnitude (both the differential mode noise and common-mode noise) over the frequency range of interest using the EMI spectrum analyzer and compare the measured AC ripple magnitude with the EMI standard limit line.
2. Determine the required differential-mode and common-mode noise attenuation and define the differential-mode and common-mode filter corner frequencies.
3. Select the common-mode choke such that it offers a high impedance over a frequency range of the common-mode noise.
4. Calculate the amount of Y-capacitance required to meet the filter attenuation characteristics.

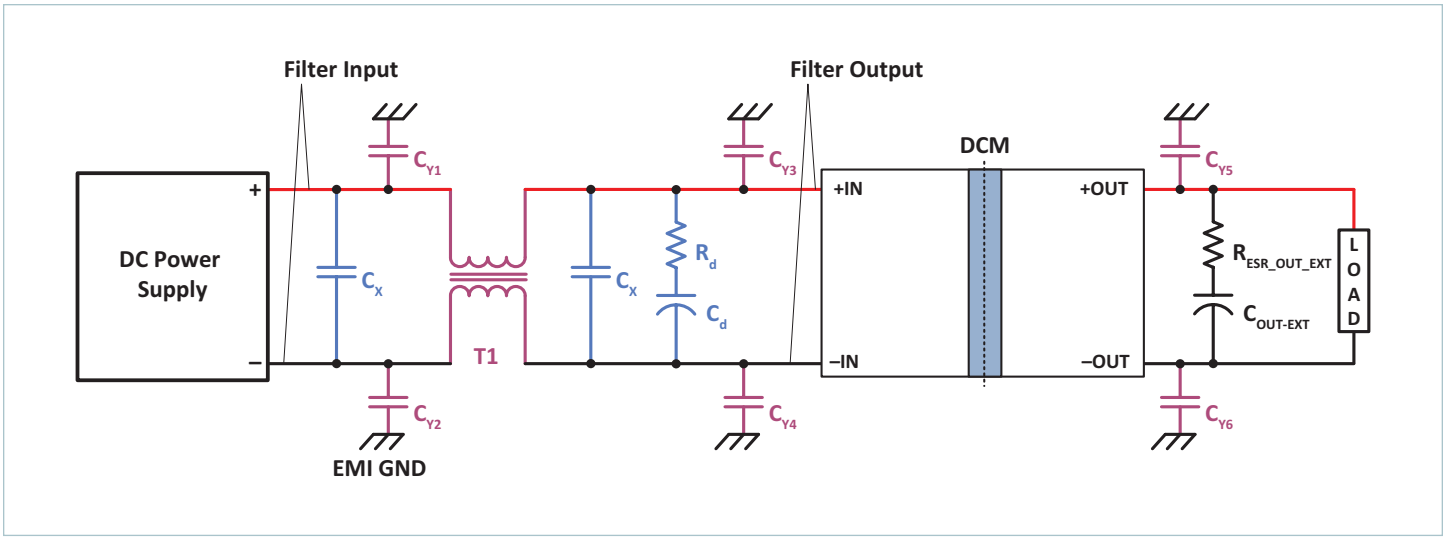


Figure 2.39 — *A typical application of common-mode noise filter*

This section provides a detailed discussion of the operation of ChiP DCMs, which fall into one of two series of parts:

- **DCMxxxxxxxxxxx00** series (Array-mode DCMs);
- **DCMxxxxxxxxxxx70** series (Enhanced V_{OUT} regulation mode DCMs);
- **DCMxxxxxxxxxxx60** series (Dual-mode DCMs)

In applications where required power is greater than a ChiP DCM's maximum output power, DCMxxxxxxxxxx00 series (array-mode DCMs) modules can be used in parallel. Array-mode ChiP DCMs use inherent droop characteristics to share the load current among modules when connected in parallel. Array-mode ChiP DCMs do not require any additional external circuitry to share the load current.

In applications where required power is less than or equal to a ChiP DCM's maximum output power, DCMxxxxxxxxxx70 series (enhanced V_{OUT} regulation mode DCMs) models optimized for standalone operation can be used.

The DCMxxxxxxxxxx60 series (dual-mode DCMs) offers both array-mode and enhanced V_{OUT} regulation mode operation in the same module. The mode of operation can be selected based on the EN pin voltage during the input voltage start up of the DCM. For more information on the mode selection, please refer to the section on control pin functions and the data sheet.

Pin Configuration

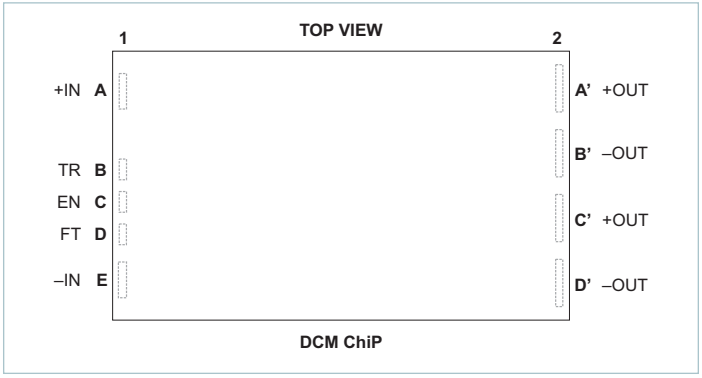


Figure 3.1 — *Pin configuration*

Control Pin Functions

The control features of the DCM includes output voltage trimming, enable / disable control and fault monitoring. This can be attained by three control pins; TR, EN and FT. The DCM control pins are implemented by using the general purpose input / output (GPIOs) pins of the micro-controller. Each control pin is pulled up to internally generated voltage (V_{CC}) of 3.3V through a pull-up resistor and are referenced to the negative input terminal –IN as shown in Figure 3.2. Each control pin has a simple internal bias and drive structure which is maintained throughout the various operating modes. The logic thresholds, bias levels and bias strengths for the control input pins do not change during start up or fault-protection conditions. In general, the control pins can all be left unconnected to select their default function.

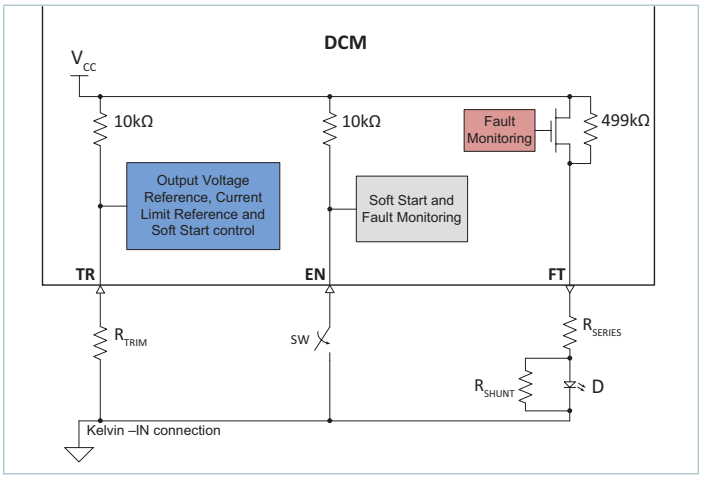


Figure 3.2 — *Internal structure of control pins*

Pin Descriptions

Pin Number	Signal Name	Type	Function
A1	+IN	INPUT POWER	Positive input power terminal
B1	TR	INPUT	Enables and disables trim functionality; adjusts output voltage when trim active
C1	EN	INPUT	***DCMxxxxxxxxxxx00 & DCMxxxxxxxxxxx70 series:*** Enables and disables power supply
			DCMxxxxxxxxxxx60 series: Dual function **1.** Enables either array or enhanced V_{OUT} regulation mode **2.** Enables and disables the power supply
D1	FT	OUTPUT	Fault monitoring
E1	–IN	INPUT POWER RETURN	Negative input power terminal
A'2, C'2	+OUT	OUTPUT POWER	Positive output power terminal
B'2, D'2	–OUT	OUTPUT POWER RETURN	Negative output power terminal

Output Voltage Trimming (TR Pin) (Applies to all DCM Series)

The TR pin selects the trim mode during start up and allows adjusting the output voltage of the converter based on the TR pin voltage. The TR pin voltage can be programmed via fixed resistors, potentiometers or external voltage signal. The TR pin is pulled to internally generated 3.3V (V_{CC}) using a 10kΩ (R_{TRIM_INT}) pull-up resistor, shown in Figure 3.2. The TR pin is sampled one time at start up, after V_{IN} exceeds V_{IN_UVLO+}. TR voltage at that time determines the function of TR for as long as the DCM is supplied with input voltage.

If TR is greater than the trim disable threshold V_{TRIM_DIS} when it is sampled, the DCM will latch in non-trim mode. This is also the case when TR is left open. An internal pull-up resistor 10kΩ pulls TR up to 3.3V selecting the non-trim mode of operation. In this mode, the programmed trim condition will simply be the rated nominal V_{OUT} of the DCM model.

If TR is sampled below the minimum trim enable threshold V_{TRIM_EN}, the trim function will be enabled and TR will control the output voltage as long as V_{IN} is applied. If the powertrain is disabled with EN or stopped by a fault condition, it retains the trim mode which was previously latched in when it resumes operation. The trim mode is re-evaluated only after removing and reapplying the input voltage to the DCM.

The maximum allowed trim range is –40% to +10% of the nominal output voltage V_{OUT_NOM}. The percentage trim range varies from model to model. Please refer to the model data sheet for output voltage trim range. The functional range of the TR pin is given by V_{TRIM_RANGE}. The minimum and maximum value of functional trim range is set at the extreme limits so as to guarantee the performance of the converter within the normal operating trim range. Operating the converter above the maximum trim range value may result in incorrect operation. Performance specifications in the data sheet are not guaranteed.

The relationship between the trim pin voltage V_{TR} and the trim resistor is given by the Equation 3.1.

$$V_{TR} = V_{CC}\left(\frac{R_{TRIM}}{R_{TRIM} + R_{TRIM\_INT}}\right) \qquad 3.1$$

TR allows dynamic trim control of the output voltage with at least 30Hz of –3dB control loop bandwidth.

In trim active mode (at full load and room temperature), the relationship between the output voltage set point V_{OUT} and trim pin voltage V_{TR} is linear. For example, the output voltage of DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) model is given by the Equation 3.2.

$$V_{OUT\text{-}FL} @ 25°C = 11.64 + \left(21.909 \bullet \frac{V_{TR}}{V_{CC}}\right) \qquad 3.2$$

The constants in the above equation are model specific. Please refer to the appropriate data sheet. Vicor provides an online tool for trim resistor and trim voltage calculations, please refer to the DCM Trim Calculator in Tools / Calculators.

The DCM has an internal current limit. When the output voltage is trimmed at or below the V_{OUT_NOM} nominal value, the converter output current is limited by the maximum average output power. Similarly, when the output voltage is trimmed above the nominal value, the internal current limit threshold will be decreased proportionally to maintain the maximum average output power.

TR Pin Considerations

For protection from external noise, the TR pin should be equipped with a low-pass filter network as shown in the Figure 3.3. $R_{D\_TR\_x}$ is provided for damping the resonant peak caused by the external capacitor and lead inductance. A minimum value of 300Ω is recommended for $R_{D\_TR\_x}$, use 100nF for C_{TRF_x}. The total trim resistor value should account for $R_{D\_TR\_x}$, i.e., calculated trim resistor = $R_{D\_TR\_x}$ + R_{TRIM_x}.

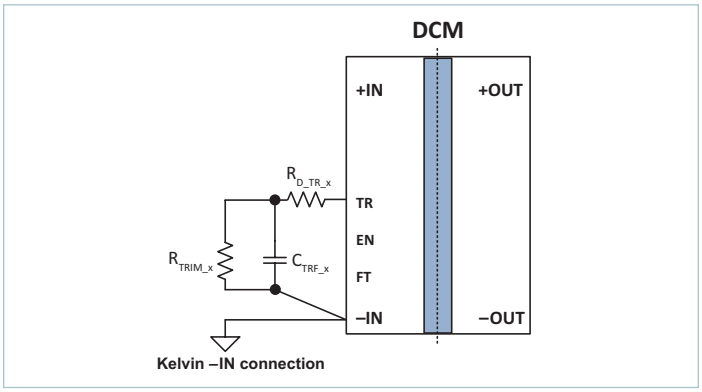


Figure 3.3 — *Filter network for TR Pin*

Enable / Disable Control (EN Pin)

DCMxxxxxxxxxx00 and DCMxxxxxxxxxx70 Series

EN pin is a digital input that enables and disables the output of the converter by controlling the powertrain. The EN pin is referenced to the –IN pin of the converter. EN is an input only; it does not pull low in the event of a fault. Use an open-collector transistor, MOSFET or Opto-coupler to control this pin. The EN pin is pulled to internally generated 3.3V (V_{CC}) using a 10kΩ (R_{ENABLE_INT}) pull-up resistor, shown in Figure 3.2.

- *Enable/Disable Control*
  - Output enable: when EN is allowed to pull up above the enable threshold (V_{ENABLE_EN}), the module will be enabled. If leaving EN floating at start up, it is pulled up to V_{CC} and the module powertrain will be enabled.
  - Output disable: EN may be pulled down externally below V_{ENABLE_DIS} (0.99V) disable threshold value in order to disable the module.
  - The EN pins of multiple units should be driven high concurrently to permit the array to start into maximum rated load. However, the direct interconnection of multiple EN pins requires additional considerations, as discussed in the section on Array Operation.

To protect from the high-frequency noise interference, the EN pin should be equipped with a low-pass filtering network as shown in Figure 3.4. $R_{D\_EN\_x}$ is provided for damping the resonant peak caused by the external capacitor and the lead inductance. Use the following for the filtering components:
$R_{D\_EN\_x}$ = 330Ω
C_{ENF_x} = 100nF
R_{ENF_x} = 1kΩ

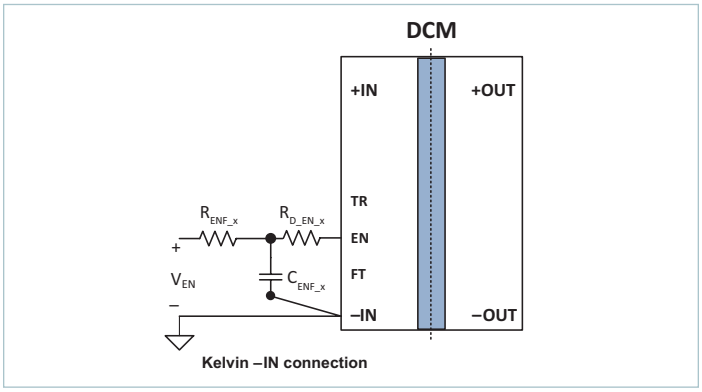


Figure 3.4 — *Filter network on the EN Pin*

DCMxxxxxxxxxx60 Series

The EN pin provides two functionalities:

- Enables Array mode or Enhanced V_{OUT} Regulation mode.
- Enables and disables the DCM converter.

The EN pin is referenced to the –IN pin of the converter. It has an internal pull up to V_{CC} through a 10kΩ resistor. EN is an input only; it does not pull low in the event of a fault.

- ***Selecting Array Mode or Enhanced V_{OUT} Regulation Mode***
  The EN pin can be used to enable or disable array mode operation or Enhanced V_{OUT} Regulation mode operation. The DCM can be configured to operate either in Array mode or in Enhanced V_{OUT} Regulation mode by setting the voltage on the EN pin at application of V_{IN} (i.e., when $V_{IN} < V_{IN\text{-}INIT}$); see Figure 3.5 for EN pin voltage thresholds. The DCM will latch in selected mode of operation once V_{IN} exceeds $V_{IN\text{-}INIT}$ and persist in that same mode until loss of input voltage.
  - At application of V_{IN} (i.e., when $V_{IN} < V_{IN\text{-}INIT}$), if the EN pin is left floating or pulled to Array mode enable threshold voltage, $V_{ARRAY\text{-}EN\text{-}TH}$, DCM operates in Array mode.
  - At application of V_{IN} (i.e., $V_{IN} < V_{IN\text{-}INIT}$), if the EN pin is pulled to Enhanced V_{OUT} Regulation mode enable threshold voltage, $V_{REG\text{-}EN\text{-}TH}$, DCM operates in Enhanced V_{OUT} Regulation mode.

Note that the selected mode of operation is not changed when a DCM recovers from any fault condition.

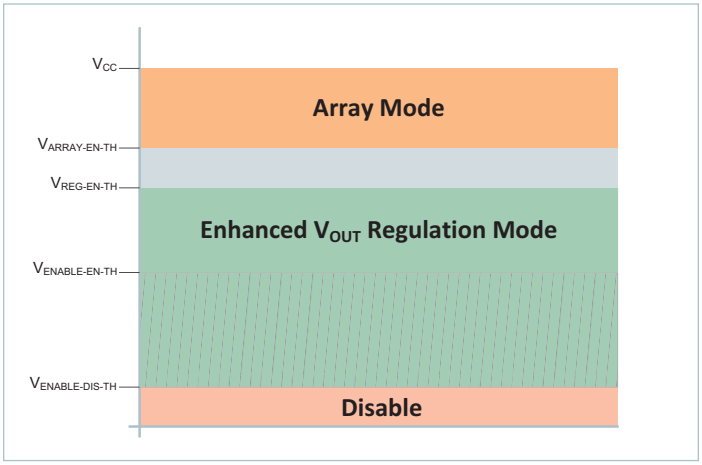


Figure 3.5 — *EN pin voltage thresholds for DCMxxxxxxxxxx60 series*

- *Enable/Disable Control*
  - Output enable: when EN is allowed to pull up above the enable threshold ($V_{ARRAY\_EN\_TH}$), the module will be enabled. If leaving EN floating, it is pulled up to V_{CC} and the module will be enabled.
  - Output disable: EN may be pulled down externally in order to disable the module.
  - The EN pins of multiple units should be driven high concurrently to permit the array to start into maximum rated load. However, the direct interconnection of multiple EN pins requires additional considerations, as discussed in the section on Array Operation.

Fault Monitoring (FT Pin) (Applies to all DCM Series)

FT is the positive-true output generated by the internal Fault Monitoring circuit. During the soft start process of the output voltage of the DCM, state of FT signal is unknown.

When the output finishes the soft start process or when the module is enabled and no fault is present, the FT pin does not have the current drive capability.

When the DCM activates fault protection, the FT pin is driven high (to 3.3V) by a low-impedance driver. This configuration helps avoid the need for the system to generate a separate low-voltage supply for powering the fault pin monitoring circuit, since a simple opto-coupler can be entirely driven from the FT pin.

Module may be damaged from an overcurrent FT drive, thus a resistor in series for current limiting is recommended. In Figure 3.6, the R_{SERIES} resistor acts as a current limiter to keep the maximum current below the 4mA limit of the FT pin. With a single DCM, a 1.5kΩ resistor will limit the current to about 2.2mA, sufficient to light an LED. Under normal conditions, the FT pin is internally biased to 3.3V by a 499kΩ ($R_{FAULT-INT}$) resistor, but can easily be held low by an external pull-down resistor. In the fault indicating LED circuit below (Figure 3.6), R_{SHUNT} is part of a voltage divider that holds the diode voltage in the OFF state when no fault is detected; a 49kΩ resistor is sufficient for a single DCM.

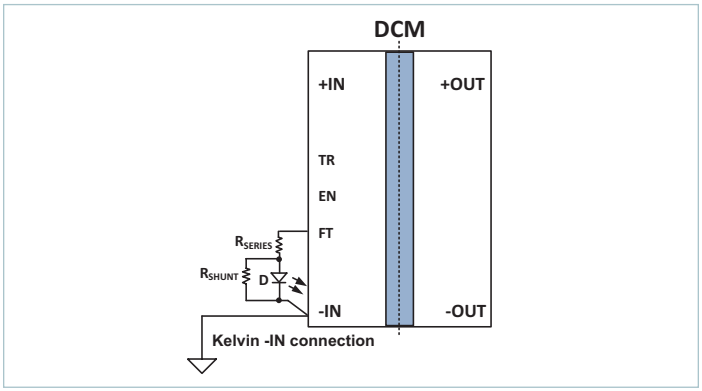
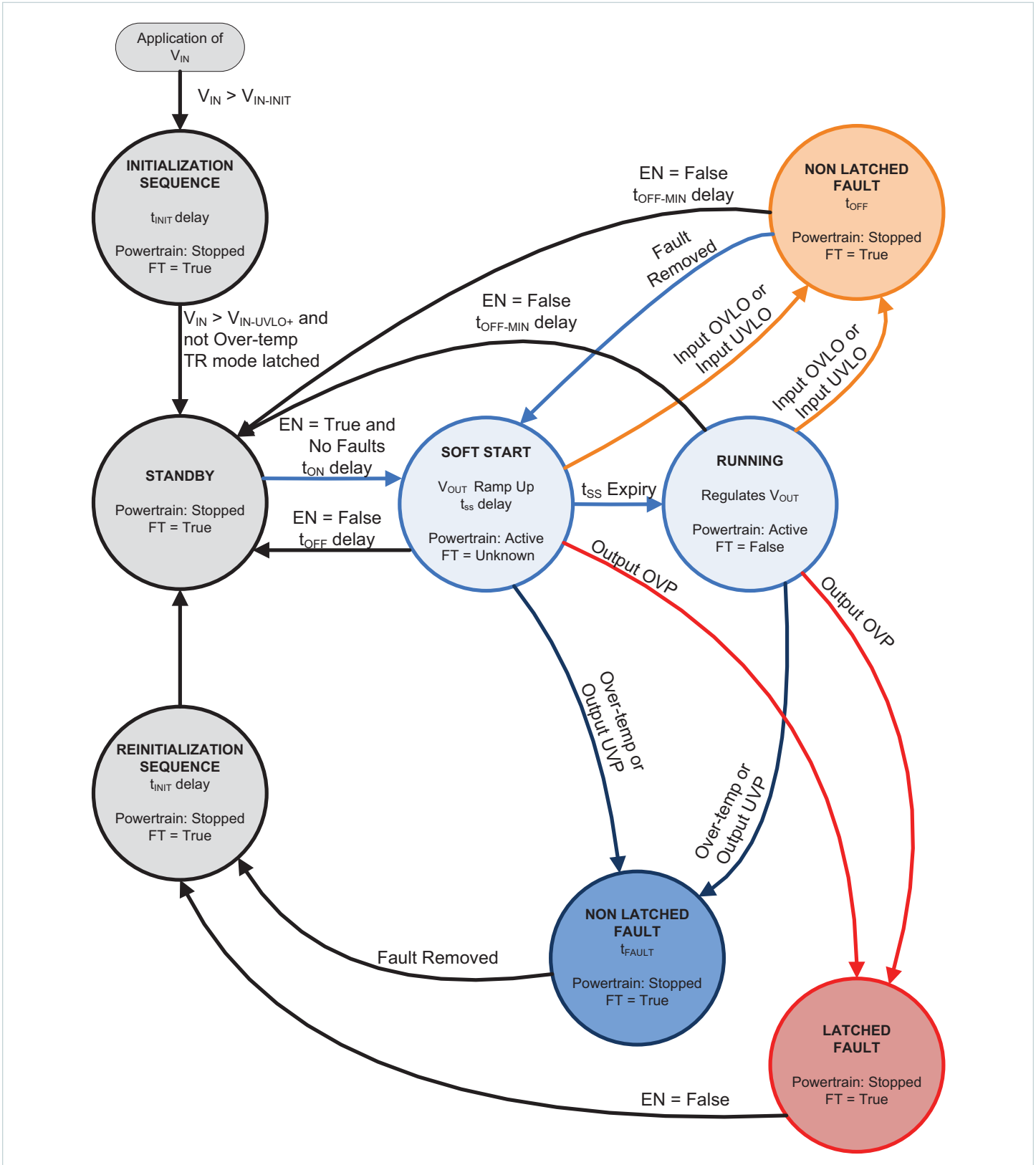


Figure 3.6 — *External circuit on the FT pin*

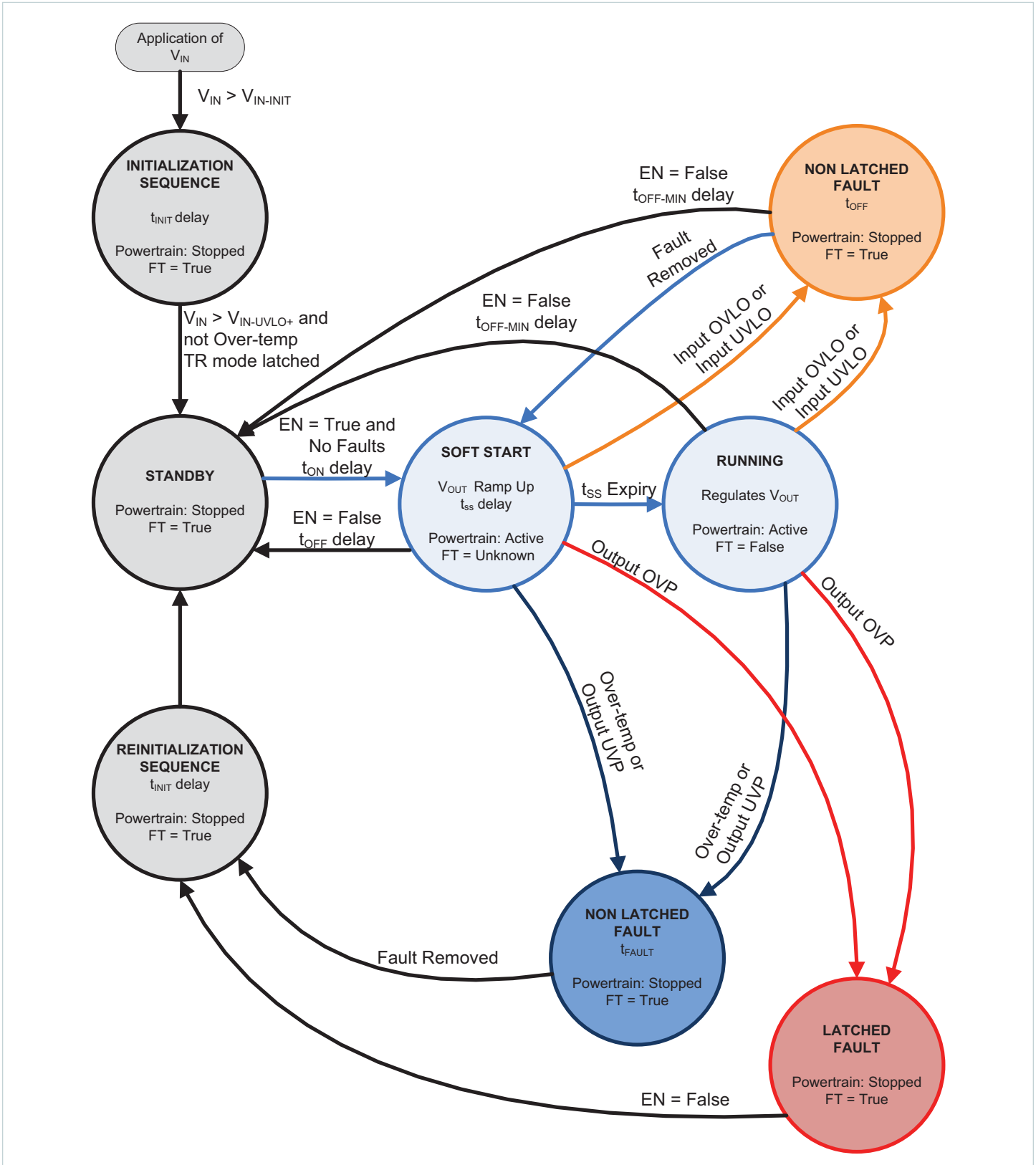
High-Level Functional State Diagram
DCMxxxxxxxxxx00 and DCMxxxxxxxxxx70 Series Only

Conditions that cause state transitions are shown along arrows.
Sub-sequence activities listed inside the state bubbles.



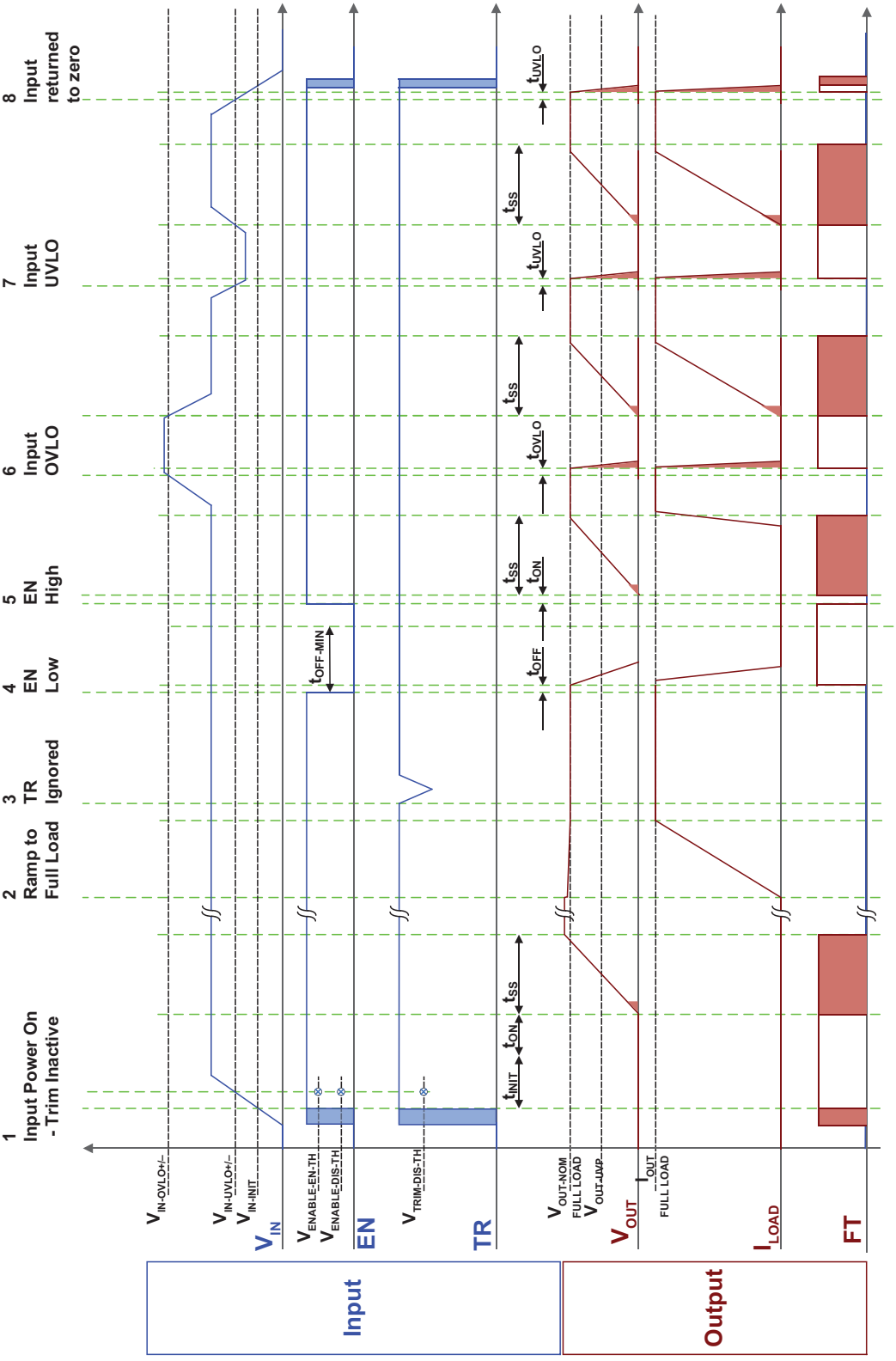
High-Level Functional State Diagram
DCMxxxxxxxxxx60 Series Only

Conditions that cause state transitions are shown along arrows.
Sub-sequence activities listed inside the state bubbles.



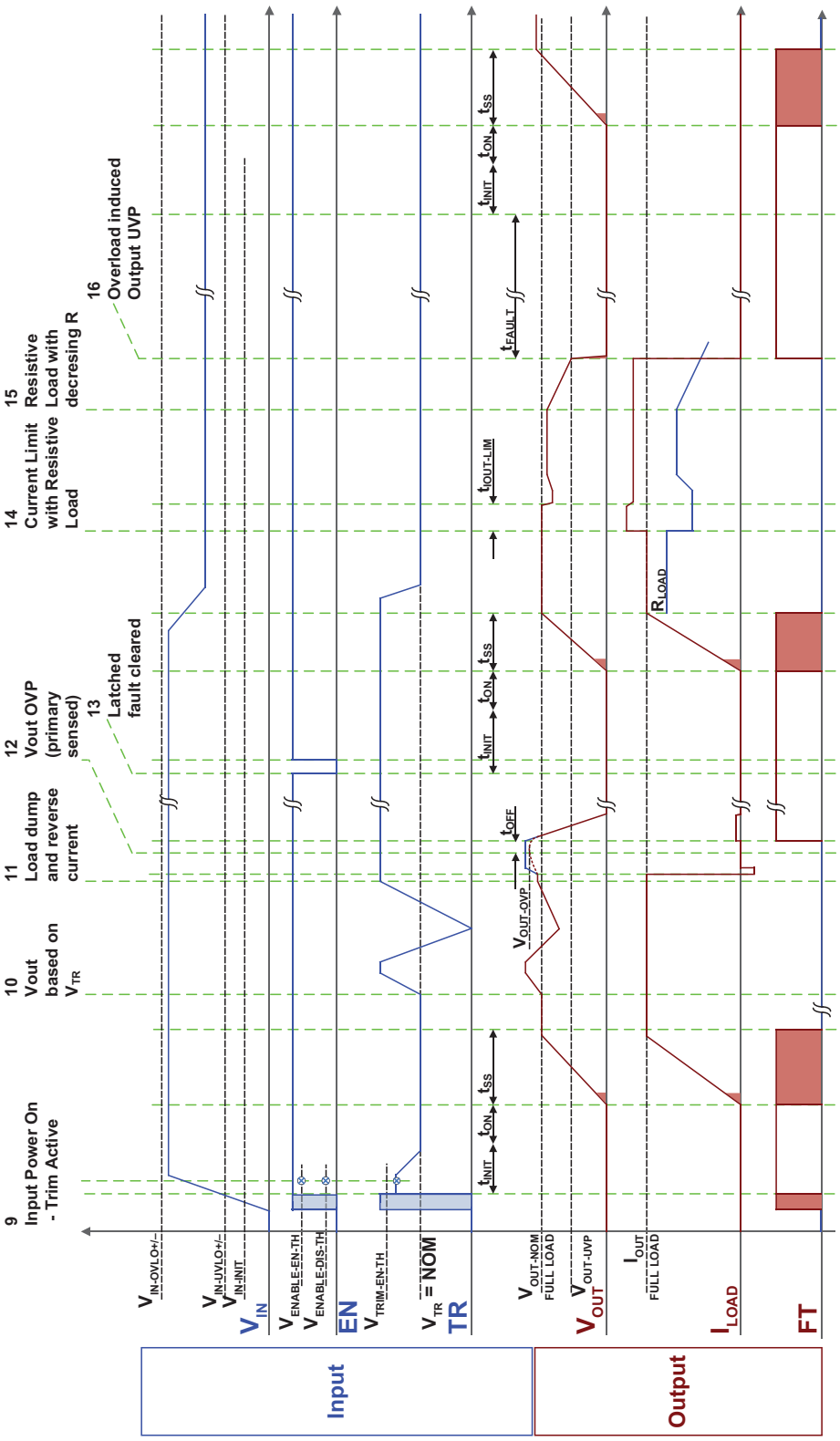
Timing Diagrams: DCMxxxxxxxxxx00 Series

Module Inputs are shown in blue;
Module Outputs are shown in brown.



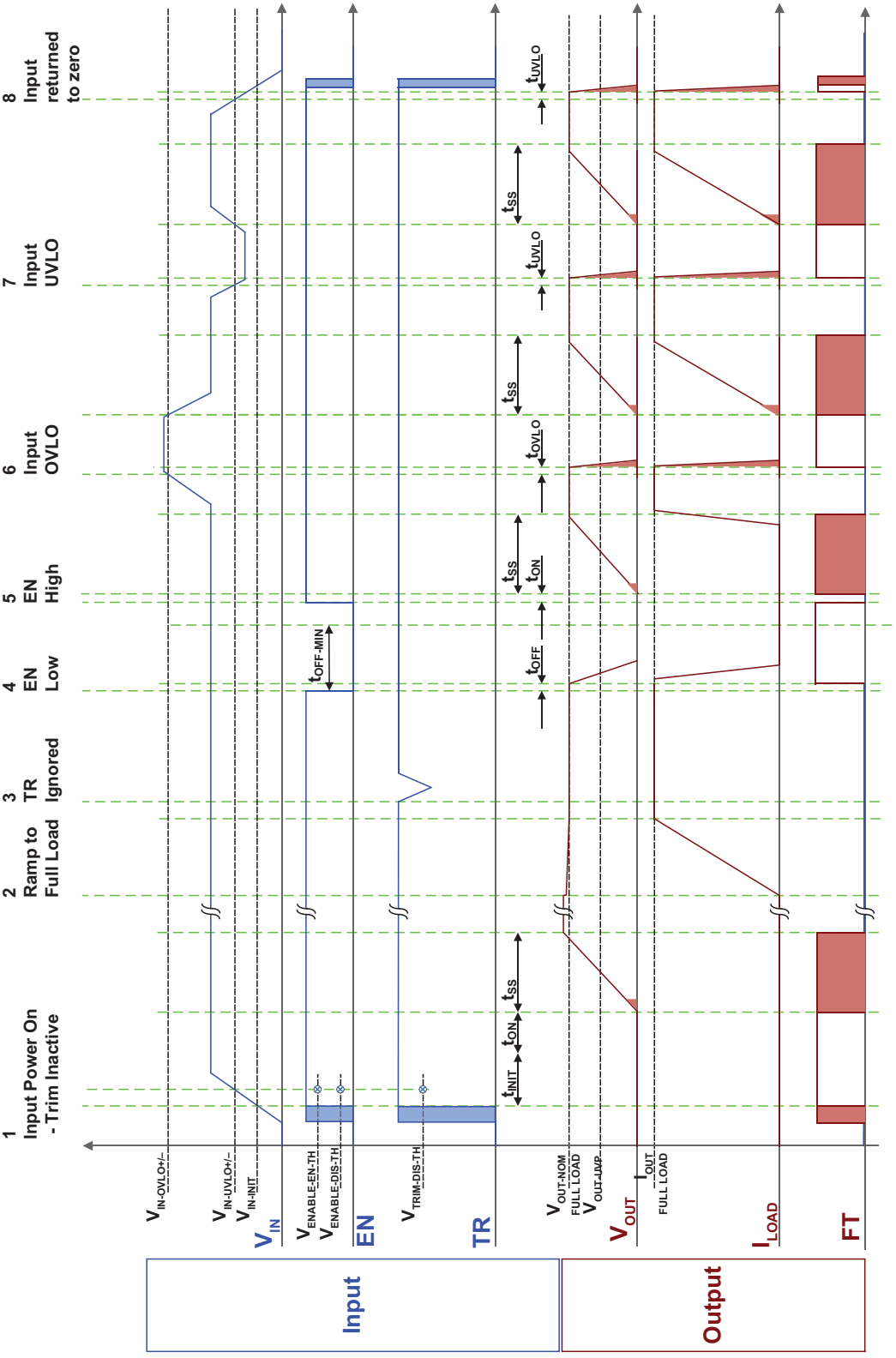
Timing Diagrams: DCMxxxxxxxxxx00 Series (Cont.)

Module Inputs are shown in blue;
Module Outputs are shown in brown.



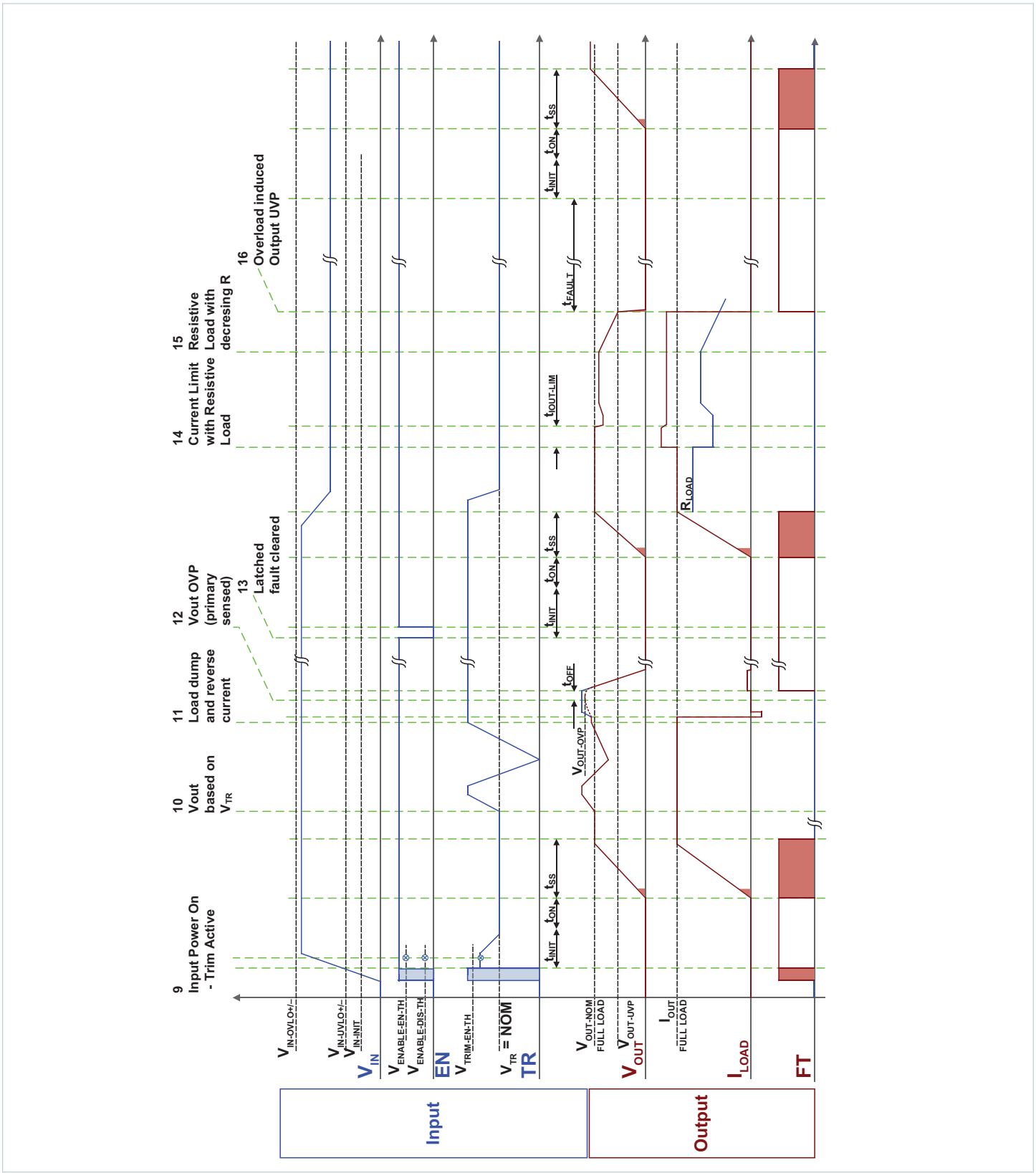
Timing Diagrams: DCMxxxxxxxxxx70 Series

Module Inputs are shown in blue;
Module Outputs are shown in brown.



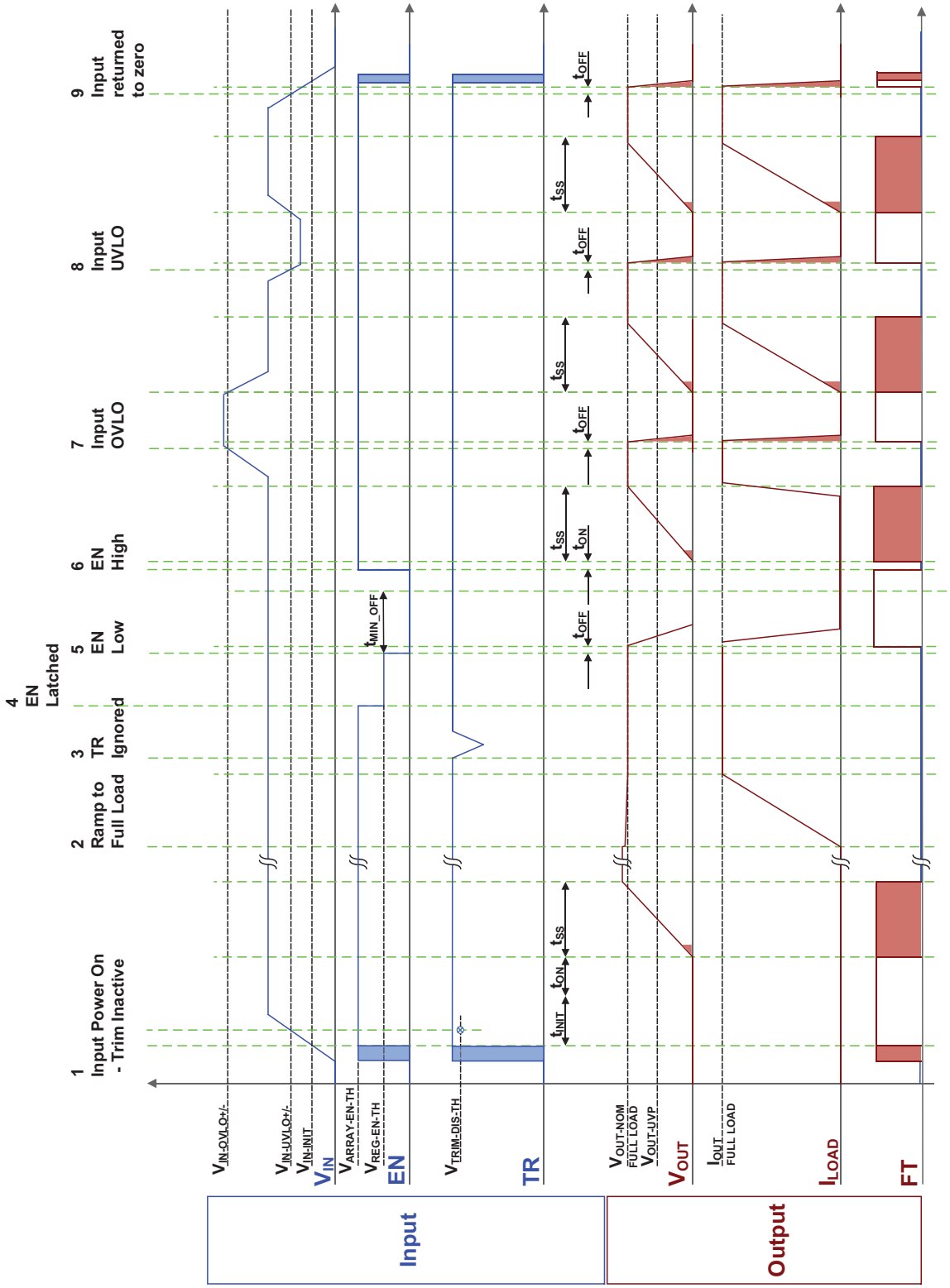
Timing Diagrams: DCMxxxxxxxxxx70 Series (Cont.)

Module Inputs are shown in blue;
Module Outputs are shown in brown.



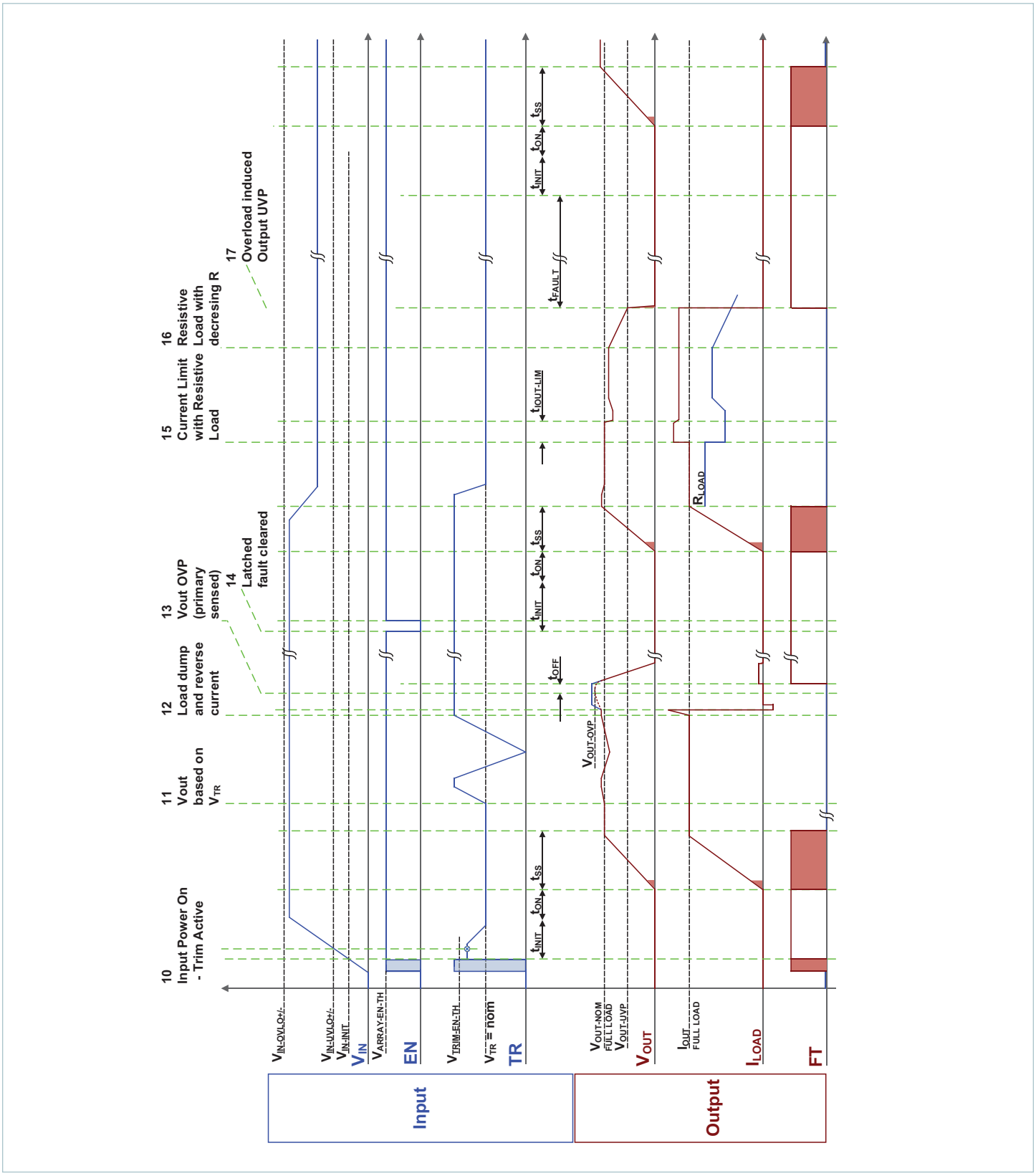
Timing Diagrams: DCMxxxxxxxxxx60 Series: Array Mode

Module Inputs are shown in blue;
Module Outputs are shown in brown.



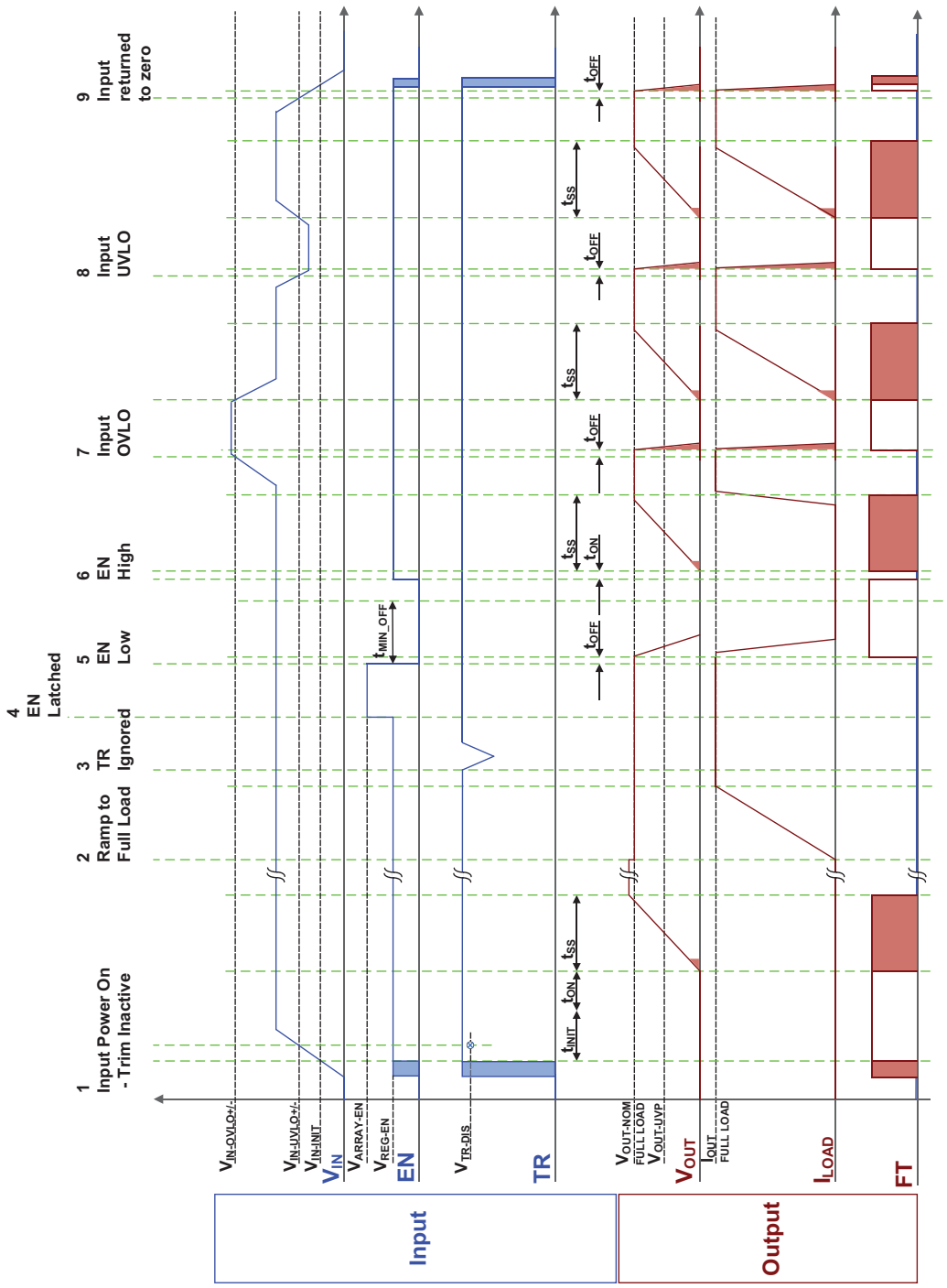
Timing Diagrams: DCMxxxxxxxxxx60 Series: Array Mode

Module Inputs are shown in blue;
Module Outputs are shown in brown.



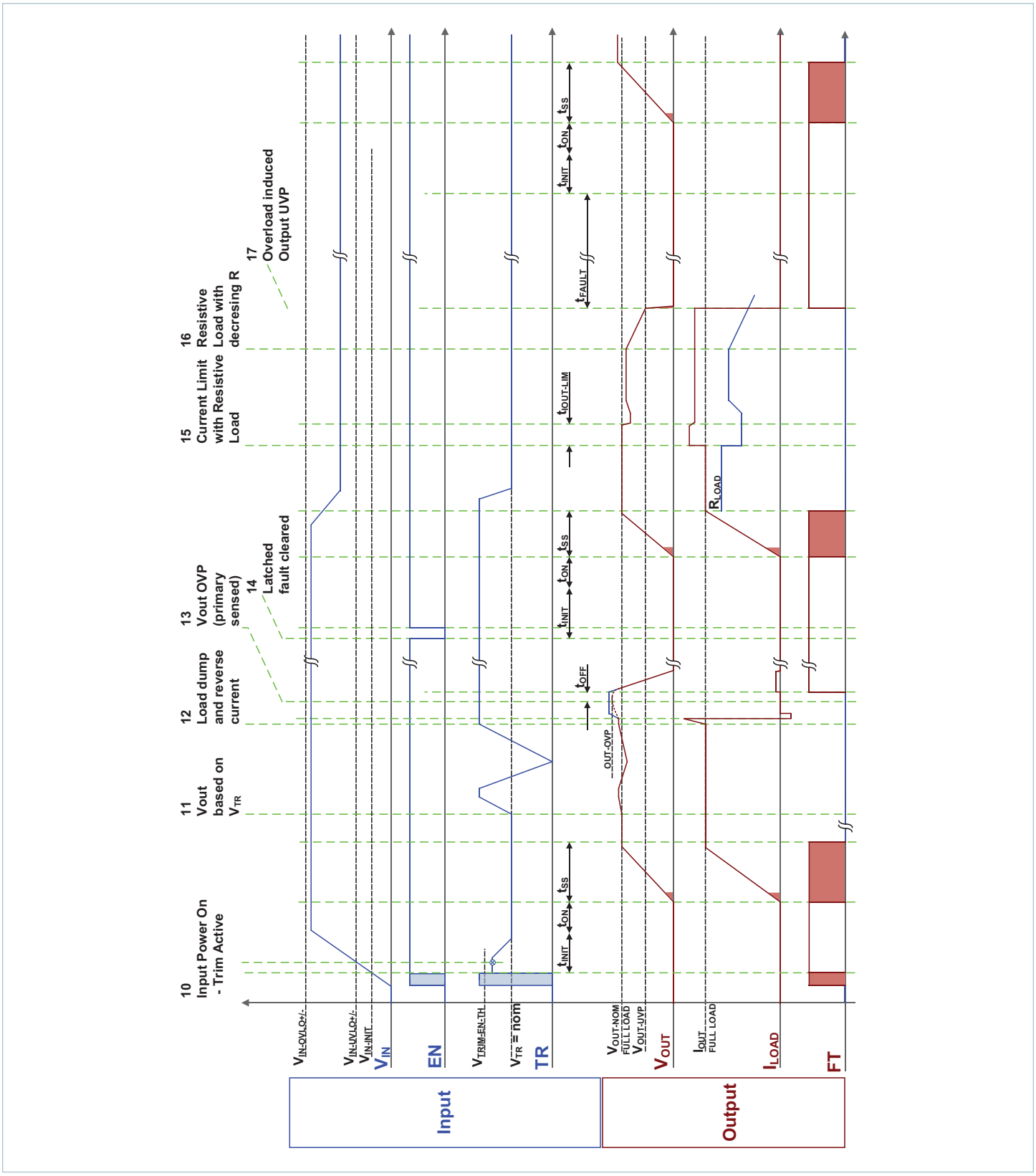
Timing Diagrams: DCMxxxxxxxxxx60 Series: Enhanced V_{OUT} Regulation Mode

Module Inputs are shown in blue;
Module Outputs are shown in brown.



Timing Diagrams: DCMxxxxxxxxxx60 Series: Enhanced V_{OUT} Regulation Mode

Module Inputs are shown in blue;
Module Outputs are shown in brown.



Start-Up Process (Applies to all DCM Series)

The start-up process of the DCM is explained in the high-level functional state diagram, also refer to the timing diagrams for the operating behavior of the DCM.

V_{IN} Start Up

When V_{IN} is applied and when $V_{IN} > V_{IN\_INIT}$, DCM will go through initialization sequence. The initialization sequence will last for $t_{INIT} + t_{ON}$ duration. Please refer to the product specific data sheet for t_{INIT} , t_{ON} timings. During the initialization sequence, the internal micro-controller will become active and the micro-controller will start monitoring the faults, status of EN pin (i.e., the DCM is enabled or disabled via EN pin) and the trim mode is latched based on the TR pin voltage. When $V_{IN} > V_{IN\text{-}UVLO+}$ and no fault is detected, DCM will finish the initialization sequence and enters into the soft-start process, which is discussed below.

Soft Start

Once the DCM finishes the initialization sequence and if no faults are detected, DCM will go through a soft-start process. Soft-start duration is given by t_{ss}, which can be found in the product specific data sheet. The soft start routine ramps the output voltage by modulating the internal error amplifier reference. This causes the output voltage to approximate a piecewise linear ramp. The output ramp finishes when the voltage reaches either the nominal output voltage, or the trimmed output voltage in cases where trim mode is active. **During soft start, the maximum load current capability is reduced. Until V_{OUT} achieves at least $V_{OUT\text{-}FL\text{-}THRESH}$, the output current must be less than $I_{OUT\text{-}START}$ in order to guarantee start up. Note that this is current available to the load, above that which is required to charge the output capacitor.**

Note: The FT pin status is unknown when $V_{IN} < V_{IN\_INIT}$ and during soft-start ramp time t_{SS}.

EN Start Up

When EN pin is pulled low to –IN of the DCM and V_{IN} is applied, the powertrain stays in standby mode. Therefore, the output of the DCM is disabled until EN pin is released or pulled high. During the standby mode, fault signal i.e., FT pin is high.

The DCM allows EN start up. With V_{IN} pre-applied, the output of the DCM can be either enabled or disabled by pulling the EN pin high or low. In this condition, the powertrain goes into standby mode during which the fault signal (FT pin) is high.

Nominal Output Voltage Load Line (Applies to DCMxxxxxxxxxx00 and DCMxxxxxxxxxx60 in Array Mode)

Throughout this subsection, the programmed output voltage, (either the specified nominal output voltage if trim is inactive or the trimmed output voltage if trim is active), is specified at full load, and at room temperature. The actual output voltage of the DCM is given by the programmed trimmed output voltage, with modification based on load and temperature. The nominal output voltage of DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) model is 28.0V, and the actual output voltage will match this at full load and room temperature with trim inactive.

The largest modification to the actual output voltage compared to the programmed output is due to the 5.263% $V_{OUT\text{-}NOM}$ load line, which for this model corresponds to $\Delta V_{OUT\text{-}LOAD}$ of 1.4736V. As the load is reduced, the internal error amplifier reference rises, and as a consequence the output voltage also rises. This load line is the primary enabler of the wireless current sharing amongst an array of DCMs.

The load line impact on the output voltage is absolute, and does not scale with programmed trim voltage.

For a given programmed output voltage, the actual output voltage versus load current at for nominal trim and room temperature is given by the following equation:

$$V_{OUT}@25^{o}C = 28.0V + 1.4736 \bullet \left(1 - \frac{I_{OUT}}{17.86}\right) \qquad 3.3$$

Nominal Output Voltage Temperature Coefficient (Applies to DCMxxxxxxxxxx00 and DCMxxxxxxxxxx60 in Array Mode)

A second additive term to the programmed output voltage is based on the temperature of the module. This term permits improved thermal balancing among modules in an array, especially when the factory nominal trim point is utilized (trim mode inactive). This term is much smaller than the load line described above, representing only a –3.73mV/°C change. Regulation coefficient is relative to 25°C.

For nominal trim and full load, the output voltage relates to the temperature according to the following equation:

$$V_{OUT\text{-}FL} = 28.0V - 3.733 \bullet 0.001 \bullet \left(T_{INT} - 25\right) \qquad 3.4$$

where T_{INT} is in °C.

The impact of temperature coefficient on the output voltage is absolute, and does not scale with trim or load.

Light-Load Boosting (Applies to all DCM Series)

The DCM enters Light-Load Boosting under light-loading conditions, when the internal power consumption of the converter plus the external output load is less than the minimum conversion power. For most DCM models, output voltage boosting can occur when the external load current is 10% or less of the DCM rated load current under any line, trim and temperature conditions. However, this scenario is most pronounced when the DCM input voltage is high, the trim voltage is low, and there is no load at the output.

During Light-Load Boosting, the DCM alternates between two operating conditions:

- Initially the error amplifier attempts to regulate V_{OUT} by enabling the converter powertrain, but the minimum energy per pulse that the powertrain can supply is greater than the power needed to maintain output regulation, so the output voltage climbs. As a result of that slight excess output voltage, the error amplifier momentarily inhibits the powertrain, allowing the output voltage to fall again. Once the output voltage falls below the error amplifier set point, the error amplifier starts the converter powertrain switching again.
- The second condition, when the powertrain is not switching, will typically last for tens or hundreds of times that of a regular switching period. Due to the primary-referred method of sensing the output voltage, the accuracy with which the error amplifier senses V_{OUT} is greatly reduced while the powertrain is momentarily inhibited. This results in an effective boosting of the actual V_{OUT} during Light-Load Boosting operation. Another result of the primary-sensed output voltage is that if an output load is suddenly applied during the momentary inhibit time, there may be an increased delay before V_{OUT} returns to its regulated level. The choice of output capacitor minimizes this, as covered in the Design Requirements - Output Capacitor subsection.

Overall Output Voltage Transfer Function

DCMxxxxxxxxxx00 and DCMxxxxxxxxxx60 series in Array Mode

Taking trim (Equation 3.2), load line (Equation 3.3) and temperature coefficient (Equation 3.4) into account, and adding the contribution of light-load boosting described above, the overall output voltage transfer function general equation becomes:

$$V_{OUT} = 11.64 + \left(21.909 \bullet \frac{V_{TR}}{V_{CC}}\right) + 1.4736 \bullet \left(1 - \frac{I_{OUT}}{17.86}\right) - 3.733 \bullet 0.001 \bullet \left(T_{INT} - 25\right) + \Delta V_{OUT\text{-}LL} \quad 3.5$$

DCMxxxxxxxxxx70 and DCMxxxxxxxxxx60 series in Enhanced V_{OUT} Regulation Mode

Taking trim (Equation 3.2) into account, and adding the contribution of light-load boosting described above, the overall output voltage transfer function general equation becomes:

$$V_{OUT} = 11.64 + \left(21.909 \bullet \frac{V_{TR}}{V_{CC}}\right) + \Delta V_{OUT\text{-}LL} \quad 3.6$$

Please see the specific part number data sheet for the light-load boosting threshold.

Output Current Limit (Applies to all DCM Series)

The DCM features a fully operational current limit which effectively keeps the module operating inside the Safe Operating Area (SOA), shown in Figure 3.7 and 3.8, for all valid trim and load profiles. The current limit approximates a "brick wall" limit, where the output current is prevented from exceeding the current limit threshold by reducing the output voltage via the internal error amplifier reference. The current limit threshold at nominal trim and below is typically 120% of rated output current, but it can vary between 100% and 135%.

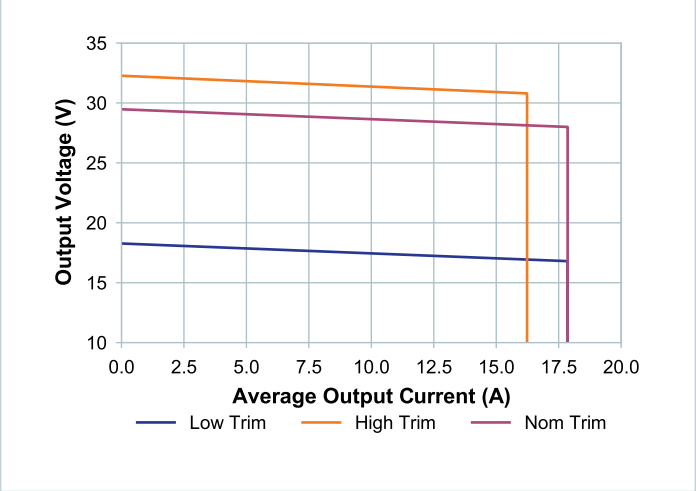


Figure 3.7 — *Electrical specified operating area (SOA): Array mode*

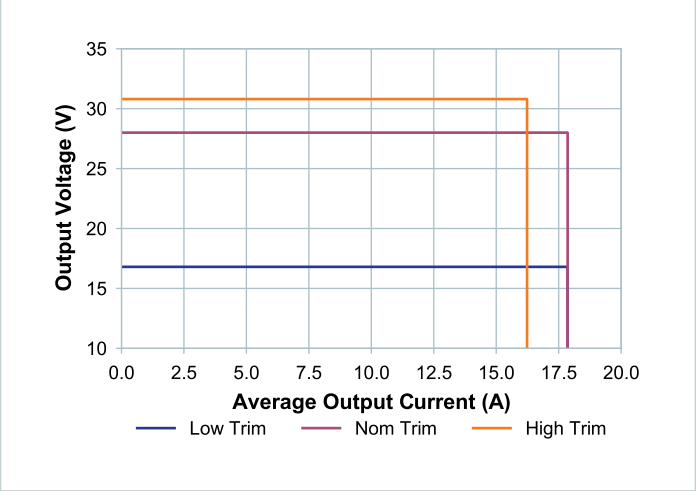


Figure 3.8 — *Electrical specified operating area (SOA): Enhanced V_{OUT} Regulation mode*

In order to preserve the SOA, when the converter is trimmed above the nominal output voltage, the current limit threshold is automatically reduced to limit the available output power, please refer to "High Trim" in Figures 3.7 and 3.8. When the output current exceeds the current limit threshold, current limit action is held off by current limit delay, $t_{IOUT\text{-}LIM}$ = 1ms, which permits the DCM to momentarily deliver higher peak output currents to the load. Peak output power during this time is still constrained by the internal Power Limit of the module. The fast Power Limit and relatively slow Current Limit work together to keep the module inside the SOA.

Delaying entry into current limit also permits the DCM to minimize droop voltage for load steps. Sustained operation in current limit is permitted, and no de-rating of output power is required, even in an array configuration. Some applications may benefit from well matched current distribution, in which case fine tuning sharing via the trim pins permits control over sharing. The DCM does not require this for proper operation, due to the power limit and current limit behaviors described here, current limit can reduce the output voltage to as little as the UVP threshold ($V_{OUT-UVP}$). Below this minimum output voltage compliance level, further loading will cause the module to shut down due to the output undervoltage fault protection.

Fault Handling
(Applies to all DCM Series)

Input undervoltage fault protection (UVLO)

The converter's input voltage is monitored to detect an input under voltage condition. If the converter is not already running, then it will ignore enable commands until the input voltage is greater than $V_{IN-UVLO+}$. If the converter is running and the input voltage falls below $V_{IN-UVLO-}$, the converter recognizes a fault condition, FT pin will become high and the powertrain stops switching, and the output voltage of the unit falls. Input voltage transients which fall below UVLO for less than t_{UVLO} may not be detected by the fault protection logic, in which case the converter will continue regular operation. No protection is required in this case. Once the UVLO fault is detected by the fault protection logic, the converter shuts down and waits for the input voltage to rise above $V_{IN-UVLO+}$, provided the converter is still enabled, it will then restart.

Input overvoltage fault protection (OVLO)

The converter's input voltage is monitored to detect an input over voltage condition. When the input voltage is more than the $V_{IN-OVLO+}$, a fault is detected, FT pin will become high and the powertrain stops switching, and the output voltage of the converter falls. After an OVLO fault occurs, the converter will wait for the input voltage to fall below $V_{IN-OVLO-}$. Provided the converter is still enabled, the powertrain will restart. The powertrain controller itself also monitors the input voltage. Transient OVLO events which have not yet been detected by the fault sequence logic may first be detected by the controller if the input slew rate is sufficiently large. In this case, powertrain switching will immediately stop. If the input voltage falls back in range before the fault sequence logic detects the out of range condition, the powertrain will resume switching and the fault logic will not interrupt operation regardless of whether the powertrain is running at the time or not, if the input voltage does not recover from OVLO before t_{OVLO}, the converter fault logic will detect the fault.

Output undervoltage fault protection (UVP)

The converter determines that an output overload or short circuit condition exists by measuring its primary sensed output voltage and the output of the internal error amplifier. In general, whenever the powertrain is switching and the primary-sensed output voltage falls below $V_{OUT-UVP}$ threshold, a short circuit fault will be registered. Once an output undervoltage condition is detected, the powertrain immediately stops switching, and the output voltage of the converter falls. The converter remains disabled for a time t_{FAULT}. Once recovered and provided the converter is still enabled, the powertrain will again enter the soft-start sequence after t_{INIT} and t_{ON}.

Output overvoltage fault protection (OVP)

The converter monitors the output voltage during each switching cycle by a corresponding voltage reflected to the primary side control circuitry. If the primary sensed output voltage exceeds $V_{OUT-OVP}$, the OVP fault protection is triggered. The control logic disables the powertrain, and the output voltage of the converter falls. This type of fault is latched, and the converter will not start again until the latch is cleared. Clearing the fault latch is achieved by either disabling the converter via the EN pin, or else by removing the input power, such that the input voltage falls below $V_{IN-INIT}$.

Temperature fault protections (OTP)

The fault logic monitors the internal temperature of the converter. If the measured temperature exceeds $T_{INT-OTP}$, a temperature fault is registered. As with the under voltage fault protection, once a temperature fault is registered, the powertrain immediately stops switching, the output voltage of the converter falls, and the converter remains disabled for at least time t_{FAULT}. Then, the converter waits for the internal temperature to return to below $T_{INT-OTP}$ before recovering. Provided the converter is still enabled, the DCM will restart after t_{INIT} and t_{ON}.

Parallel Operation of the DC-DC Converter Modules (DCMs)

When an application calls for more power than can be delivered by a single DCM, multiple DCMs can be put in parallel when the DCM models optimized for array operation is used. This section of the design guide discusses the parallel operation of ChiP DCMs. Paralleling DCMs is straightforward, since the operation of each DCM in an array is nearly identical to that of a single DCM circuit. In a parallel circuit, each DCM operates on its own load line, based on its share of the load; in general, the effect of adding DCMs in parallel is to remap that same load line over a higher current range, with no de-rating.

Current sharing between DCMs is automatically implemented. It is dependent on the individual DCM's output set points and load lines. Good load sharing among DCMs in an array is generally desired; however in most cases, it's not critical to accurately match the output set points, since DCMs are designed to operate without damage even in the case of a large sharing imbalance. An example of maximum sharing imbalance, between a DCM at full load and another DCM at minimum load is presented in this section (see section: "Special Application: Non-equal Trim Levels").

Despite not being required for operation, still it is better to optimize the current sharing, because that results in a more predictable aggregate load line and more equalized power dissipation. Equalizing power sharing across all DCMs also means that each DCM is operating at its lowest possible temperature, which results in better efficiency. To achieve good current sharing it is not necessary to have extremely accurate set points, since the load line has a bigger contribution to the output operating point vs. load than a small set-point error; additionally, the DCM has a built-in negative temperature coefficient (see Output Voltage Regulation section below) which helps to further compensate for small current sharing imbalances.

Overall Output Voltage Transfer Function

This section describes the overall output voltage transfer function of the DCM optimized for array operation. In order to implement current sharing without the use of communication between DCMs, the DCMs optimized for array operation are equipped with a negative-slope load-line and temperature coefficients, in order to implement a droop share.

For example, the overall output voltage transfer function for DCM4623TD2K31E0T00 (optimized for array operation) when taking load line, temperature coefficient and trim into account, becomes:

$$V_{OUT} = 11.64 + \left(21.909 \bullet \frac{V_{TR}}{V_{CC}}\right) + 1.4736 \bullet \left(1 - \frac{I_{OUT}}{17.86}\right) - 3.733 \bullet 0.001 \bullet \left(T_{INT} - 25\right) + \Delta V_{OUT\text{-}LL} \qquad 4.1$$

Note: Example above applies to DCM4623TD2K31E0T00 only.
To calculate V_{OUT} for other DCMs, see the relevant DCM data sheet.

Sample Circuit

An example of a circuit with four parallel DCMs is shown in Figure 4.1. In this circuit, the four DCMs have different input voltage sources (all referenced to the same –IN).

DCMs have on-board protection for input overvoltage and overcurrent, so the fuses F1 – F4 shown in Figure 4.1 are only needed for applications that must pass safety approvals, such as CE Mark or UL60950 and also to avoid the risk of fire and board damage during the input short circuit failure. In that case, note that each DCM needs its own input fuse. For more information on fuse selection and recommendations, see the section on "Safety Considerations".

Each DCM has to see at least a minimum value of $C_{OUT\text{-}EXT}$ local to its output pins, before any output inductors (and therefore closer to the DCM than to the junction of all DCM outputs). In arrays where all the DCMs are always started together, the array may have up to n* maximum value of $C_{OUT\text{-}EXT}$ of total output capacitance (both local and bus capacitance). In arrays where DCMs can be started individually, the total capacitance seen by any DCM output (both local and bus capacitance) must be equal or below the maximum value of $C_{OUT\text{-}EXT}$ of a single DCM. See sub-sections "Start Up" and "Support Circuitry" for more information.

For stability, to minimize ringing, and to provide optimal margin between the DCM's rated input low line and its input undervoltage fault protection threshold (UVLO), the source impedance of V_{IN} must be no more than half the combined effective input impedance of the DCM array. For example, for the DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) model at full output power (500W) and nominal efficiency (93%), the input power is 555W; at low line (160V) this corresponds to an equivalent input impedance of 46.12Ω (i.e., $160^2/555$). For an array of four units, the combined input impedance is 11.53Ω, and the source impedance must be no higher than 5.765Ω. If this is not the case, the input filter circuit must compensate for the excessive impedance, for more information on input filter design, please see the section "Differential Mode Input Filter Design and Simulations". A optimum value of decoupling capacitor must be used at each DCM's input to compensate the excessive impedance, for more information on decoupling capacitor, please refer to the section "Source Impedance and Its Effects on System Stability".

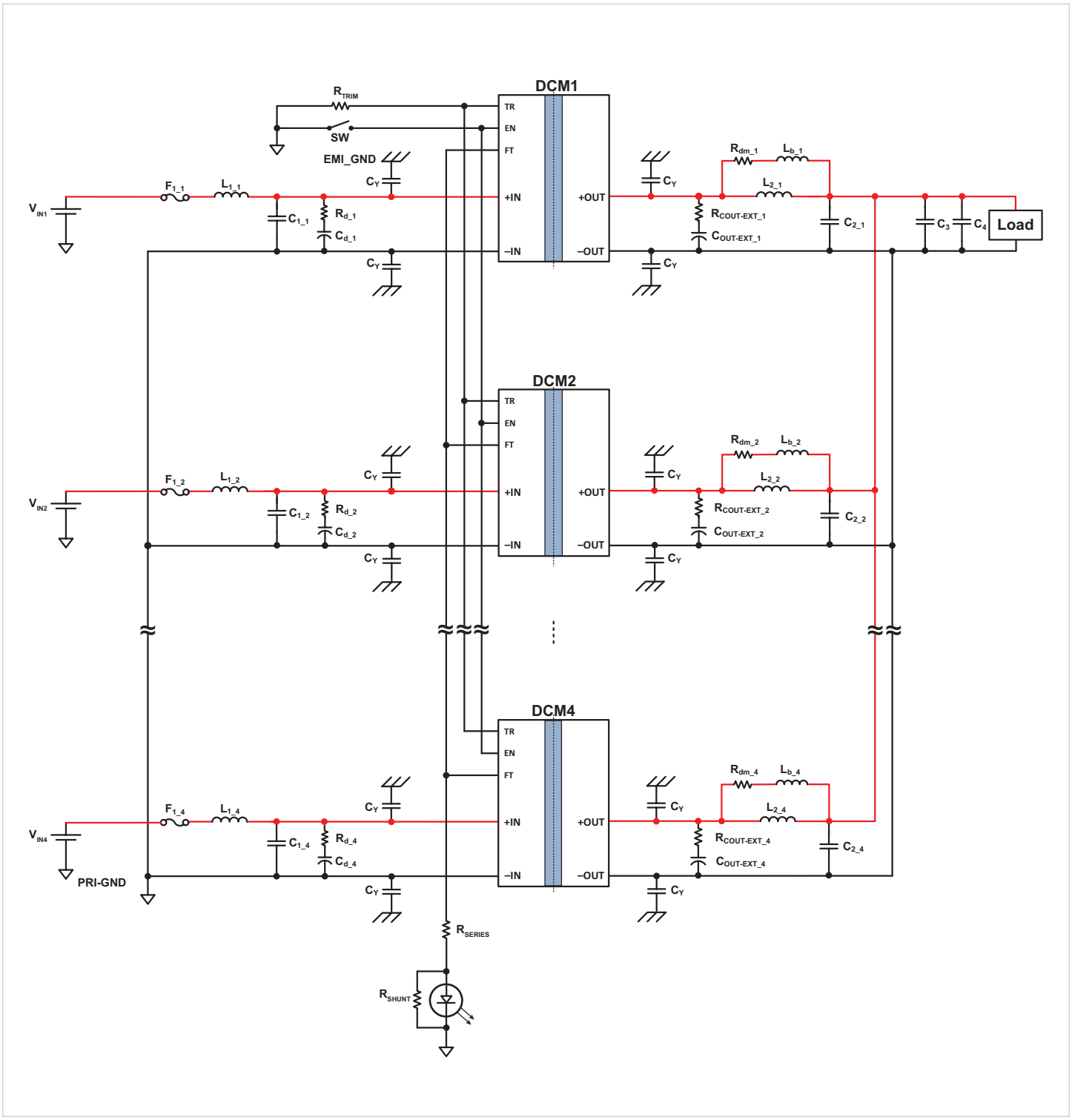


Figure 4.1 — *Parallel DCM circuit*

Output Voltage Regulation

The DCM provides a regulated output voltage around a load line that is 5.263% of the nominal voltage referenced to full load. Decreasing the load causes the output voltage to rise.

Details Regarding DCM Load-Line Slopes and Specified Values

Specifying 5.263% at full load is the same as specifying the load line as having 5.0% of some no-load voltage. For example, with a 24V nominal output DCM,

$$V_{OUT\_NO\_LOAD} = V_{OUT\_FULL\_LOAD} \bullet (1 + 0.05263) \qquad 4.2$$

$$= 24 \bullet (1 + 0.05263) = 25.26V$$

In the other direction:

$$V_{OUT\_FULL\_LOAD} = V_{OUT\_NO\_LOAD} \bullet (1 - 0.05) \qquad 4.3$$

$$= 25.26 \bullet (0.95) = 24V$$

Since the marketed $V_{OUT-NOM}$ refers to the full-load voltage, to keep the literature consistent, the 5.263% figure will be used here

An example of an ideal V_{OUT} vs. I_{OUT} plot for the DCM4623TD2H26F0T00 is shown in Figure 4.2, which is a modified version of one of the DCM data sheet figures ideal V_{OUT} vs. load current, at 25°C case). This is an ideal plot because it does not consider the contribution of light load boosting, which is addressed separately.

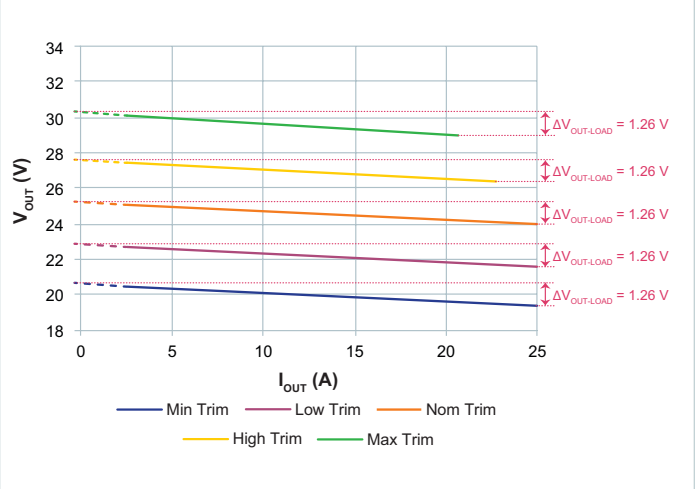


Figure 4.2 — *Ideal V_{OUT} vs. I_{OUT} plot for DCM4623TD2H26F0T00*

As shown in the Figure 4.2, changing the trim value doesn't affect the slope of the load line; the slope is still 5.263% of the nominal output voltage at full load, which for the model used in this example corresponds to a $V_{OUT-LOAD}$ of 1.26V. The same is true of changes in temperature: voltage decreases with increasing temperature, but the slope of the output voltage transfer function doesn't change. (See "Overall Output Voltage Transfer Function" in the DCM data sheet.)

If the equivalent series resistance introduced by the DCM load line is needed, it can be calculated starting from the load line equation given in the DCM data sheet, in the section "Nominal Output Voltage Load Line." For example, the load line equation for the DCM4623TD2H26F0x00 (with nominal trim) is:

$$V_{OUT} @ 25^oC = V_{OUT\_FULL\_LOAD} + \Delta V_{OUT\text{-}LOAD} \bullet \left(1 - \frac{I_{OUT}}{I_{OUT\_RATED}}\right) \qquad 4.4$$

Where:

$V_{OUT\_FULL\_LOAD}$ is the voltage at full load and nominal trim,

$V_{OUT-LOAD}$ is the rise of the "ideal" load line,

I_{OUT} is the actual output current, and

I_{OUT_RATED} is the rated output current in Amps (full-load current).

The equation above can be rewritten as:

$$V_{OUT} @ 25^oC = V_{OUT\_FULL\_LOAD} + \Delta V_{OUT\text{-}LOAD} - \Delta V_{OUT\text{-}LOAD} \bullet \left(\frac{I_{OUT}}{I_{OUT\_RATED}}\right) \qquad 4.5$$

Using typical values:

$V_{OUT-LOAD}$ = 1.26V

$V_{OUT\_FULL\_LOAD}$ = 24.0V

I_{OUT_RATED} = 25.0A

and combining terms,

$$V_{OUT} @ 25^oC = 25.26 - \left(\frac{1.26}{25.0}\right) \bullet I_{OUT}$$

Where 25.26V is the "ideal" voltage at no load and nominal trim, which corresponds to the 24.0V output at full load and nominal trim plus 1.26V for the load line.

$$V_{OUT} @ 25^oC = 25.26 - 0.0504 \bullet I_{OUT}$$

The equivalent series resistance in Ohms introduced by the load line, $V_{OUT-LOAD}/I_{OUT}$ (50.4mΩ in this example), can be referred to as $R_{INT\_LOADLINE}$.

Load Sharing

The primary objective of paralleling DCMs is to extend the loading capabilities beyond that of a single DCM. See Figure 4.3 for an example. The Figure 4.3 shows multiple DCMs operating along the same load line as a single DCM, but with the output current scaled proportionally with the number of DCMs in parallel. As implied in Figure 4.3, the failure of a single unit doesn't necessarily result in the array being brought down, if the array is sized as N+1 redundant relative to the maximum load. As in other cases, sharing is based mainly on the load line and to a lesser degree, the temperature coefficient, which is discussed next.

Parallel units with the same output set point (i.e., same trim value and same temperature), ideally would have their load lines perfectly overlap, and therefore their current sharing would be perfect. In reality, there might be a small difference in sharing due to the output voltage set-point accuracy, which could cause the real load line of each DCM to move slightly from the ideal set point. This would cause some sharing imbalance: that is, a unit with a slightly higher output voltage set point would contribute a little more to the output current than a unit with a lower output voltage set point. Inaccuracy in the set point represents a small contribution to the load line, so the resulting sharing imbalance would be minor.

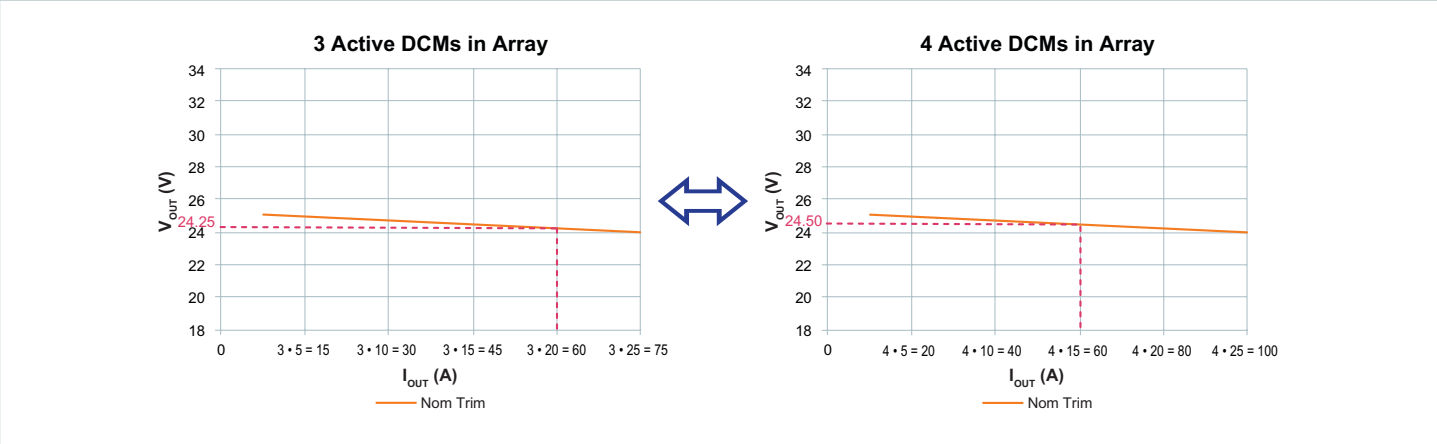


Figure 4.3 — *Parallel DCMs behave like a single DCM with a higher output current*

The maximum set-point accuracy specified in the data sheet (%$V_{OUT-ACCURACY}$, ±2% for most models, –3% to +2% for some special DCMs) refers to the maximum variation of the set point over all possible operating conditions (line, load, trim and temperature). The set-point accuracy for nominal conditions (nominal V_{IN}, nominal trim, full load, 25°C) is ±0.5% V_{OUT_NOM} (see the minimum and maximum values for "Output voltage set point" in the data sheet Electrical Specifications).

Temperature has a small, beneficial effect on current sharing. The DCM has a negative voltage-temperature coefficient (see "Overall Output Voltage Transfer Function" in the data sheet). If a unit is loaded more than others, its relative temperature tends to rise, which causes its output voltage to be reduced. Note that this change in set point does not affect the load line slope. Since the output voltages of the other parallel DCMs match that of the loaded DCM, their outputs would follow their load lines, increasing their share of the load current and bringing the circuit back to equilibrium.

DCMs operate well in parallel, even if their trim settings are not all the same. Unequal trim settings cause each DCM load line to start at a different y-intercept (see Figure 4.4); since their output voltages are forced to be the same value by the paralleled output connections, their currents will be different when the circuit achieves balance. The voltages and currents are maintained at those levels using the mechanisms described above. From Figure 4.4, it can be seen that setting the trim at different levels between units creates a mismatch in current sharing.

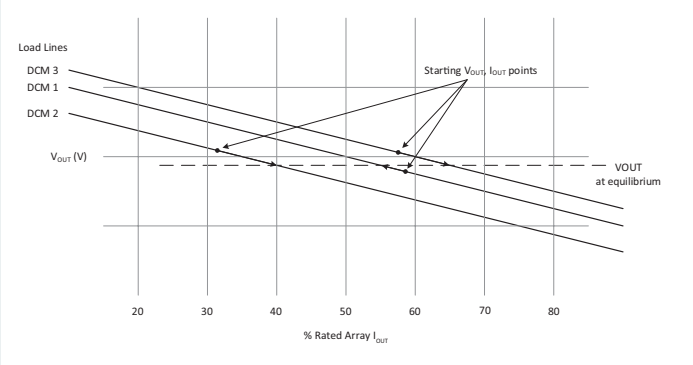


Figure 4.4 — *Load lines of parallel DCMs trimmed to different voltages*

Sharing improves at the upper limit of the output power range. Because of the finite accuracy of the output set point, the output voltages won't be identical (see Figure 4.4) so as the output power increases, the DCM with the highest voltage will reach its maximum output current before the others. When that happens, it will operate as a constant current source. (The DCMs not in constant current will continue to regulate the output voltage).

For either trim/sharing scenario discussed above, the output ripple is typically reduced in a parallel DCM circuit compared to that of a single unit, because the DCMs aren't synchronized. That is, their switching periods are not in phase, so the combined outputs of parallel DCMs can behave like a single output with a higher effective switching frequency and lower ripple amplitude. In the best case, the switching periods of N parallel DCMs would be evenly staggered in time, so that the equivalent switching frequency would be N • $f_{SW\_STANDALONE}$. Since all DCMs would contribute equally to maintaining the output voltage, the output ripple would be $V_{OUT\_RIPPLE\_STANDALONE}$/N. In the worst case scenario, all DCMs would have the same frequency and be in phase, such that the equivalent switching frequency and total output ripple would be the same as that of a single DCM. In a real-world situation, the switching periods are randomly distributed, so the output ripple lies somewhere between the two extreme cases.

Start Up

The start-up behavior of a DCM array depends on the type of load: resistive or constant current.

For a resistive load, the load current increases as the DCM array output voltage rises. On start up, DCMs have a soft-start ramp when operated alone; in an array, the DCMs don't all turn on at the same time, so there will be an additional component of the soft-start ramp due to a subset of DCMs starting before the others. This is most notable when the DCMs are started from the application of V_{IN}, with a slow input dV/dt. During the soft start ramp, if the load current V_{OUT}/R_{LOAD} exceeds the combined current limits (I_{OUT-LM}) of the active DCMs, then those DCMs go into current limit and the start-up ramp plateaus to $V_{OUT} = R_{LOAD} \bullet I_{OUT-LM}$ (assuming this V_{OUT} is above $V_{OUT-UVP}$, the minimum current-limited V_{OUT}, listed in the DCM data sheet). As additional DCMs turn on and "catch up" to the first group, they add current drive capability (that is, they increase the total current limit), and the output voltage increases to a higher level, given by the load resistance multiplied by the new total current limit. This continues until there are enough active DCMs to provide the full-load current at V_{OUT_NOM}, allowing all DCMs to exit from current-limited operation.

With a constant current load, the load current remains the same even if the DCM output voltage decreases. At start up, a DCM has a load current capability of $I_{OUT-START}$, which is approximately 10% of the full load. If parallel DCMs were started from the application of V_{IN} and the load current exceeded the sum of the current limits of the active DCMs (I_{OUT-LM}), the active DCMs would go into current limit, as in the case for the resistive load. In this case, the DCM output voltage would drop, because the load current would be greater than the current limit, so the output voltage would collapse. The higher the constant-current set point of the load, the faster the DCM output voltage would collapse. In some extreme scenarios, V_{OUT} could collapse when the first DCM turned on, before additional DCMs could start driving the load.

To prevent this, the start-up delay between units would have to be smaller than the current limit delay; that is, the time from the first to the last DCM turning on would have to be shorter than the time it would take the current limit of the first DCM to kick in. This can be done by using EN to start the DCMs. To summarize, for constant current loads, EN ensures that the turn-on delay between DCMs is smaller than the current limit delay of one DCM.

Special Application: Optimizing Current Sharing at High Temperature

Optimizing the current sharing between DCMs equalizes power dissipation. While DCMs still operate even when the load current is not balanced, equalizing power dissipation leads to higher efficiency, since generally speaking, efficiency is slightly reduced near the maximum operating temperature.

There is an uncommon condition where good load sharing across an array is required for operation. This happens when the circuit operates at a temperature and power that are high enough to force the use of the de-rating curve shown in Figure 4.5.

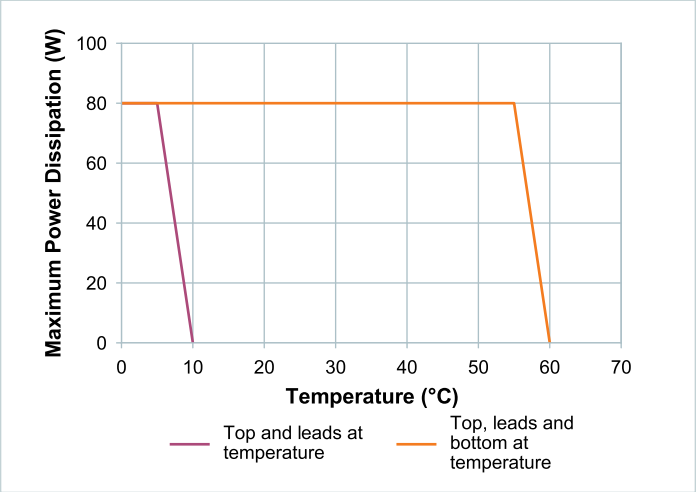


Figure 4.5 — *Thermal specified operating area: max power dissipation vs. case temp for arrays or current-limited operation*

In these applications, good current sharing is important because a gross imbalance would increase the temperature of the overloaded part, which would decrease its maximum power. There are two scenarios:

- When operating at a temperature and power level that are far from the de-rating curve, a load imbalance causes a temperature difference, (which is partially compensated for by the temperature coefficient), but the maximum power does not change. In this case, a loading imbalance does not adversely affect the system.
- When operating close to or at the de-rating curve, a load imbalance causes the temperature of the overloaded part to increase, which decreases the maximum power the unit can tolerate without triggering over-temperature protection (OTP). If the power being processed by the unit is above the derated maximum power, the DCM in question will trigger OTP and shut down. The other units have to compensate for the power drop caused by the unit shutting down, so their temperatures increase, reducing their maximum output power that the remaining units can tolerate without triggering OTP. This can lead to a domino effect that can potentially cause each DCM to trigger OTP and shut down one by one until the whole system shuts down. For these applications, good current sharing is required.

Special Application: Non-Equal Trim Levels

Deliberately setting the programmed trim of DCMs in an array to different levels, (such that some units reach their current limit long before others), could effectively be used to extend the equivalent load line of the array over the entire array load rating. While this is not a common application, it shows how robust the DCMs are, even under non-ideal conditions.

As an example, consider two units in parallel, both with V_{OUT_NOM} = 20V (at full load) and 10A maximum current each. As previously explained, DCMs have a built-in load line that is 5.263% of the nominal output voltage from full load to no load. For the units in this example, the load line would be 20 • (0.05263) = 1.0526V (see Figure 4.5). At nominal trim the DCM would show an output voltage of 20V at full load and 21.0526V at no load (excluding the possible contribution of light load boosting, which is discussed separately). For these two DCMs in parallel, with nominal trim, the contribution of the load line would go from 21.0526V at no load to 20V at full load (I_{MAX}). I_{MAX} would be 20A, the sum of the individual currents.

This example considers a simplified ideal scenario where the current limit inception point is at 100% rated I_{OUT}. In reality the current limit inception is variable based on line and temperature conditions; min, typ and max values are provided in the DCM data sheet (Output current limit, Page 5).

If one unit, DCM1, is taken out of the parallel circuit (array) and its trim increased to 21.0526V at full load, its load line would still be 1.0526V, but it would go from 21.0526V at full load to 22.1052V (21.0526V + 1.0526V) at no load (see Figure 4.5). Putting this DCM back into the original circuit, and increasing the load from the zero to the maximum, the nominally trimmed DCM (DCM2) would not contribute to driving the load until DCM1 reached an output voltage of 21.0526V. At that point, DCM1 would be at full load, while DCM2 would be at the highest set point of its load line (i.e., the point at the load line for which the unit outputs zero current). As the load is increased, DCM1 would go in to current limit and DCM2 would start driving the load, meaning that it would regulate the voltage based on its own load line. With the load at 20A, DCM2 would also be at full load and V_{OUT} = 20V.

The voltage from no load to the full load for the array would have gone from 22.1052V to 20V; the equivalent load line of the array would be almost 10% (i.e., almost double the load line of a single unit).

This example is of little practical value, since it negates many of the advantages of putting DCMs™ in parallel, but it shows that DCMs would still function in a predictable manner even under these extreme conditions (as long as the cooling for the DCMs satisfies the limits in Figure 4.5, maximum dissipation versus case temperature).

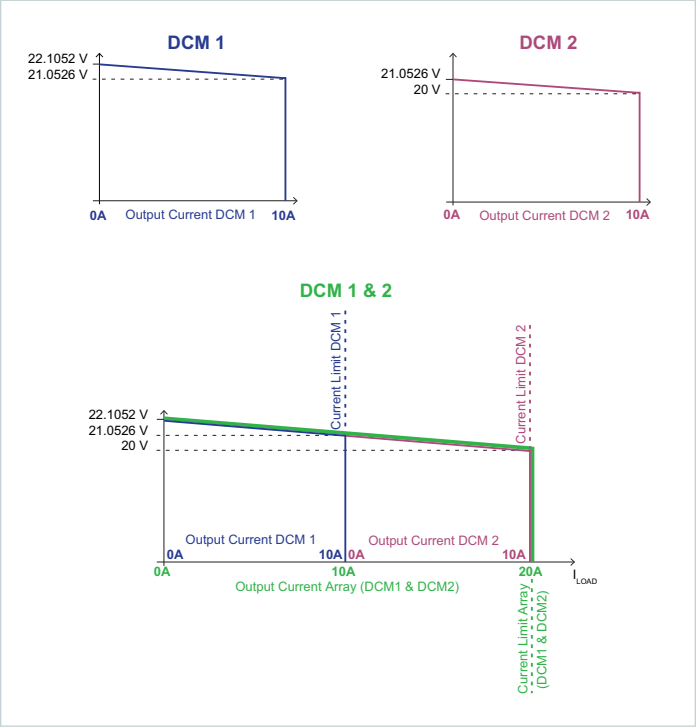


Figure 4.5 — *Effect of parallel DCMs with different trim set points on load line*

Problem Associated with the Parallel Operation of DC-DC Converter Modules

As mentioned above, when multiple DCMs are connected in parallel array configuration, they can share the current without any requirement of additional external circuitry, using the inherent droop share property. However, there are a few potential problems associated with the parallel operation of the switching converters, which are listed below:

- Beat frequency noise at the common input and output bus
- Chaotic condition in the feedback control loops of the DCMs, which leads to oscillations in the output voltage

1. *Undesired Beat Frequencies in Parallel Configuration of the DCMs*

Although the parallel connected DCMs are of the same type and are designed to operate at the same switching frequencies, due to part-to-part variability, the DCMs in a parallel array configuration will operate at slightly different operating points. As a result, the DCMs switch at different frequencies. The interaction among the switching noise of each DCM in a parallel array results in undesired beat frequencies at the common input and output bus. As a result, AC ripple currents circulating in the input and output sections of the converters are increased. The path of the circulating AC ripple currents is depicted in Figure 4.6. The beat frequencies generated are the differences between the operating frequencies of the DCMs, which is given by the Equation 4.6:

$$f_b = \left| f_{SW1} - f_{SW2} \right| \qquad 4.6$$

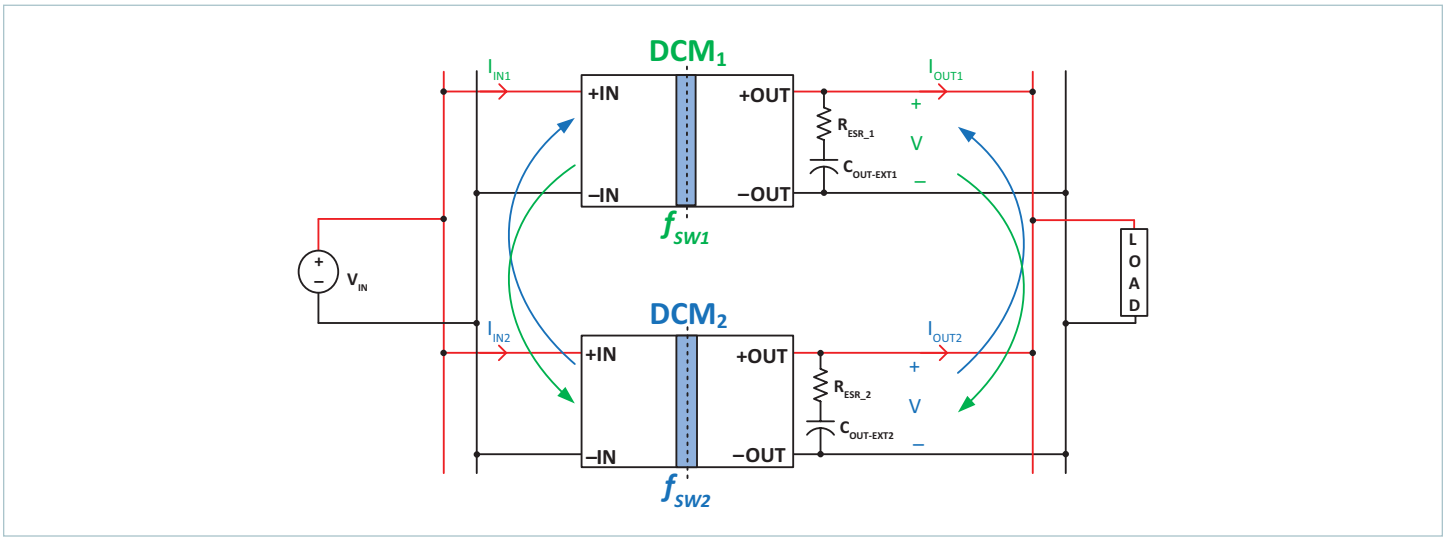


Figure 4.6 — *Parallel array of DCMs, path of AC circulating currents*

For example, the DCM1 and DCM2 with the nominal switching frequency of 1MHz might have the operating switching frequencies of f_{SW1} = 1MHz and f_{SW2} = 1.02MHz. Thus, the resulting beat frequency noise f_b will be much lower in frequency i.e., f_b = 20kHz. The total AC ripple current in the input and output of the DCMs will have much lower, 20kHz, frequency component, which is difficult to filter out using a typical filtering network. The circulating AC ripple currents can cause interference between the interconnected systems, which in turn can lead to the system stability and power quality issues. The circulating AC ripple currents also cause stress in the DCM internal bypass capacitors, and in some cases the DCM itself can detect a false positive fault condition.

2. ***Chaotic Conditions in Parallel Configuration of the DCMs***

In parallel operation of the DCMs, the output nodes of each DCM are connected at the common bus. The output of each DCM comprises the DC component and the AC ripple related to the relative converter's switching frequency. At the common node, the interactions between the feedback control loop of each DCM may result in oscillations in the output voltage. The oscillations in the output voltage are a result of one converter's switching frequency noise being the other converter's high-frequency perturbation.

Design Guidelines for Suppressing Beat Frequency Oscillations and Feedback Control Loop Interactions

To prevent beat frequency oscillations in the parallel converter system, the injected AC ripple currents from each converter must be limited. This can be achieved by adding a small value of an inductor and low-ESR capacitors (such as ceramic capacitors) at the input and output of each DCM, as shown in Figure 4.7. The inductor increases the interconnected line impedance at high frequency, resisting the flow of AC ripple currents. Thus, placing the ceramic capacitors on the common output bus after the decoupling inductors aides in attenuating the circulating AC ripple currents. Hence, the magnitude of the beat frequency oscillations are drastically reduced.

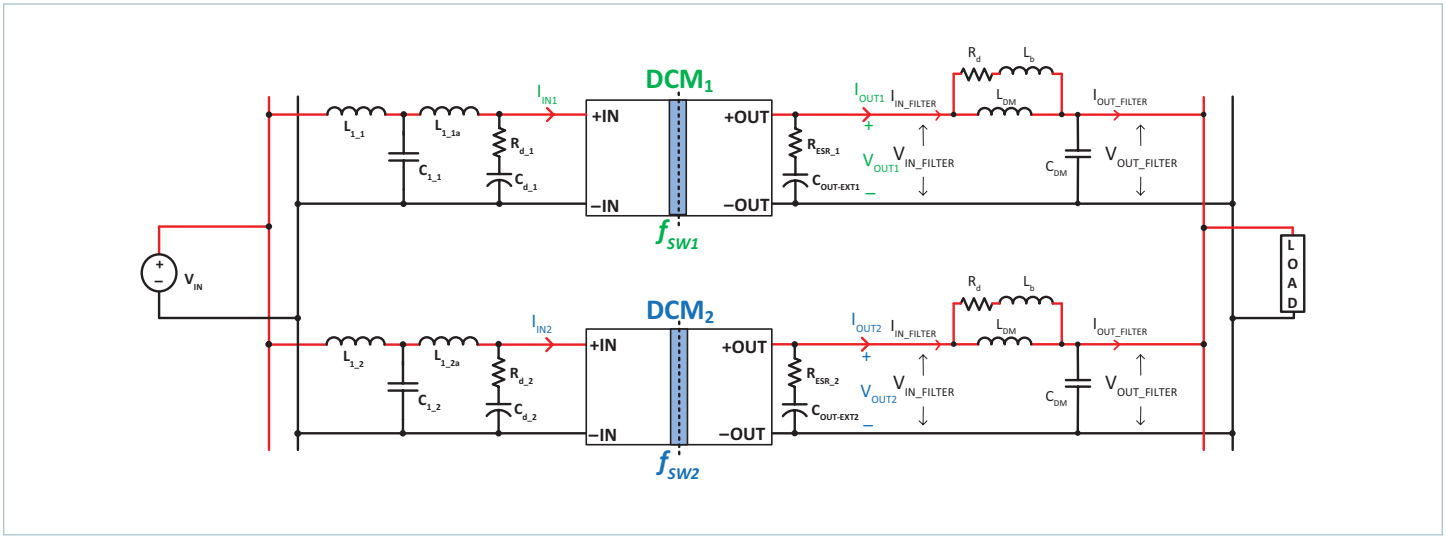


Figure 4.7 — *Parallel array of DCMs with decoupling filter networks on input and output side*

Demonstration of the Effect of Input and Output Filters on the Beat Frequency Oscillations:

To demonstrate the beat frequency oscillations in parallel operation of the DCMs, a two-up parallel configuration of DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) without any input and output filter is considered, shown in Figure 4.6. The test results shown in Figure 4.8 show that the there is a significant amount of beat frequency oscillations in both the input and output currents, the frequency of the beat noise is approximately 583Hz. This is because of the interference between the input and output side of parallel DCMs. As mentioned earlier, the interference can lead to high circulating currents and could potentially cause stress to the internal components of the DCM. From the waveform shown in Figure 4.8, it can be observed that the RMS amplitude of the input current noise is approximately 95.9mA (CH1: Yellow) and output noise current is 28.3mA (CH3: Blue). The test results for 270V_{DC} and 420V_{DC} input voltage are shown below in Figure 4.9 and 4.10.

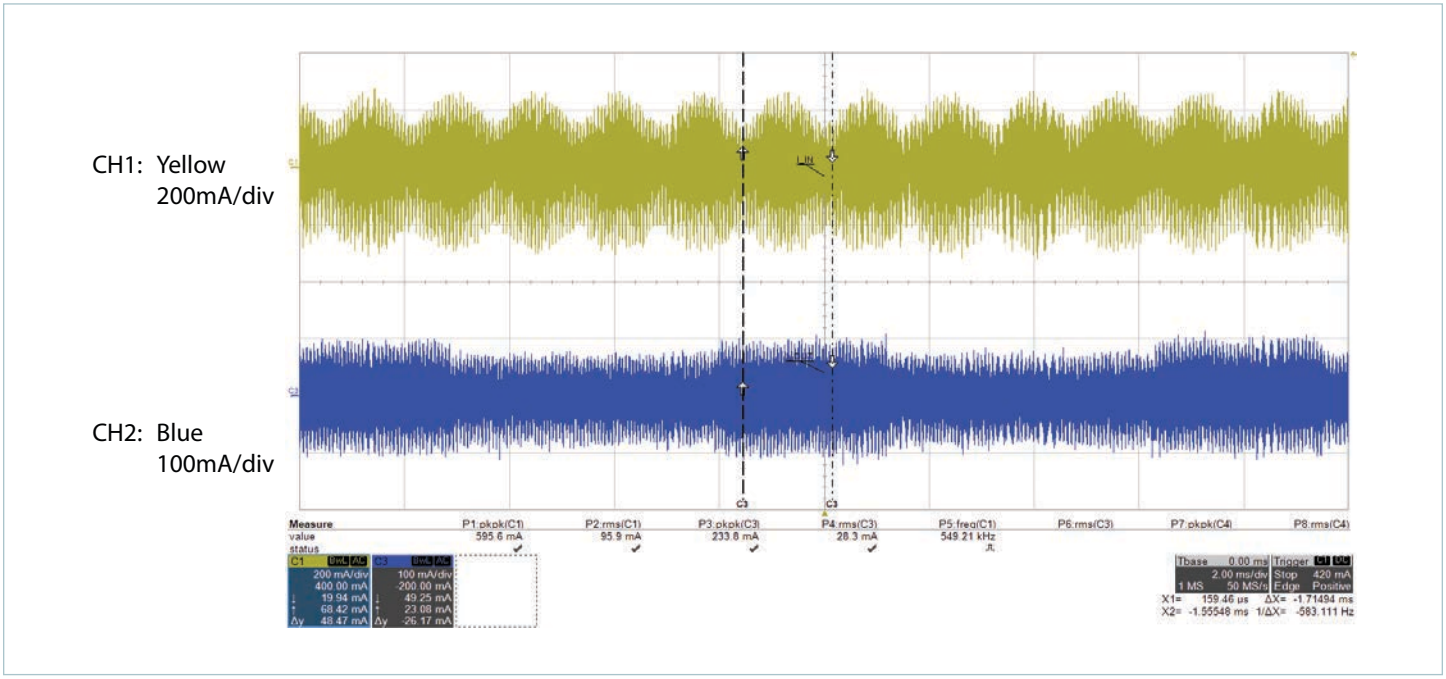


Figure 4.8 — *Two-up parallel array without input and output filters, V_{IN} = 160V_{DC}, full load*

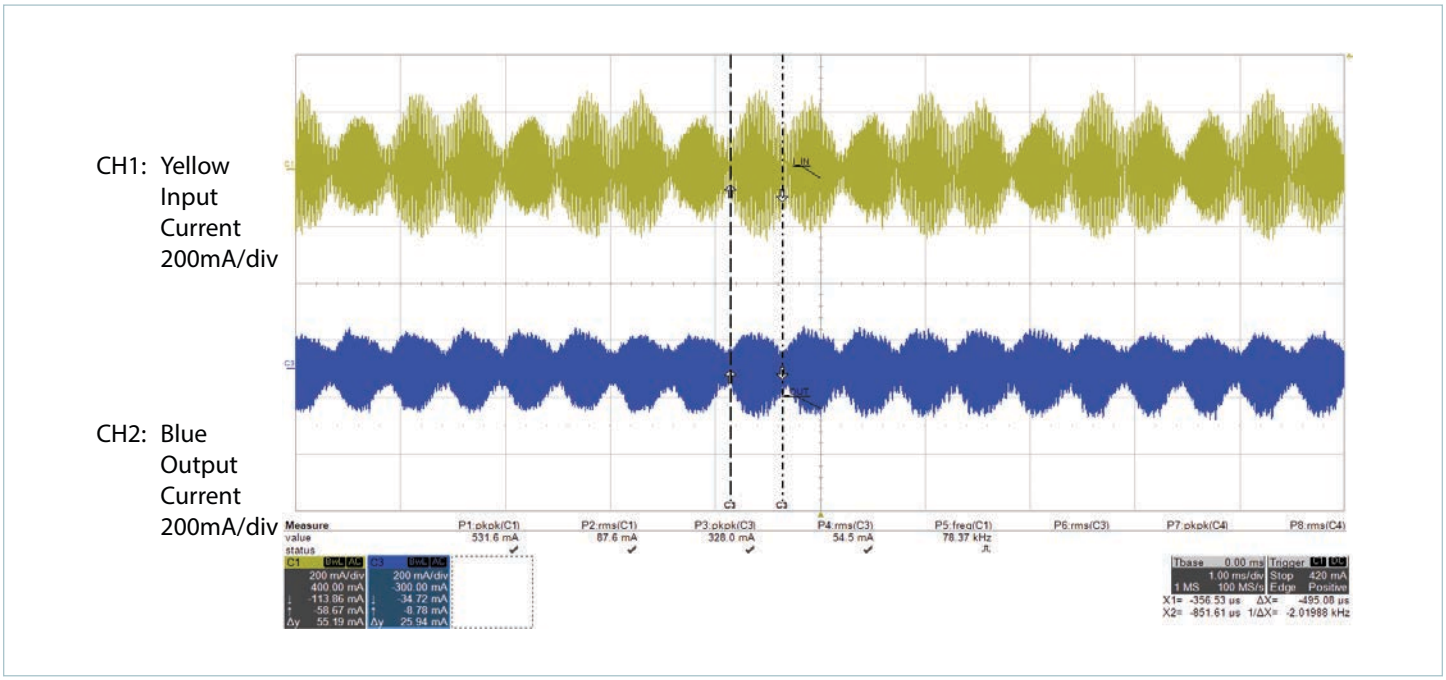


Figure 4.9 — *Two-up parallel array without input and output filters, V_{IN} = 270V_{DC}, full load*

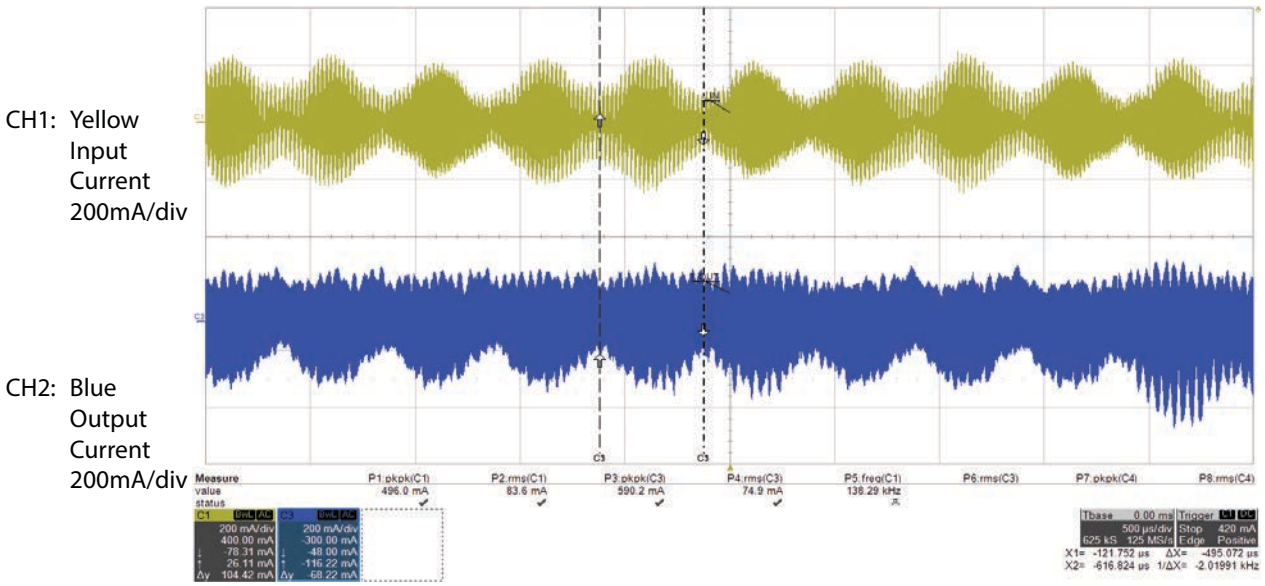


Figure 4.10 — *Two-up parallel array without input and output filters, V_{IN} = 420V_{DC}, full load*

From the waveform shown in Figure 4.9, 4.10, it can be seen that there is an interference between the parallel DCMs at higher input voltages as well.

To avoid the interaction between the DCMs, a filter on each DCM's input and output is added as shown in Figure 4.7. Following is the list of components that are used for input and output filters.

Input Filter

Reference Designator	Value	Mfg. Part Number & Count/DCM
C_{1_1}	6.6µF	C5750X6S2W225K250KA, #3
L_{1_1}, L_{1_2}	15µH	SRP1038A-150M, #1
R_{d_1}, R_{d_2}	1.5Ω	RK73B3ATTE1R5J, #1
C_{d_1}, C_{d_2}	13.2µF	C5750X6S2W225K250KA, #6
L_{1_1a}, L_{1_2a}	0.22µH	SRP4020-R22M, #1

Output Filter

Reference Designator	Value	Mfg. Part Number & Count/DCM
C_{2_1}	80µF	GRM32EC72A106KE05L, #8
L_{2_1}, L_{2_2}	0.33µH	744309033, #1
R_{d_1}, R_{d_2}	0.05Ω	RL2512FK-070R05L, #1
L_{b_1}, L_{b_2}	72nH	IFLR2727EZER72NM01, #1

It can be noticed in Figure 4.11 that the beat frequency oscillations are significantly reduced at 160V_{DC} input voltage. However, the beat frequency oscillations are still present when the input voltage is set to 270V_{DC} and 420V_{DC}, please refer to Figure 4.12 and 4.13. This is due to the common mode noise; at higher input voltages, the effect of common mode noise is significant. As a result, there is interference between the parallel DCMs, leading to the beat frequency oscillations. Therefore, a common mode choke (T1) of 1mH/10A is added at the common input of the parallel configuration of the DCMs, shown in Figure 4.14. Figure 4.15, 4.16, and 4.17 shows the measurements of the input current (CH1: Yellow) and output current (CH2: Blue). It can be observed that the common mode noise interference is significantly reduced on both the input and output of the parallel DCMs for 160 – 420V input voltage range.

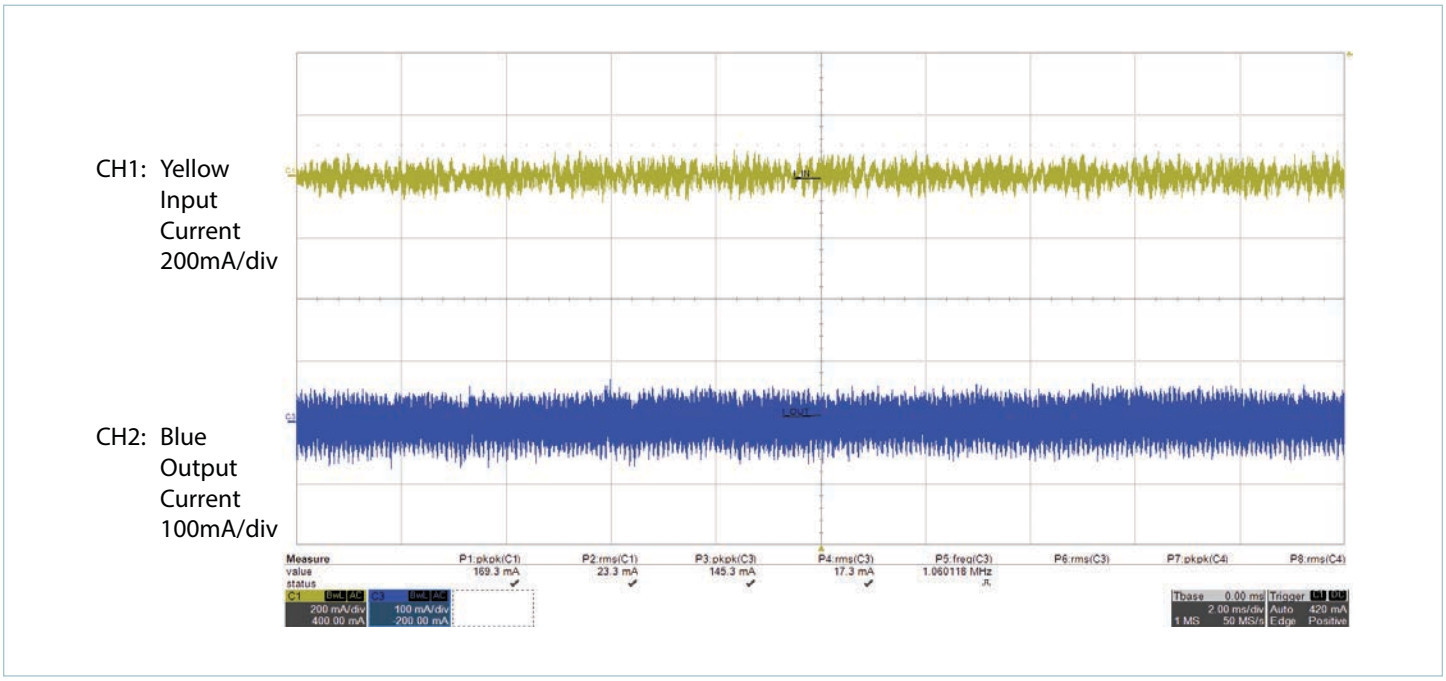


Figure 4.11 — *Two-up parallel array with input and output filters, V_{IN} = 160V_{DC}, full load*

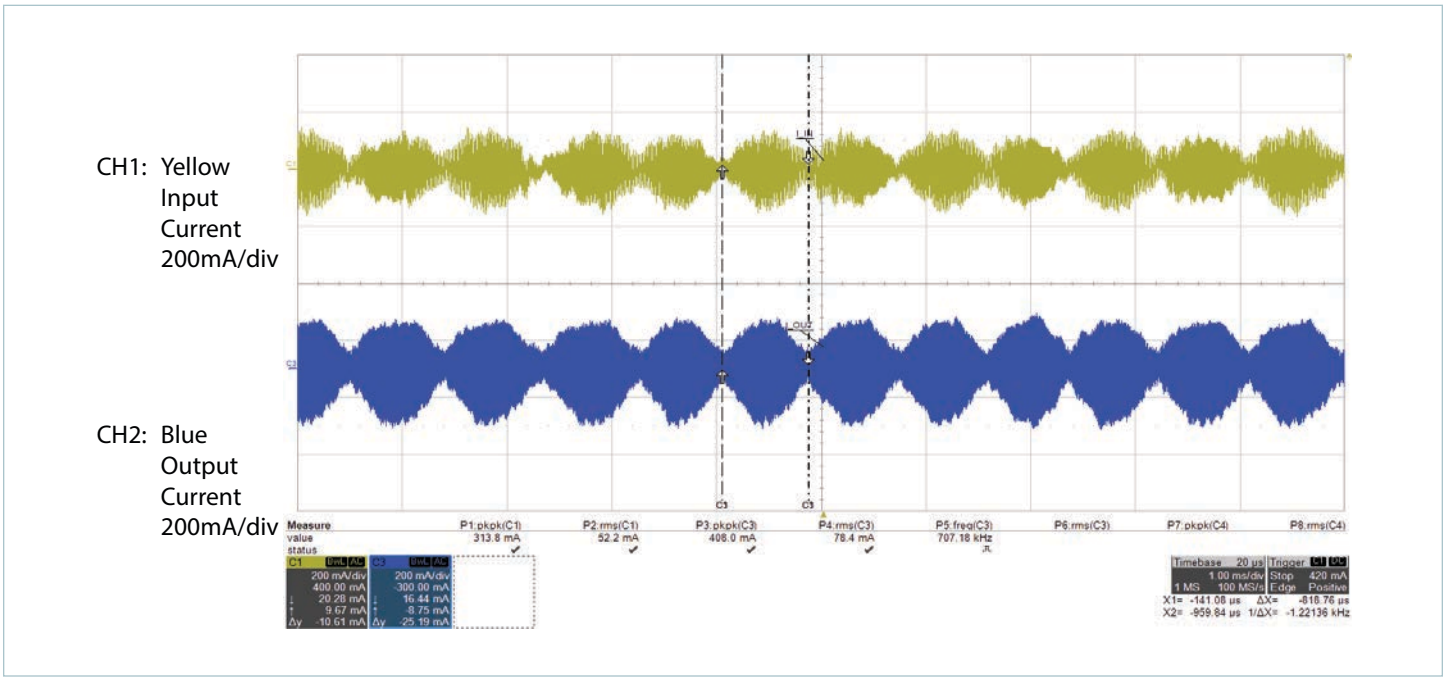


Figure 4.12 — *Two-up parallel array with input and output filters, V_{IN} = 270V_{DC}, full load*

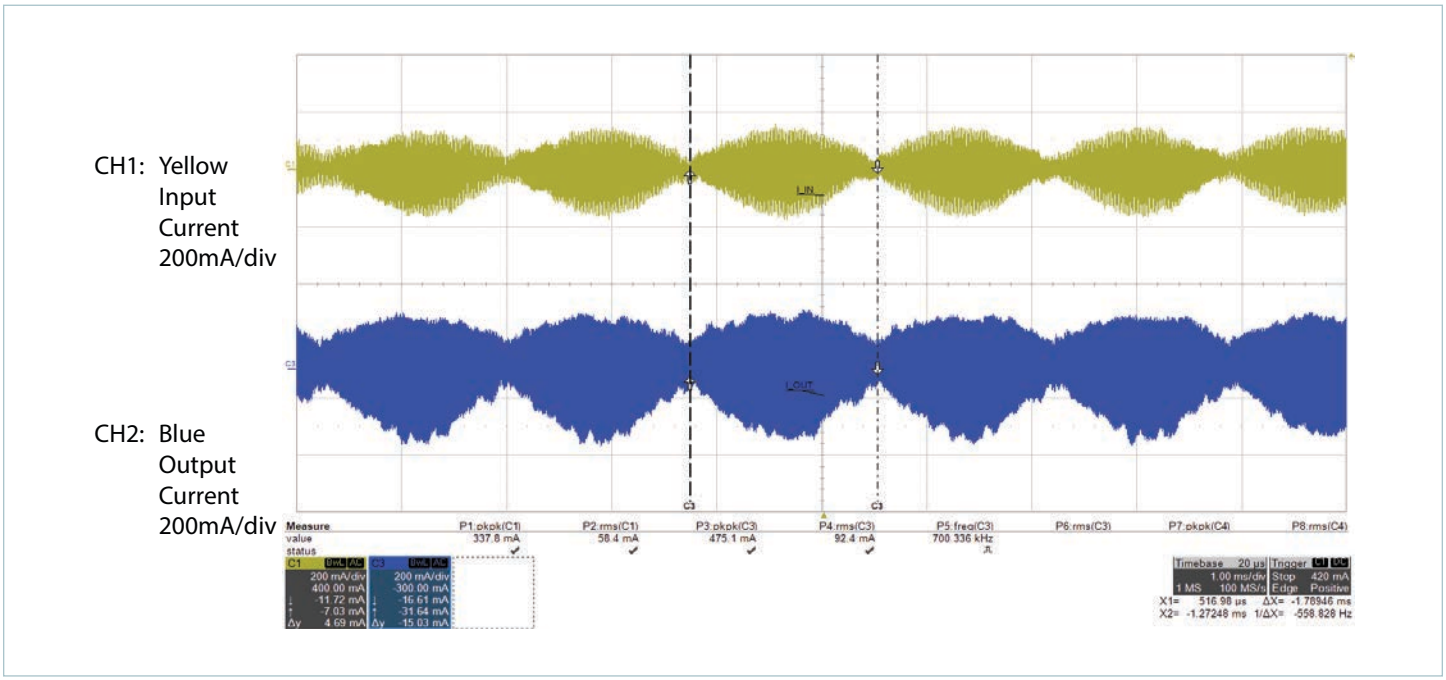


Figure 4.13 — *Two-up parallel array with input and output filters, V_{IN} = 420V_{DC}, full load*

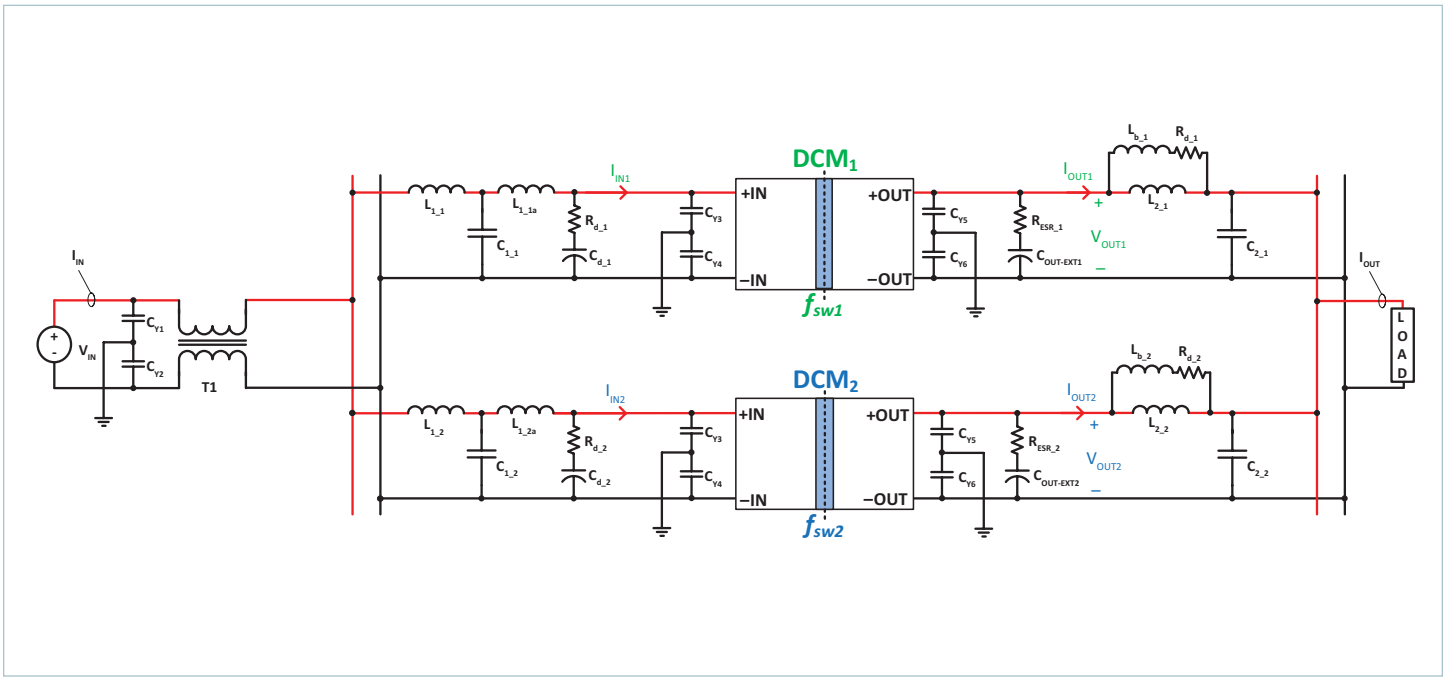


Figure 4.14 — *Two-up parallel array with input, output filters and a common mode choke on the input*

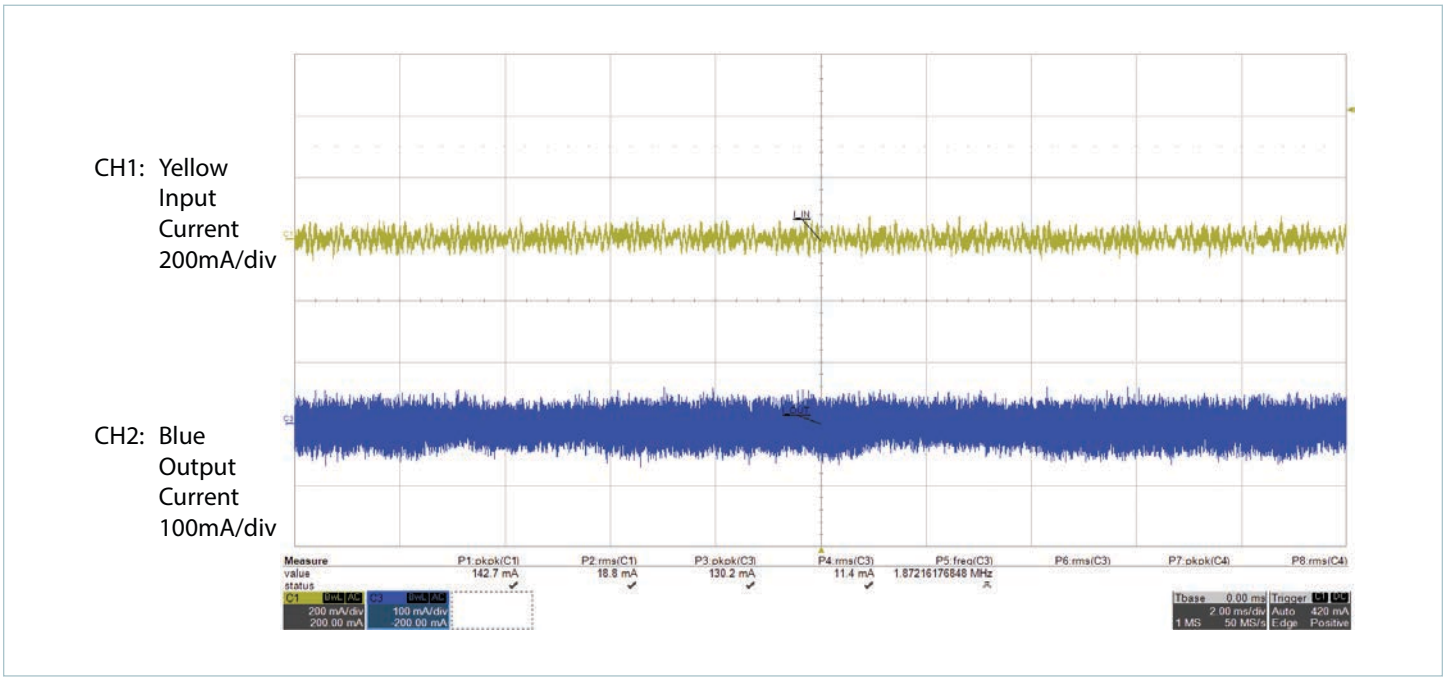


Figure 4.15 — *Two-up parallel array with input, output filters and a common mode choke on the input, V_{IN} = 160V_{DC}, full load*

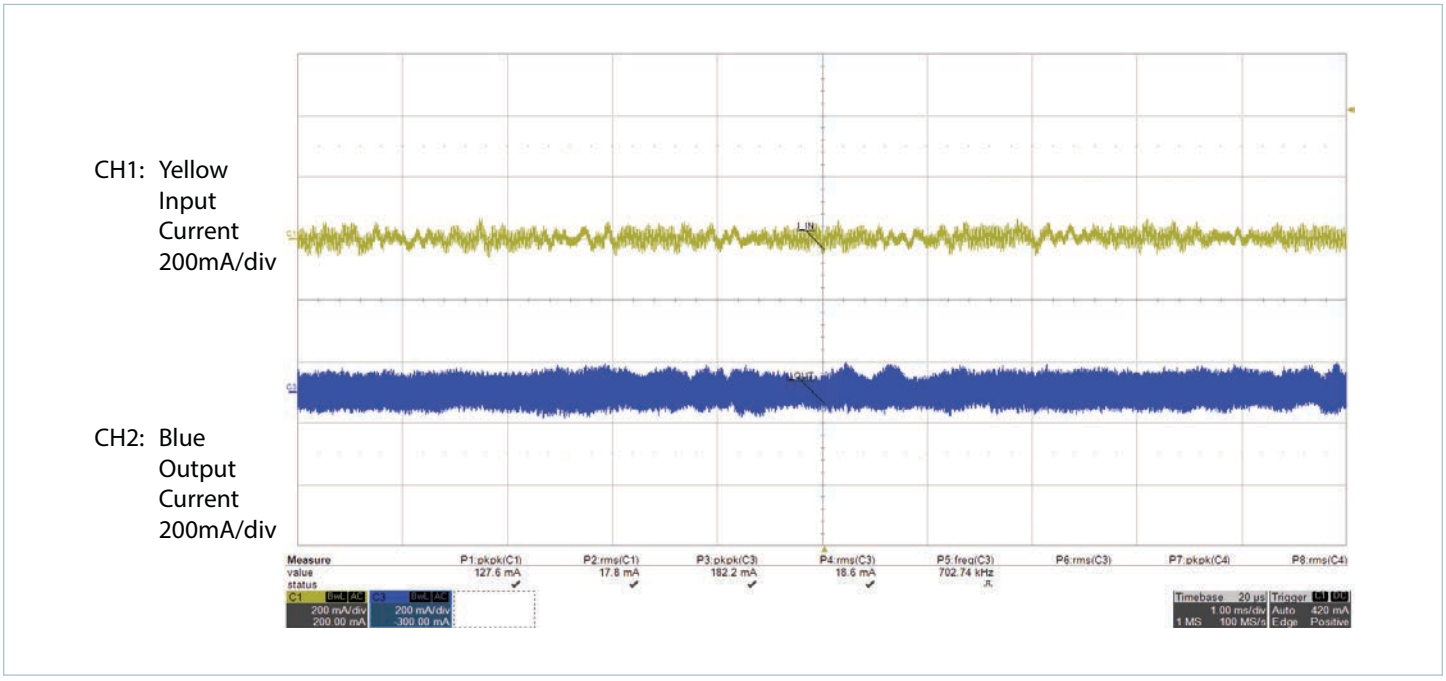


Figure 4.16 — *Two-up parallel array with input, output filters and a common mode choke on the input, V_{IN} = 270V_{DC}, full load*

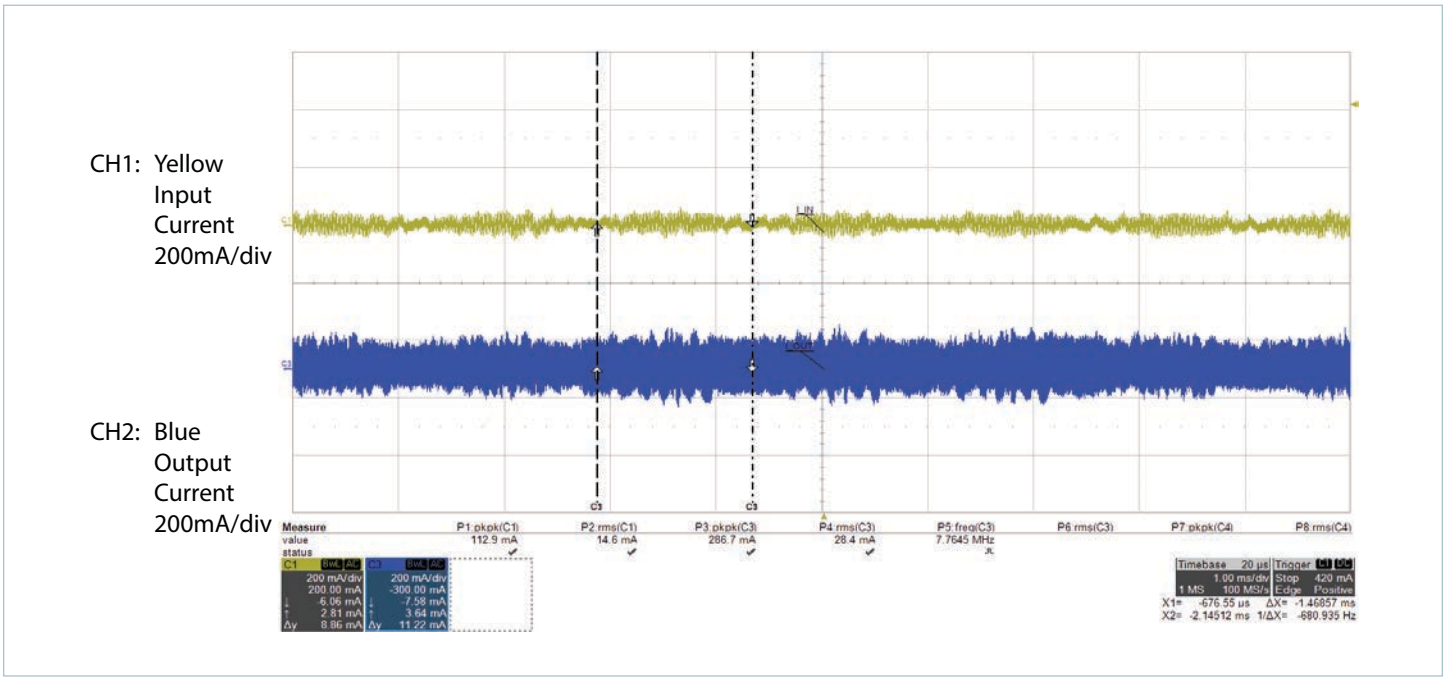


Figure 4.17 — *Two-up parallel array with input, output filters and a common mode choke on the input, V_{IN} = 420V_{DC}, full load*

Introduction

The DC-DC Converter Module (DCM) provides isolation, regulation, fault protection and monitoring in a single module. Through a negative slope load line and temperature coefficient, DCM arrays implement wireless current sharing. For single DCM circuits, DCM model with enhanced regulation are available. For parallel operation, the DCM models optimized for array operation rely on a load line for current sharing. The nominal load regulation is 5% (see the $\%V_{OUT-LOAD}$ specification in the DCM data sheet), excluding other regulation error terms. This may not be sufficient for applications that have tight voltage regulation requirements. In those applications, an isolated analog feedback loop, such as the one shown in Figure 5.1, can be used to improve the load regulation performance. The circuit shown here is recommended for general use in high-accuracy applications that need to preserve the input-output isolation offered by the DCM. The circuit is applicable to single DCMs as well as arrays of up to eight units.

For array applications, on the primary side, after any needed differential-mode filtering, the DCMs must share a common –IN node, which is also the ground reference for the remote-sense sub-circuit output. The DCM TR pins are all driven by single output of the remote-sense sub-circuit, so it is important to minimize voltage differences between the various DCM –IN pins through careful layout techniques. On the secondary side, the remote-sense sub-circuit senses the output voltage through the R1/R2 resistor network, compares that to a reference voltage, and converts the error voltage into a trim voltage for the whole array.

Since the DCMs are all effectively programmed to the same trim voltage, the current sharing between modules is still the same as it would be without the remote-sense circuit, as covered in section on "Parallel Operation".

This circuit works with all "Array Optimized" ChiP DCM type, and achieves a regulation accuracy of ±1% at all line, load, temperature and trim conditions.

Circuit Schematic

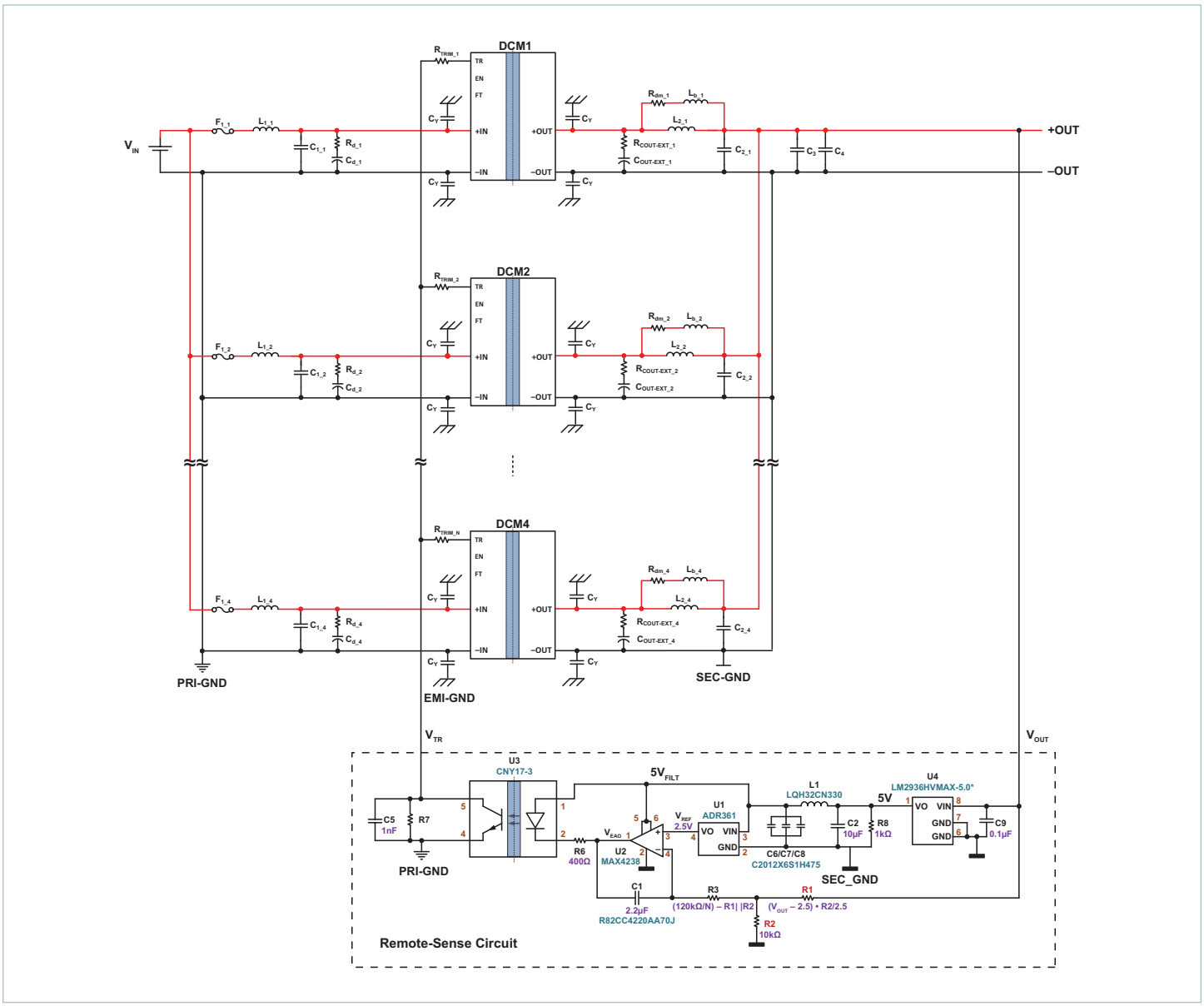


Figure 5.1 — *Remote-sense circuit for DCM*

Functional Description of Remote-Sense Circuit

The output voltage is sensed through resistor network R1 and R2 relative to secondary ground SEC-SGND; the sensed voltage becomes:

$$V_{OUT} \bullet \frac{R2}{R1 + R2} \qquad (5.1)$$

1. The sensed voltage is compared to the reference voltage V_{REF}, which in this schematic is generated by the 2.5V reference U1.

$$V_{REF} = 2.5V \qquad (5.2)$$

1. If another V_{REF} voltage is preferred, V_{REF} is recommended to be between 1.5V and 3V for optimum noise immunity.
2. The difference gets accumulated by an integrating error amplifier (consisting of R3, C1 and U2), which generates V_{EAO}.
3. The difference between V_{EAO} and 5 V_{FILT} drives the input of the optocoupler U3.
4. The optocoupler (U3) is used to preserve the galvanic isolation of the DCM array.
5. The output of U3 is its collector current. That current develops a voltage drop across the R_{TRIM_x} and $R_{TRIM\text{-}INT\_x}$ resistors and establishes the DCM trim pin voltages. (The $R_{TRIM\text{-}INT\_x}$ are the internal pull-up resistors inside each DCM. Each $R_{TRIM\text{-}INT\_x}$ pulls up to VCC, the DCM's internally generated 3.3V supply.) Figure 5.2 details how the trim pin voltages are generated, along with a simplified model for N DCMs in parallel. The R_{TRIM_x} resistors are all the same nominal value, as are all of the $R_{TRIM\text{-}INT\_x}$ resistors.
6. If the sensed version of V_{OUT} is less than V_{REF}, the error amplifier output rises, and the drive current into the optocoupler's LED is reduced. This in turn reduces the optocoupler's (output) collector current, permitting the pull-up resistors to pull the trim voltage higher, which raises each DCMs programmed output trim voltage. Conversely, if V_{OUT} is too high, the DCM trim pin voltages are similarly driven lower, which lowers V_{OUT}.
7. R6 is chosen to set the voltage transfer ratio of the optocoupler, to ensure that it operates as expected over temperature and with age (see Appendix I).
8. R7 establishes a minimum load on the TR pins by setting the maximum trim bus voltage.
   a. R7 must be chosen so that the maximum trim voltage will be below the TR trim enable threshold, even with no optocoupler current; some margin is needed so that trim remains enabled in the presence of noise.
   b. The value of R7 may be further reduced, to limit the maximum trim voltage, which can be helpful in reducing overshoot during load transients and start up. For N DCMs in parallel, the trim voltage input to the DCM, $V_{TR'\_x}$ (see Figure 5.2), can be calculated as:

$$V_{TR'max} = 3.3 \bullet \frac{N \bullet R7 + R_{TRIM\_x}}{N \bullet R7 + R_{TRIM\_x} + R_{TRIM\text{-}INT\_x}} \qquad (5.3)$$

Where R_{TRIM_x} = 301Ω, $R_{TRIM\text{-}INT\_x}$ = 10kΩ as specified in the DCM data sheet, N is the number of DCMs in parallel.

Thus the maximum trim voltage input can be calculated as:

$$V_{TR'max} = 3.3 \bullet \frac{N \bullet R7 + 301}{N \bullet R7 + 10301} \qquad (5.4)$$

For example, if the trim voltage is to be limited to 3V, the value of R7 can be chosen as:

$$R7 = \frac{100k\Omega}{N} \qquad (5.5)$$

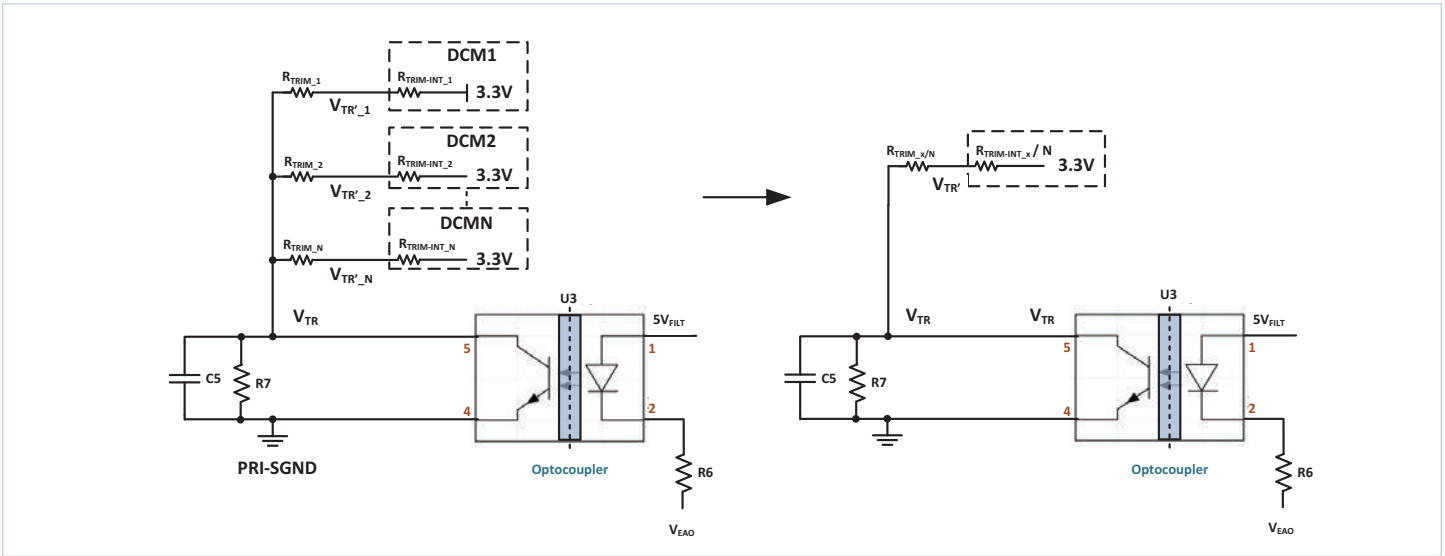


Figure 5.2 — *Trim voltage generation method and its simplified model*

C5 is a low-value ceramic capacitor, such as 1nF, which is used to exclude high-frequency noise from V_{TR}.

9. The bus that is used to supply U1, U2 and U3 is generated from V_{OUT}. Through this method, no external 5V power supply is needed. U4 regulates V_{OUT} to an unfiltered 5V, which is called 5V in Figure 5.1. This 5V then goes through the filter network (C2, L1, C6-C8) and becomes a filtered 5V, which is called $5V_{FILT}$. R8 discharges the filter capacitors when V_{OUT} is off. The output of this circuit is the $5V_{FILT}$ bus that supplies U1, U2 and U3.

10. Optionally, U4/C6-C8/L1/C2/R8 can be removed from the circuit if a precision external 5V power supply with at least 50mA capability is available to drive the $5V_{FILT}$ bus. The benefit of using an external 5V power supply is that it uses fewer components. The disadvantage is that if the external supply is energized before the DCMs are enabled, then the error amplifier will "wind up" to a maximum trim condition. When the DCMs are started, the system output voltage will significantly overshoot the set point until the integrator unwinds. When using an external 5V power supply, R7 should be chosen carefully so that V_{OUT} does not exceed the maximum voltage allowed by the application, or the DCMs should be enabled prior to energizing the external 5V supply node.

Through this method, the output voltage of the DCM can be trimmed to:

$$V_{OUT} = V_{REF} \bullet \frac{R1 + R2}{R2} \qquad (5.6)$$

The maximum cut off frequency of the whole loop is 30Hz, but with CTR variance, temperature, and aging of the optocoupler, it can be as low as approximately 7.5Hz.

V_{OUT}	U4 Recommendation	Comment
$6V \le V_{OUT} \le 60V$	Use LM2936HVMAX-5.0 for U4	
$V_{OUT} \le 6V$	Use an appropriate regulator for U4 so that the output voltage of U4 will be between 4V and 5.5V, or use an independent supply rail in the application	For DCM modules with a rated $V_{OUT-NOM}$ of 5V or 3.3V, for example.

Table 5.1 — *Notes for the choice of U4*

Component Selection

The detailed schematic of the DCM remote-sense circuit has been shown in Figure 5.1, with IC device types and component values. The generic components' part numbers have not been marked in the schematic. Unconnected pins have not been shown for simplicity.

The recommended components for the remote-sense circuit are summarized here (excluding the generic components):

Part ID	Type	Manufacturer Part Number	Digi-Key Part Number	Note
C1	CAP FILM 2.2µF 50V_{DC} RADIAL	R82CC4220AA70J	399-6027-ND	Low leakage, low dielectric absorption
U1	IC V_{REF} SERIES 2.5V TSOT23-5	ADR361BUJZ-REEL7	ADR361BUJZ-REEL7CT-ND	High precision
U2	IC OPAMP GP 1MHZ RRO SOT23-6	MAX4238AUT+T	MAX4238AUT+TDKR-ND	Low input offset voltage, low input offset current, low supply consumption, but not necessarily high bandwidth or high slew rate
U3	OPTOISO 5KV TRANS W/BASE 6SMD	CNY17-3X017T	CNY17-3X017TCT-ND	5kV isolation; Current Transfer Ratio no less than 100% @ 10mA
U4	IC REG LDO 5V 50MA 8SOIC	LM2936HV-MAX-5.0/NOPB	LM2936HVMAX-5.0/NOPBCT-ND	See Table 5.1
C6/C7/C8	CAP CER 4.7µF 50V 20% X6S 0805	C2012X6S1H-475M125AC	445-7600-1-ND	
L1	IND 33µH 10% 200mA	LQH32CN330K53L	490-4062-1-ND	

Table 5.2 — *Recommended components for remote-sense circuit*

R1, R2 and R7 may vary according to the application and DCM module. Consider the following before choosing these values:

a. R1/R2 = $V_{OUT}/V_{REF} - 1$, V_{OUT} is the trimmed DCM output voltage.

b. Choose high-accuracy resistors (up to 0.1% accuracy) for R1 and R2; their accuracy directly relates to the resultant output voltage set point.

c. Choose R2 = 10kΩ; then the resistance of R1 can be calculated as:

$$R1 = \frac{V_{OUT} - 2.5}{2.5} \bullet R2$$

This will minimize current consumption and power dissipation in the divider network, while maintaining good immunity from noise and effects of bias currents from amplifier input. With R2 being fixed at 10kΩ, a high-accuracy resistor value for R1 may not be available. In that case, the nominal value of R2 can be adjusted to be within ±10% of 10kΩ.

d. R7 limits the maximum programmed trim for the DCMs. Use Equation 5.3 to determine the value of R7.

Loop Compensation

When trim is active, the DCM TR pin provides dynamic trim control of the module's output voltage with at least 30Hz of (small signal) control bandwidth over the output voltage of the DCM converter. The phase shift at 30Hz is approximately 45°.

The whole open loop transfer function at 30Hz or below can be calculated as:

$$A(s) = A_{TR}(s) \bullet \frac{R2}{R2 \bullet R1} \bullet \frac{1}{R3' \bullet C1 \bullet s} \bullet C_{TR} \bullet \frac{R_{TRIM\text{-}INT\_x}}{N \bullet R6} \quad (5.7)$$

Where C_{TR} is the Current Transfer Ratio of the optocoupler, which is specified in the optocoupler data sheet;

$$R3' = R3 + \frac{R1 \bullet R2}{R1 + R2}$$

recall that N is the number of DCM modules in parallel.

For frequencies less than or equal to 30Hz, the analysis is as follows:

$$V_{OUT} \bullet \frac{R2}{R1 + R2} = 2.5 \quad (5.8)$$

A_{TR} (s) is the transfer function from TR to V_{OUT}, which is a constant A_{TR} at very low frequency and ≤A_{TR} at 30Hz.

Rearranging the equality:

$$\frac{R2}{R2 + R1} = \frac{2.5}{V_{OUT}} \quad (5.9)$$

Multiplying both sides by A_{TR} (s),

$$A_{TR}(s) \bullet \frac{R2}{R2 + R1} = \frac{2.5 \bullet A_{TR}(s)}{V_{OUT}} \quad (5.10)$$

The term 2.5 • A_{TR} (s) / V_{OUT} increases with increasing trim range. For existing DCMs, the widest trim range is –40% to 10% of V_{OUT_NOM}. For these DCMs, 2.5 • A_{TR} / V_{OUT_MIN} ≈ 1

Therefore:

$$A_{TR}(s) \bullet \frac{R2}{R2 + R1} \le 1 \quad (5.11)$$

Inserting this result into Equation 5.7:

$$A(s) \le 1 \bullet \frac{1}{R3' \bullet 2.2\mu F \bullet s} \bullet C_{TR} \bullet \frac{10k\Omega}{N \bullet 400} \quad (5.12)$$

If R3 is chosen so that A(s) goes to 0dB at 30Hz, the whole system will have approximately 45° phase margin.

Setting A(s) to 0dB at 30Hz results in:

$$R3' = \frac{60k\Omega \bullet C_{TR}}{N} \quad (5.13)$$

For the optocoupler used in the schematic, the maximum C_{TR} is in the range of 1 to 2. So for the worst case gain, C_{TR} = 2:

$$R3' = \frac{120k\Omega}{N} \quad (5.14)$$

$$R3 = \frac{120k\Omega}{N} - \frac{R1 \bullet R2}{R1 + R2} \quad (5.15)$$

Test Results (Steady State, Start Up, and Transient)

Steady State Load Regulation

Using the DCM4623TD2H53E0T00 as an example, the results for an array of eight DCMs are shown in Figure 5.3.

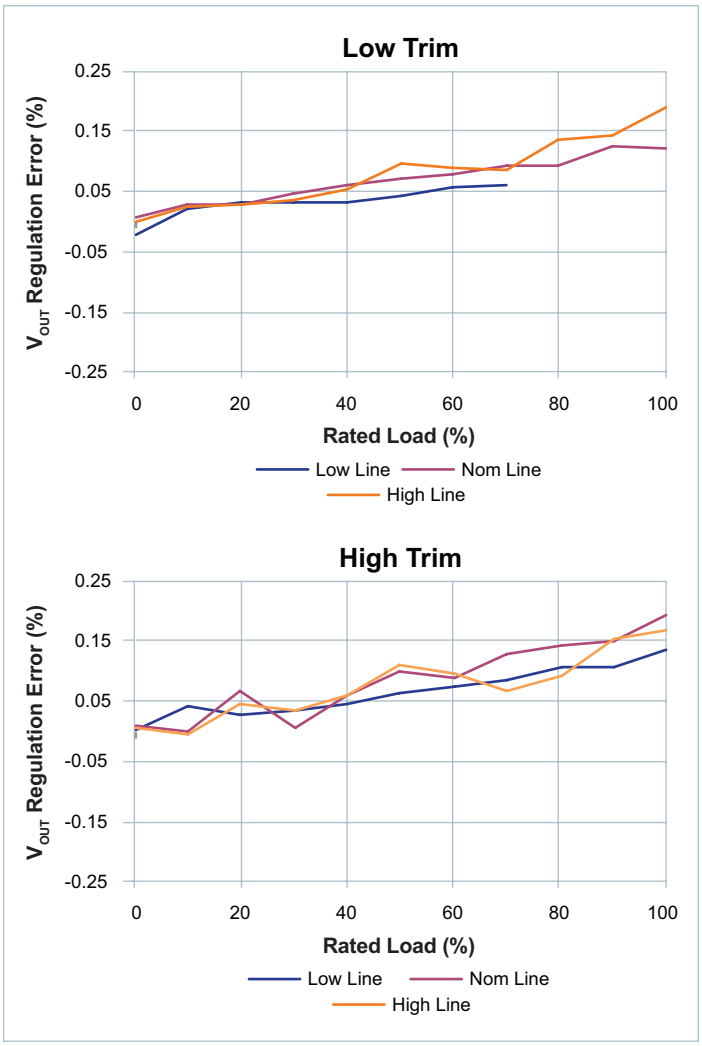


Figure 5.3 — *Test results for an eight-up DCM4623TD2H53E0T00 array with this remote-sense circuit*

Start Up

Typical start-up waveforms are shown in Figure 5.4 and Figure 5.5. During start up, once V_{OUT} reaches U4's minimum input voltage, U4 will generate the 5V bus to supply U1, U2 and U3. The waveform of the start up typically comes in two stages: in the first stage, V_{OUT} rises to the minimum trimmed V_{OUT}; in the second stage, the circuit comes to the steady state and brings V_{OUT} to the correct trimmed value.

This circuit needs to be started up after V_{OUT} and the 5V bus have fully discharged to avoid trimming to the highest V_{OUT}.

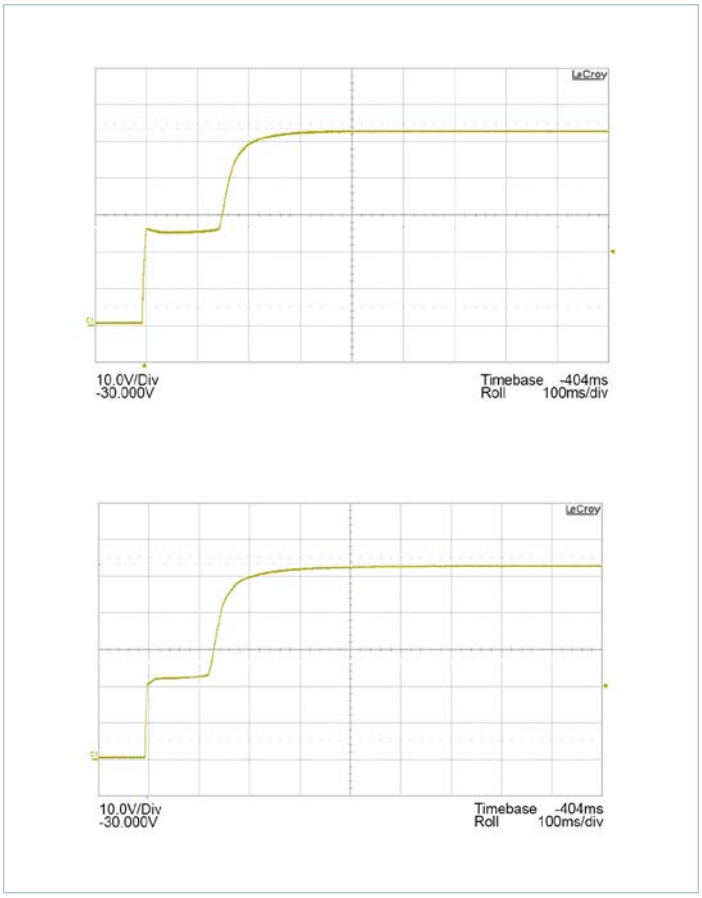


Figure 5.4 — *Test results for a single DCM4623TD2H53E0T00 (low line, maximum external C_{OUT}) start up into high trim with this remote-sense circuit*

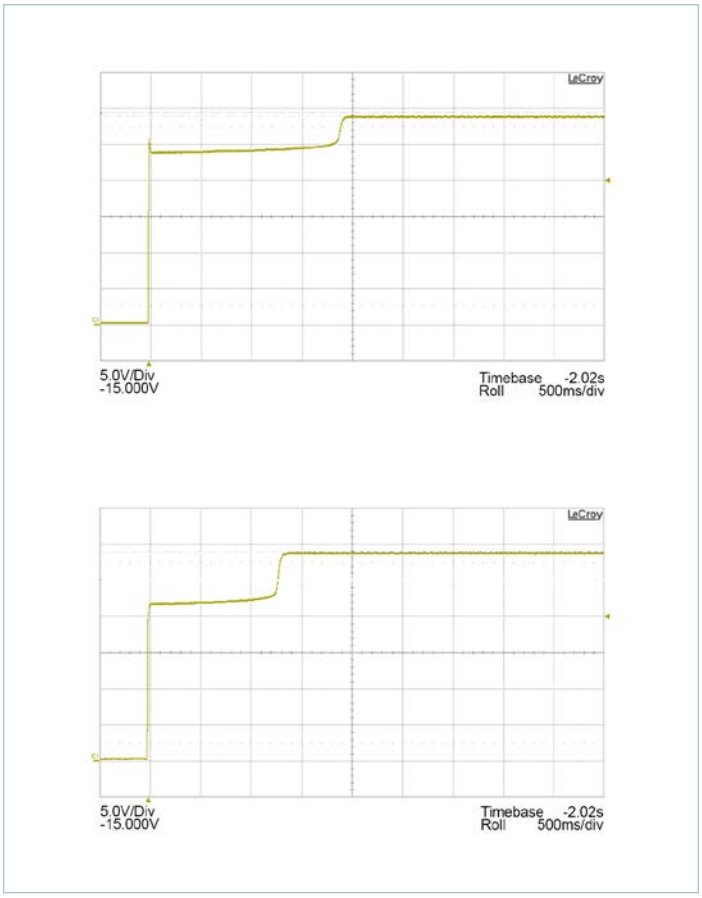


Figure 5.5 — *Test results for a single DCM4623TD2H53E0T00 (high line, maximum external C_{OUT}) start up into low trim with this remote-sense circuit*

Load Transient Response

There is a delay from the transient until the circuit reaches the corrected output voltage, which is due to the limited bandwidth of the DCM TR pin and remote-sense circuit. Because of this narrow bandwidth, the remote-sense circuit doesn't affect the initial response to a transient. Figure 5.6 shows a comparison of transient response without the remote-sense circuit to the response with the remote-sense circuit in operation.

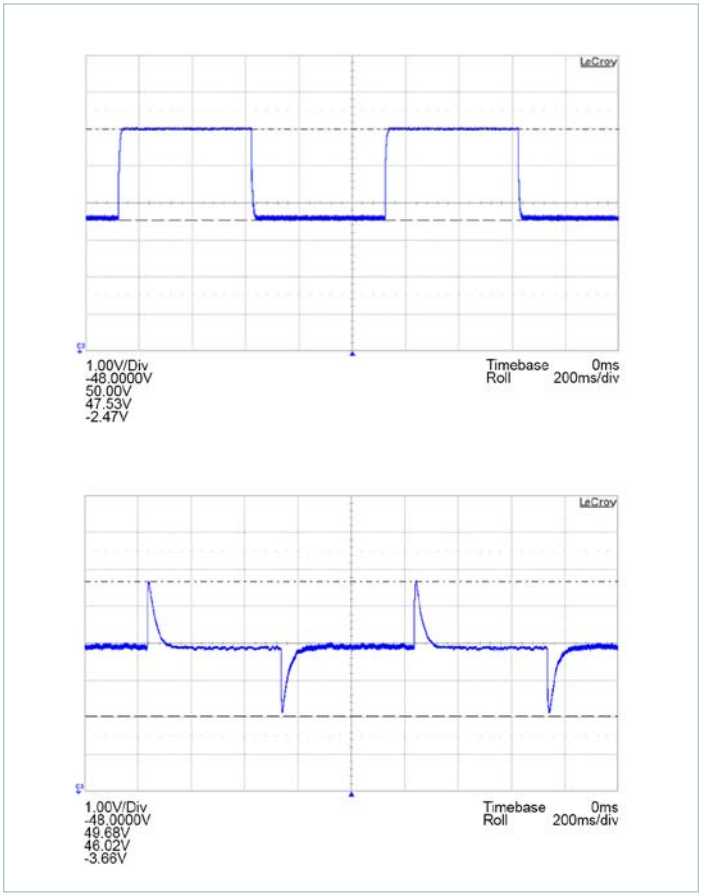


Figure 5.6 — *Comparison of a single DCM4623TD2H53E0T00 transient response (nominal line, nominal trim, electronic load in CC mode 10 – 100% load transient) without the remote-sense circuit and with the circuit included*

Conclusion

Using the remote-sense circuit shown here, DCM-based voltage regulators can achieve output voltage accuracy of ±1%. Within the 30Hz bandwidth of the circuit, other aspects of DCM operation are unchanged. This method works for any number of DCMs in parallel, up to eight.

Appendix I. Choosing R6 to Account for CTR Variance in the CNY17-3 Over Temperature and Time

1. Information from Vishay CNY17 data sheet

CURRENT TRANSFER RATIO (T_{amb} = 25 °C, unless otherwise specified)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
I_C/I_F	V_{CE} = 5 V, I_F = 10 mA	CNY17-1	CTR	40		80	%
		CNY17-2	CTR	63		125	%
		CNY17-3	CTR	100		200	%
		CNY17-4	CTR	160		320	%
	V_{CE} = 5 V, I_F = 1 mA	CNY17-1	CTR	13	30		%
		CNY17-2	CTR	22	45		%
		CNY17-3	CTR	34	70		%
		CNY17-4	CTR	56	90		%

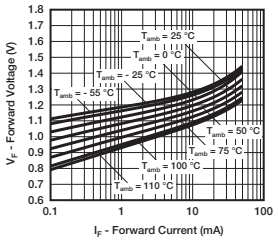


Fig. 5 - Forward Voltage vs. Forward Current

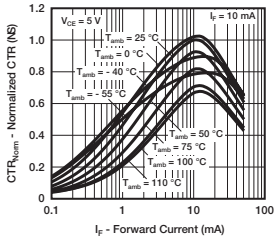


Fig. 11 - Normalized CTR (NS) vs. Forward Current

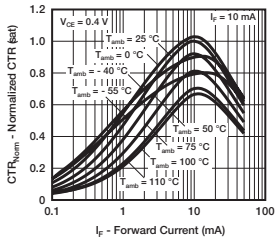


Fig. 12 - Normalized CTR (sat) vs. Forward Current

2. Calculation of CNY17-3 controller current achievable over temperature and time:

- Choosing R6 = 400Ω, a supply voltage of 4V (the lowest value specified in Table 5.1), C_{TR} = 100% and estimating the voltage drop across the optocoupler at 1.28V, the maximum forward current that the secondary side of the remote-sense circuit could have over the full temperature range is approximately (4V – 1.28V)/400Ω = 6.8mA.
- The next step is to find the minimum C_{TR} at I_F = 6.8mA, using linear interpolation on the data in the table for I_F = 1mA and I_F = 10mA. This results in a minimum C_{TR} of ((10mA – 6.8mA) • 34% + (6.8mA – 1mA) • 100%)/(10mA – 1mA) = 76.5% at 25ºC
- From the Normalized C_{TR} curves above, C_{TR} could decrease to 60% of its peak value over temperature, which is 76.5% • 60% = 45.9%
- From Vishay reliability data, C_{TR} is reduced by 15% over 8000 operation hours, giving C_{TR} = 45.9% • (1 – 15%) = 39%
- Thus the collector current will be at least 6.8mA • 39% = 2.65mA, to ensure proper operation with aging.
- Since 3.3V – (2.65V • 1.25) = –0.01V < 0V, this will result in a trim voltage close to 0V, which is sufficient to drive all DCMs to trim low.
- When the forward current is small, the CNY17-3 will be able to drive all DCMs to high trim, so high trim is achievable for any choice of R6.

Thus R6 = 400Ω should be a valid choice for this circuit to work over temperature and time, from single DCMs through arrays of eight DCMs.

Appendix II. Current Regulation

If current regulation is needed instead of voltage regulation, with some modifications, the remote-sense circuit can be adapted to regulate a constant-current output.

Instead of sensing the output voltage with R1 and R2, a shunt resistor is used to measure the output current. The voltage across the shunt resistor is sensed with an additional differential amplifier stage, which feeds R3. R1 and R2 are not present, since the current signal scaling is accomplished by current sense amplifier. The rest of the circuit is unchanged. A typical schematic with the current sense sub-circuit is shown in Figure 5.8.

Notice that current regulation needs to be limited to the minimum rated output current (I_{OUT}) of the DCM, to avoid interfering with the DCM's operational current limit and cause issues.

In applications such as battery charging, the actual V_{OUT} can be different from the trimmed voltage of the DCM. Additional considerations may be needed:

1. The DCM has a minimum V_{OUT} before it might detect output under voltage. For example, the DCM would not be able to charge a battery whose voltage is below V_{OUT_UVP}.
2. The DCM current capability is reduced when the DCM is trimmed higher than nominal (regardless of the actual V_{OUT}), so the output current from the system should be no higher than n • (Rated P_{OUT} / Maximum $V_{OUT-TRIMMING}$) to avoid entering current limit.

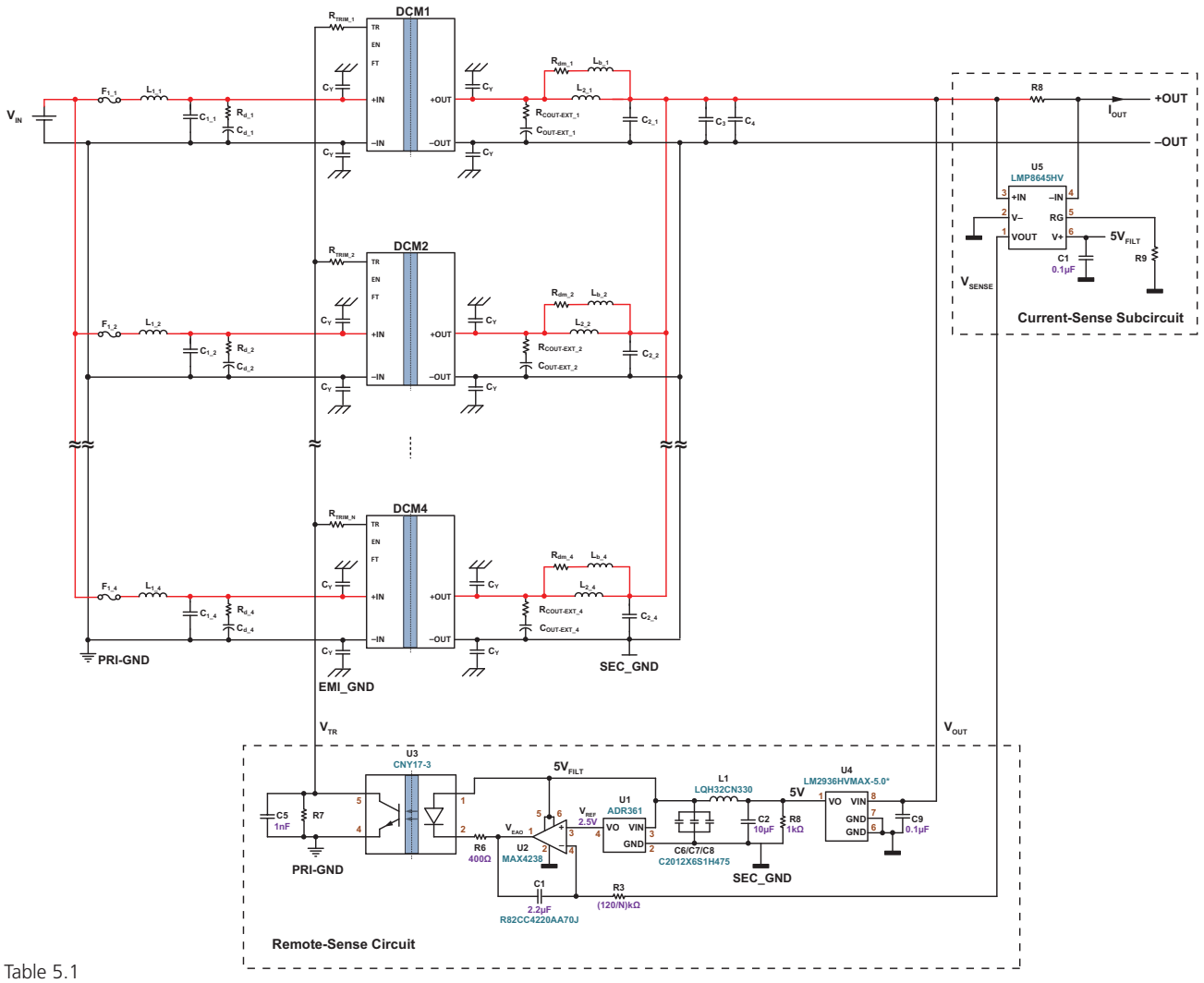
The transfer function between the output current I_{OUT} and the sense voltage V_{SENSE} in Figure 5.8 is:

$$V_{SENSE} = I_{OUT} \bullet R8 \bullet R9 \bullet Gm \qquad (5.16)$$

With an LMP8645HV, the typical Gm is 200µA/V.

Through this method, the total output current of the DCMs can be trimmed to:

$$I_{OUT} = V_{REF} \bullet \frac{1}{R8 \bullet R9 \bullet Gm} \qquad (5.17)$$



*See Table 5.1

Figure 5.8 — *Remote-sense circuit for DCM for current regulation with single current-sense shunt*

In high-current applications, individual current sense resistors for each DCM output may be preferred (as shown in Figure 5.9) over using a single high-dissipation current sense resistor for the entire DCM array. With R81, R82, … R8N all equal to R8, and R91, R92, … R9N all equal to R9, the total output current of the DCMs can be trimmed to:

$$I_{OUT} = V_{REF} \bullet \frac{1}{R8 \bullet R9 \bullet Gm} \qquad (5.18)$$

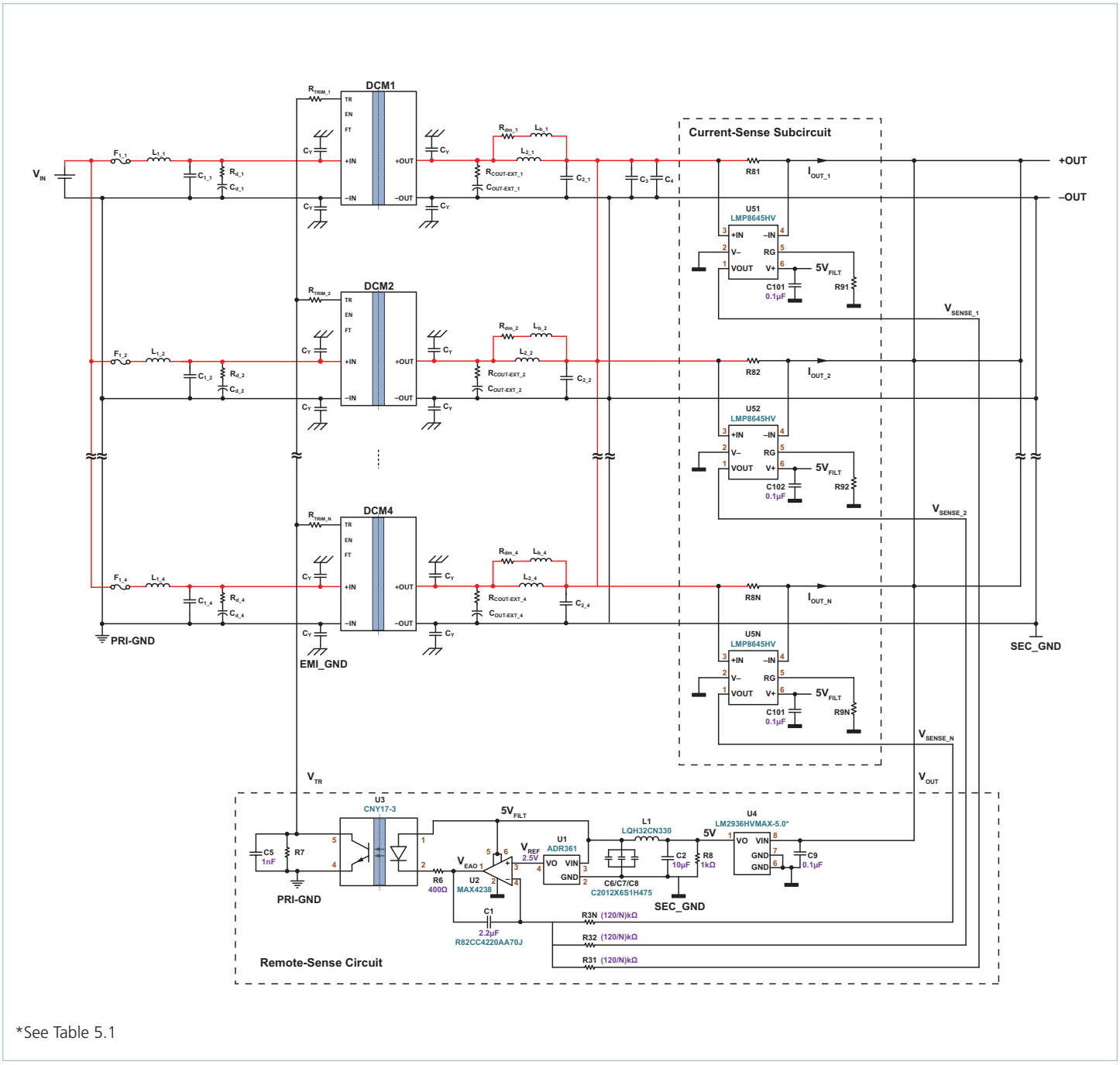


Figure 5.9 — *Remote-sense circuit for DCM for current regulation with individual current-sense shunts*

DCM Input Terminals in Series Configuration

Series input configuration of multiple DCMs will exceed the absolute maximum ratings of the internal components and operates above the electrical Safe Operating Area (SOA) limits. This in turn leads to permanent damage of the DCM. Therefore, it is not an approved and recommended application.

DCM Output Terminals in Series Configuration

NOTE: Series stacking of DCM output is not approved.

Certain applications require high-voltage inputs relative to most standard commercial off-the-shelf (COTS) DC-DC converters that are designed to provide output voltages within the Safety Extra Low Voltage (SELV) levels i.e., <55V. Thus, series configuration of multiple DC-DC converter's output terminals is the preferred method to obtain the single high-voltage output to meet the application requirements. However, with the series output configuration of the DCM, there are several technical issues to the topology of the DCM that make the circuit configuration not feasible. A few issues are: stress to the internal components, start up / restart problems (due to current limitation at start up), possible interaction of current limit protections and meeting regulatory / compliance approvals. Apart from the issues at the component level, the implementation at the system level would introduce several additional issues as well and would require a large amount of external components. Therefore, DCM series output configuration is not recommended and not an approved application. Additionally, please note that since series stacking of DCMs is a non-approved application, using our products in non-approved applications voids the warranty on the product.

Vicor has several other products that are qualified and approved for series output configuration to meet the high-voltage application requirements. These products use the Sine Amplitude Converter™ (SAC) topology, which provides isolation and fixed ratio DC-DC conversion and allows the outputs to be stacked in series. Following is the list of products that use SAC topology and are approved for series output configuration:

Unregulated Topologies

1. BCM (Bus converter module)

2. VTM Current Multiplier

Regulated Topologies

3. PRM in series with VTM

4. Yeaman Topology

5. Maxi, Mini, Micro DC-DC Converters

All the above specified products have gone through a thorough validation for series operation and therefore are the best option for those types of applications which require high voltage as input. For more information on designing higher-voltage outputs using series connected SAC's, please refer the application note AN:034 "Creating Higher Voltage Outputs Using Series Connected Sine Amplitude Converters". For notes on Yeaman Topology, please refer to the whitepaper on 350V to $12V_{DC}$ "Yeaman Topology" Power System. For designing a higher-voltage outputs using Maxi, Mini, Micro DC-DC converters, please refer to application note AN:204 "Creating High-Voltage Outputs" or contact Technical Support: apps@vicorpower.com.

Thermal Management

This section provides design guidelines for achieving effective thermal management of the ChiP DCM. Proper thermal management provides improved module and system MTBFs, and lower product life-cycle costs. The peak efficiency of the ChiP DCMs is 93.9%. Higher operating efficiency minimizes power dissipation i.e., lower heat loss. To evenly distribute the internally-generated heat across the surfaces, the ChiP DCM's top and bottom sides are molded with an optimized thermal compound material that has low thermal impedance. This enhances thermal pathways to the smooth, flat ChiP exterior. The majority of the heat can be removed using single or dual-sided cooling by using heat sinks or coldplates with some heat transfer through the leads of the package. Module cooling can be achieved by conduction or convection cooling techniques. In addition, Vicor offers heat sinks with thermal interface materials that are specifically designed for ChiP DCMs.

Efficiency and Power Dissipation

The ratio of output power to input power is defined as the module's efficiency, which is given in Equation 7.1. Efficiency is a basic figure of merit that can be used to relate power dissipation directly to module output power. The power dissipation is given in Equation 7.2.

$$\eta = \frac{P_{OUT}}{P_{IN}} \qquad (7.1)$$

$$P_{DISS} = P_{OUT} \bullet \left(\frac{1}{\eta} - 1 \right) \qquad (7.2)$$

Where P_{DISS} is the converter internal power dissipation, P_{OUT} is the output power, P_{IN} is input power and η is efficiency. The first step in evaluating cooling requirements is to calculate the worst-case power dissipation based on the module efficiency and highest anticipated load power. Clearly, higher efficiency will translate into lower power dissipation and simplify the cooling problem.

Thermal Circuit Models

In many applications, heat will be conducted from the module's top side into an attached heat sink or heat conducting member and through the module pins to the PCB, shown in Figure 7.1. Cooling of the module through the board is a function of how much copper is surrounding the module, how much air is passing over that copper and how much heat is coupled into the PCB from surrounding components. To design an effective thermal management system, a thermal model of the converter is needed.

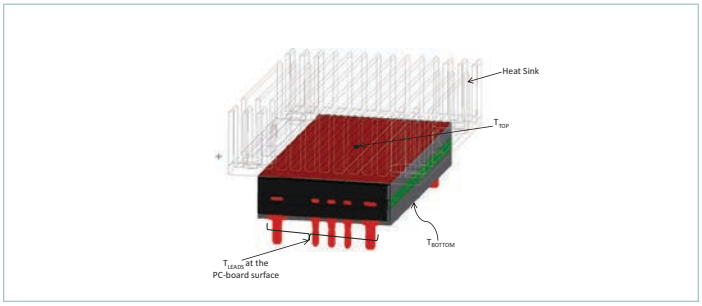


Figure 7.1 — *Heat-conductive path*

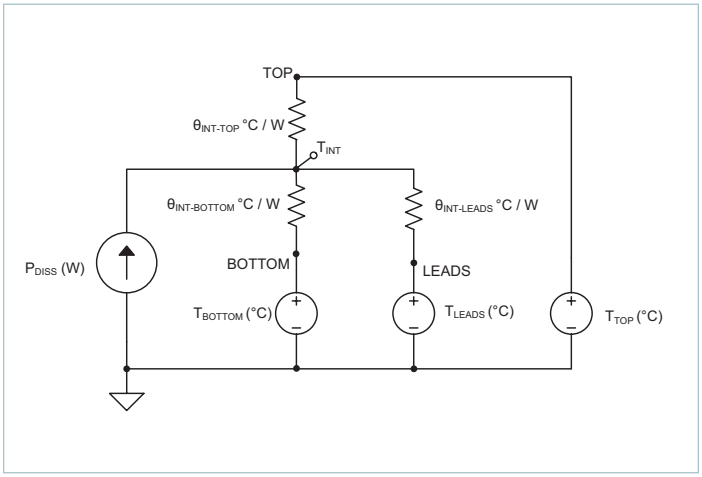


Figure 7.2 — *Thermal equivalent electrical circuit model of through-hole ChiP DCM*

Thermal circuit models have been created for ChiP DCM products to allow designers to estimate the maximum internal temperature of the product when operating under known electrical conditions in a user defined thermal environment. Figure 7.2 shows the thermal equivalent electrical circuit model of the through hole style of ChiP DCM. Note that the maximum internal temperature in the product is represented by a single temperature node T_{INT}. These models are analogous to electrical circuits and contain resistors, current sources and voltage sources.

Electrical resistors are replaced in this analogous circuit model with thermal resistances in units of degrees Celsius per watt [°C/W]. In Figure 7.2, $\theta_{INT-TOP}$, $\theta_{INT-BOTTOM}$ and $\theta_{INT-LEADS}$ are the thermal resistances of the top side, bottom side and leads of the through hole ChiP DCM. A current source (P_{DISS}) is utilized as analogous to a power dissipation source in units of watt [W]. The voltage source is utilized as an analogous temperature source in this circuit model with units of degrees celsius [°C]. Extensive lab testing of the product is done in parallel to ensure these simple circuit models are adequate for their intended purpose of estimating thermal performance. The underlying calculations are the same as utilized in the Vicor suite of online tools, refer to the PowerBench. For more details on using the online tools, please refer the application note AN: 039 "Thermal Management for VIA and ChiP Modules." The thermal data is also the same, but the online tools provide more extensive temperature dependent electrical performance modeling.

Maximum Internal Temperature

There is a single node in the circuit model that represents the maximum internal temperature of the module. This maximum internal temperature node is a virtual representation of the maximum-internal temperature within the module during any and all electrical and thermal conditions – as such it may change location as electrical and thermal operating conditions change. The maximum internal temperature derived from these circuit models should be less than the maximum temperature in the operating temperature range of the module under consideration. It also assumes the T_{TOP}, T_{BOTTOM} and T_{LEADS} as isothermal.

For example, the thermal resistance values from the DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) product data sheet are shown in Figure 7.3.

Thermal						
Operating internal temperature	T_{INT}	T-Grade	-40		125	°C
		M-Grade	-55		125	°C
Thermal resistance top side	$\theta_{INT-TOP}$	Estimated thermal resistance to maximum temperature internal component from isothermal top		2.08		°C/W
Thermal resistance leads	$\theta_{INT-LEADS}$	Estimated thermal resistance to maximum temperature internal component from isothermal leads		6.54		°C/W
Thermal resistance bottom side	$\theta_{INT-BOTTOM}$	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		2.36		°C/W
Thermal capacity				21.5		Ws/°C

Figure 7.3 — *Thermal resistance values of DCM4623TD2K31E0T00*

Use of Circuit Models

Physics dictates that the temperature rise in the circuit model is driven by the power dissipation of the product. The power dissipation can be calculated using output power and the efficiency of the module as noted in the data sheet. Data sheets also typically show temperature dependent efficiency and power dissipation in graphical format. Since a primary goal in thermal management is to determine the maximum value for internal temperature, the data sheet values for efficiency / power dissipation used in the calculation need to be those at an elevated temperature. The graph shown in Figure 7.4 shows efficiency and power dissipation curves of the DCM4623TD2K31E0T00 (160 – 420V_{IN}, 28V_{OUT}, 500W) at a 90°C case temperature for a range of output current.

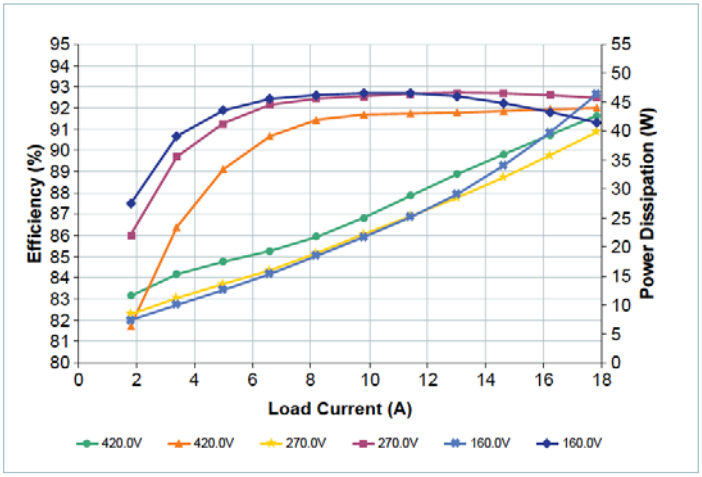


Figure 7.4 — *Efficiency and power dissipation vs. load at T_{CASE} = 90°C, nominal trim*

Once the power dissipation is added to the circuit model, what remains is for the system designer to add the thermal environment whether it is conduction cooled with a coldplate or convection cooled with a heat sinks.

The simplest case is when a coldplate is used to cool the product. For this case, a temperature-boundary condition can be added to the circuit model as an analogous voltage source since the voltage in an electrical circuit is analogous to temperature in a thermal circuit. The circuit model of a ChiP DCM with coldplate cooling through the top of the ChiP is shown in Figure 7.5. For a 10A load current at 160V input voltage, the module efficiency is 92.8% and power dissipation is 22.5W. The temperature of the coldplate needs to be maintained to 78°C or less to keep the internal temperature of the ChiP to within the 125°C maximum of the operating temperature range for the module as defined by the data sheet. The thermal resistance of any thermal interface material between the ChiP top face and the coldplate are assumed here to be negligible, otherwise the thermal interface resistance could be added in series between the top side thermal resistance and the T_{TOP} temperature boundary.

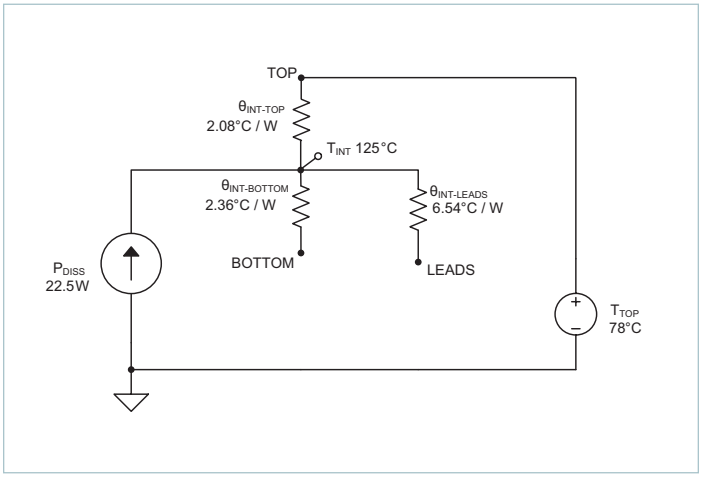


Figure 7.5 — *ChiP DCM with top coldplate cooling*

Thermal resistance from the internal ChiP to the device leads is also included in the data sheet. This can be incorporated in the thermal solution if the PCB temperature is known from historical or experimental data. Copper traces within the PCB may contribute to the cooling of the ChiP if the PCB traces are significantly large. For the example, the expected PCB temperature is 100°C and the effect of the PCB in the overall thermal solution can be quantified by this circuit model shown in Figure 7.6.

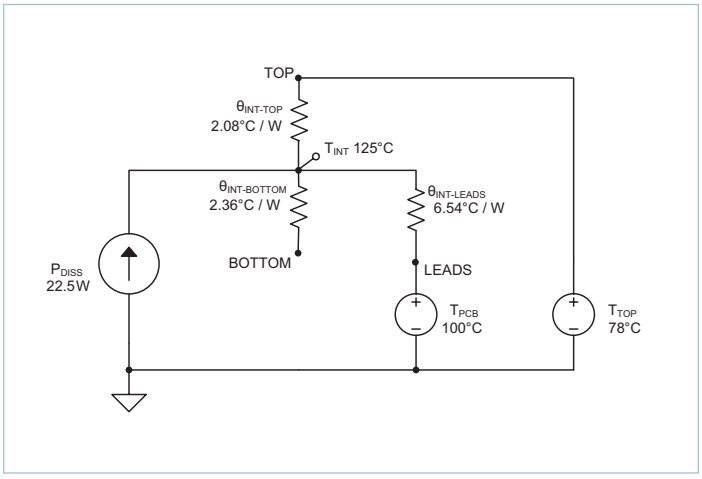


Figure 7.6 — *ChiP DCM with top coldplate and PCB cooling added*

The allowable maximum temperature of the coldplate (T_{TOP}) can be 78°C to keep the maximum internal temperature of the product to less than 125°C. The model can also be used to determine how much heat is conducted into each thermal boundary. In the example shown in Figure 7.6 above, about 3.82W of the total 22.5W dissipated by the ChiP is conducted into the PCB. Knowing this allows the designer to prepare for adequate cooling of the PCB.

Adding a second coldplate to the ChiP DCM to cool both the top and bottom would allow the two coldplates to operate at significantly higher temperature than a single coldplate cooling solution for the ChiP while still keeping the maximum internal temperature of the ChiP within the operating temperature range. This allows for a minimum cold plate temperature or 90°C rather than 78°C in the previous example. The circuit model of this system is shown in Figure 7.7. In this case, the lead resistance is not connected. This implies thermal equilibrium at the end of the resistance – meaning there is no heat flow from the internal-temperature node to the PCB through the leads resistance path.

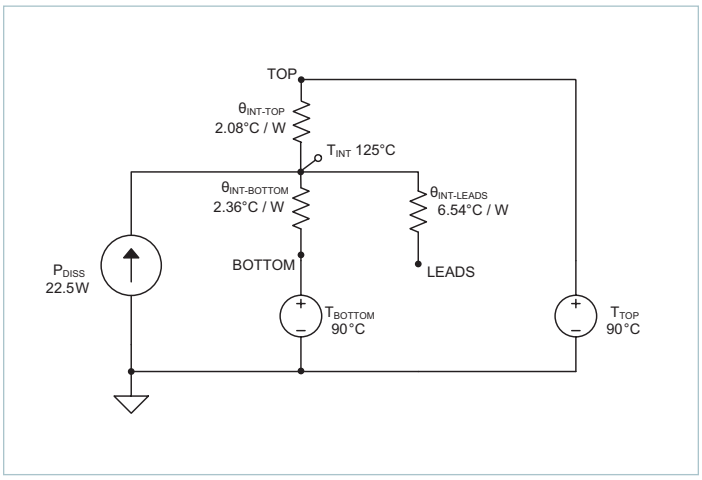


Figure 7.7 — *ChiP DCM with top and bottom coldplate*

For Vicor supplied heat sinks (Heat sinks for ChiP Modules), there is data available that will allow the designer to add the heat sink thermal behavior to the circuit model. This heat sink performance is characterized as a graph and corresponding polynomial fit with thermal resistance as a function of air flow. Figure 7.8 shows a thermal resistance graph with a 11mm longitudinal fins heat sink (P/N 40144).

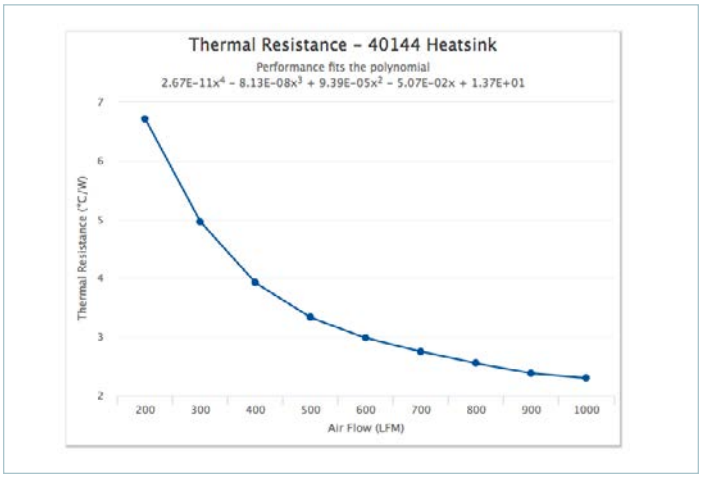


Figure 7.8 — *Thermal resistance graph and polynomial fit for 11mm longitudinal fins heat sink P/N 40144*

If this heat sink is used with a thermal boundry condition of 50°C ambient air temperature, the resultant circuit model would look like Figure 7.9 shown below. It can be seen from the circuit model that the power dissipation need to be limited to less than 12.5W under these conditions to keep the internal temperature of the ChiP within the maximum 125°C of the operating temperature range.

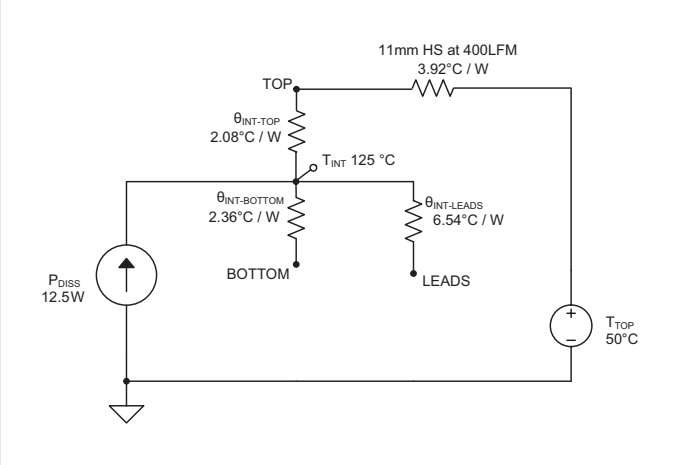


Figure 7.9 — *ChiP DCM circuit model with 11mm heat sink*

Thermal Specified Operating Area

Vicor data sheets also contain graph(s) that show acceptable thermal operating area. An example of this graph is shown in Figure 7.10 below.

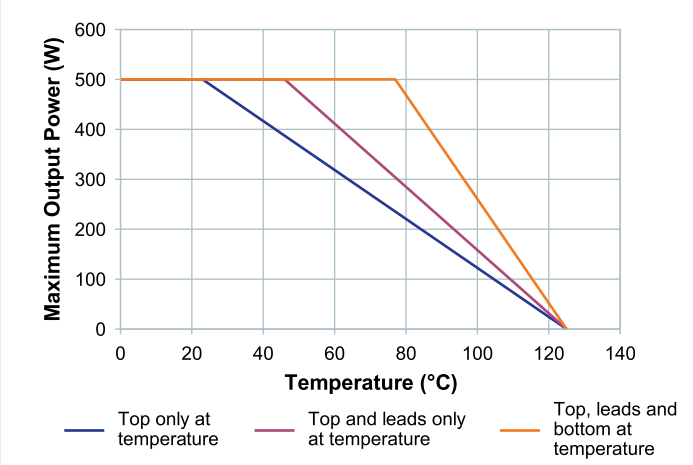


Figure 7.10 — *Thermal specified operating area: max output power vs. case temp, single unit at minimum full-load efficiency*

Adherence to conditions in the graph is intended to keep the maximum internal temperature of the product within the operating temperature range. The assumption in the graph is that the temperature on the x-axis is uniform on the face of the module. This is essentially the condition that would result in a ChiP module being attached to a heat sink or coldplate with a thin layer of thermal grease as an interface. Thermal testing to confirm performance within Vicor specifications should be directed toward making temperature measurements at these locations rather than on the module itself. Heat sinks and coldplates are typically made with aluminum or copper. Both materials have a thermal conductivity, several orders of magnitude greater than those materials present on the face of ChiP module. The high thermal conductivity means the temperature gradient in these materials is minimal. So the temperature measurements made at the base of a heat sink or on a coldplate are relatively immune to specific location requirements and are both accurate and repeatable. A single location temperature measurement, center preffered as shown in Figure 7.11, is usually sufficient to represent the temperature of the heat sink base or coldplate.

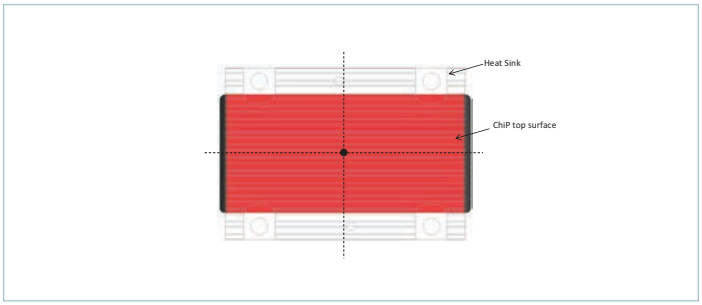


Figure 7.11 — *ChiP temperature measurement location*

Mechanical Compressive Force of Heat Sinks

It has been demonstrated that excessive mechanical compressive force in the z-axis of the Vicor ChiPs has the potential to cause a shift in electrical parameters (such as efficiency and no-load power dissipation) as well as mechanical deformation of the leads. Compressive load testing has indicated that keeping compressive z-axis force on through holes ChiPs below 20psi will prevent electrical parameter shift or mechanical deformation outside of product specifications.

Vicor provides a complete set of heat sinks for its products. These heat sinks are specifically designed to properly cool the part under most operating conditions, without applying excessive mechanical stress to the part. However, there are some applications that require a custom designed thermal solution, such as a cold plate. In these applications, the designer must consider the pressure that the thermal solution applies to the package: some thermal solutions may apply excessive or uneven pressure to the package, or they may apply pressure to the leads. These scenarios must be avoided, since there is a limit to the pressure in the z-axis that ChiP packages can support.

- Excessive pressure on the package might cause changes the electrical properties of the device; this effect can be minimized by applying even pressure across the entire surface of the package.
- The leads are not designed to support any pressure in the z-axis, so the device must be completely supported by the package, with no z-axis pressure on the leads.

If the thermal solution is carefully designed, so that it applies even pressure to the package, with no pressure on the leads, there is still a limit to the pressure that can be applied without affecting the electrical specifications.

Figure 7.12 shows what happens when Z-axis pressure is applied to the entire surface of a Vicor through-hole Chip while measuring their input current and efficiency. The graph shows the percentage of devices that successfully passed the test. (The condition for success was defined as less than 5% change in input current at no load, or less than 0.1% change in efficiency at full load.) According to these results, less than 39psi of pressure resulted in 100% of the devices remaining within specifications. To account for variations due to temperature, aging, part-to-part variability, and relatively small sample size used in the test, Vicor recommends that Z-axis pressure be kept to less than 20psi.

ChiP Compressive Load Parametric Unit

The graph in Figure 7.12 shows the pressure at which the input current and efficiency begin to be affected to a significant level (i.e., the variation in performance is above the parametric limits set for the test). Actual mechanical failure requires much more pressure. Some applications may require a thermal solution that applies more pressure to the package than the maximum allowed here. If this is the case, the user must do a complete evaluation to determine whether the device performance still meets the system requirements. In this situation, it is highly recommended that the user contact a Vicor Applications engineer for more information.

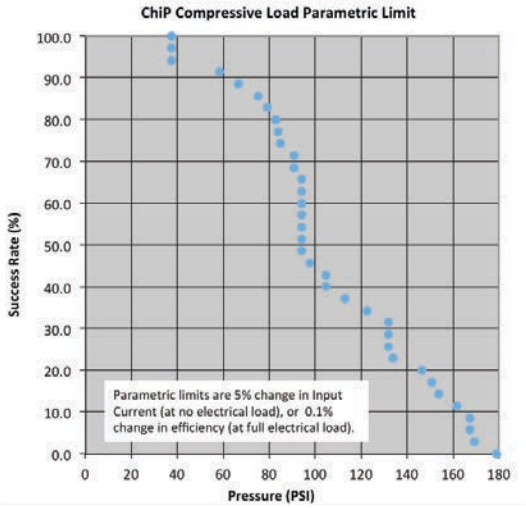


Figure 7.12 — *Test success rate vs. ChiP compressive load; test success is defined as units' performance shift remaining within the parametric limits listed in the graph*

Vicor Heat Sink

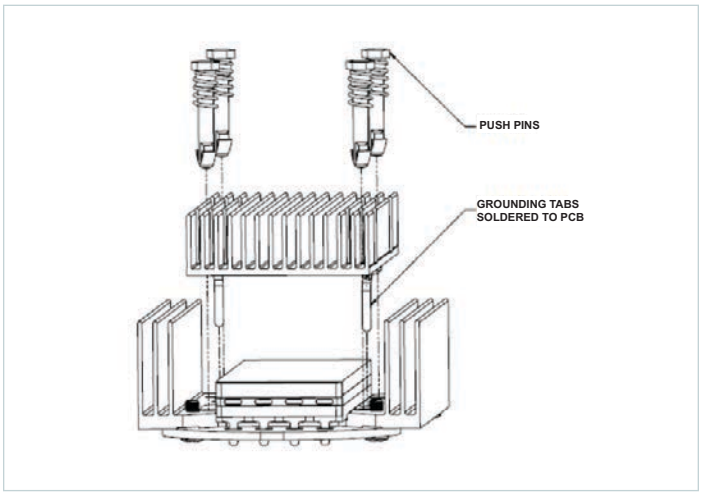


Figure 7.13 — *Diagram of Vicor heat sink, showing top plate, bottom plate and push-pins*

There are a variety of thermal pads, gels, and gap fillers that can be used to interface Vicor ChiPs to custom heat sinks or cold plates. Vicor recommends working closely with thermal interface material vendors to insure use of appropriate thermal materials that minimize compressive forces while providing adequate fill, coverage and thermal performance.

PC-Board Layout Considerations and Component Placement for Improved EMI

The design of a switching power converter PCB with good EMI performance characteristics requires special considerations. This section provides basic design guidelines on the layout of a printed circuit board (PCB) for minimizing parasitic elements due to the PCB routing that adversely affect the performance (such as conducted and radiated emissions) of the power components and electromagnetic intereference (EMI) filters. The following critical items must be considered in the layout:

1. Component Placement
2. Power Planes
3. Signal Traces and Routing
4. Ground Planes
5. Thermal Management Techniques for Printed Circuit Boards

As an example, the above considerations are illustrated using a DCM evaluation board PCB layout for the schematic shown in Figure 8.1. Please note that the layout guidelines provided here are standard practices and are based on experience with various customer applications. However, these guidelines do not guarantee that a design will meet any emissions-related standards.

1. Component Placement

   a. Physically locate EMI filters at the source of interference, i.e., close to the power converters. Filtering components, such as the Y-capacitors (C15, C16, C18, C19), input X-capacitors shown in Figure 8.2, must be placed close to the input terminals of the DCM to minimize the effect of trace inductance.

   - Keep high dI/dt current loop areas small by placing the X and Y-capacitors close to the DCM: differential-mode AC currents will flow through the input capacitors (C01, C02, C03) and internal FETs of the DCM, forming a current loop. Similarly, the common mode AC currents will flow through the Y-capacitors (C15, C16, C18, C19) and other circuit parasitic capacitances. The high dI/dt currents will generate eddy currents, resulting in magnetic fields; the stray magnetic fields increase the noise interefence with the nearby electronic circuitry and can potentially result in radiated emission issues. Therefore, minimize current-loop areas by placing the input X-capacitors and Y-capacitors closer to the input leads of the DCM. As a result, the ability of a conductor to couple energy by induction and radiation will significantly reduce.

   b. Use a wide copper plane of the negative input conductor in the layer below the high dI/dt current loops; this will generate eddy currents in the opposite direction to the loop-area eddy currents above and provide better shielding from magnetic fields. As a result, the EMI is effectively reduced. To improve the effectiveness of the shielding, minimize the height between the layers to that necessary for safety spacing requirements.

   c. Keep the required external output capacitor (please refer to the product-specific data sheet for C_{OUT_EXT}) close to the output terminals of the DCM to minimize the effect of trace inductance.

   d. Place signal-pin circuitry out of the DCM package outline to avoid DCM switching noise interference with the signal-pin circuitry.

2. Power Planes

   a. Route the input power connections using a wide copper plane as shown in Figures 8.2, 8.3. Using wide copper planes will decrease the trace inductance as well as increase the current-carrying capability over a fixed distance.

   b. Similarly, route the output power connections using wide copper planes, as shown in Figures 8.3 and 8.4. Place the +OUT and –OUT copper planes alternatively on the PCB layers. Interleaving the +OUT and –OUT planes increases the current-carrying capability and decreases the inductance of the connection while offering some "free" differential capacitance by way of the natural board parasitics.

   c. Keep the power traces as short as possible to reduce radiated EMI.

   d. Interconnect the power planes routed on multiple layers using vias to keep trace impedance low.

   e. High-current traces should be run as close as possible to their respective return traces. The power and ground planes virtually become a single plane at high frequencies, and should, therefore, be kept near each other. The closest way to route the power and ground traces is by placing them on adjacent layers. As a result, loop area/inductance is minimized. Both power and ground traces should be made as wide as possible.

   f. Do not fill planes directly beneath EMI filter (ex. MFM) housing and discrete common mode chokes, instead route the power and EMI planes outside the package outline as shown in Figure 8.6. This prevents parasitic coupling between the traces and the filter components which are above the power/ground planes. Filling the planes under the EMI filter/discrete common-mode chokes may raise the voltage in the power/ground planes due to the stray magnetic fields from the common-mode chokes and adversely affect the performance of the EMI filters.

3. Signal Traces and Routing

   a. Route the signal traces on the internal layers and use Kelvin connections to prevent power currents from interacting with the signal-level currents. Layer 3 was chosen for signal routing in the design example, shown in Figure 8.5. Shield the signal layer above and below with the –IN reference plane, as shown in Figures 8.3 and 8.4, which results in smaller loop areas and limits coupling of other signals.

   b. The use of ground or voltage planes as a shield can reduce the interaction of electromagnetic interference upon devices, circuits or portions of circuits.

   c. Fill the signal layer with a reference-ground copper pour and place multiple vias on the reference ground planes to interconnect the ground planes on the different layers.

4. Ground Planes

a. Route the EMI ground plane underneath the DCM on all layers and interconnect with multiple vias. As an example, the EMI ground plane is shown in Figure 8.7. Placing multiple vias on the EMI ground plane will significantly lower the trace impedance as well as facilitate heat dissipation from the DCM, i.e., the EMI ground plane acts as a heat sink. Use of a belly heat sink connected to the EMI ground plane will further improve DCM heat dissipation.

b. Make EMI ground conductors large enough to ensure that they do not behave as antennas that radiate or pick up noise.

5. Thermal Management Techniques for Printed Circuit Boards

a. Copper is a relatively good conductor of heat as well as being the main material used to conduct electricity. This capability permits the use of large planes of copper to perform the heat-sinking function necessary to keep the board and the board assembly cool.

- For example, mounting the DCM on the input and output pins with larger copper planes can help in dissipating some amount of DCM's internally-generated heat through the leads. The thermal resistance of the DCM leads are provided in each model's data sheet for use in thermal modeling.

b. Heat will also be generated depending on the amount of current being drawn through the circuit conductors. Therefore, proper conductor width and thickness must be assessed to ensure that the current being passed through the conductor does not raise the temperature of the PCB assembly above a safe temperature, which may increase the failure rate.

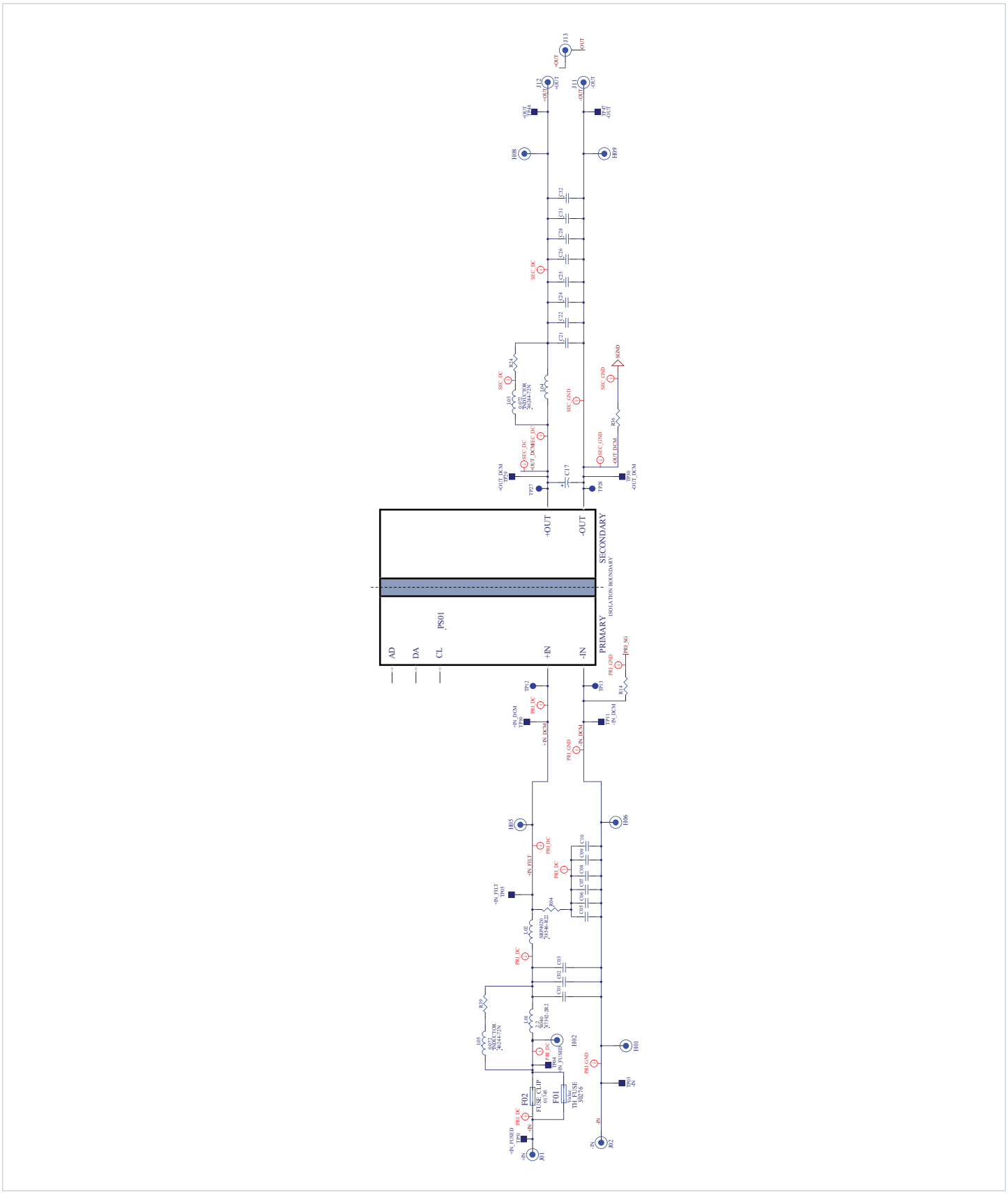


Figure 8.1 — *Schematic of example DCM evaluation board*

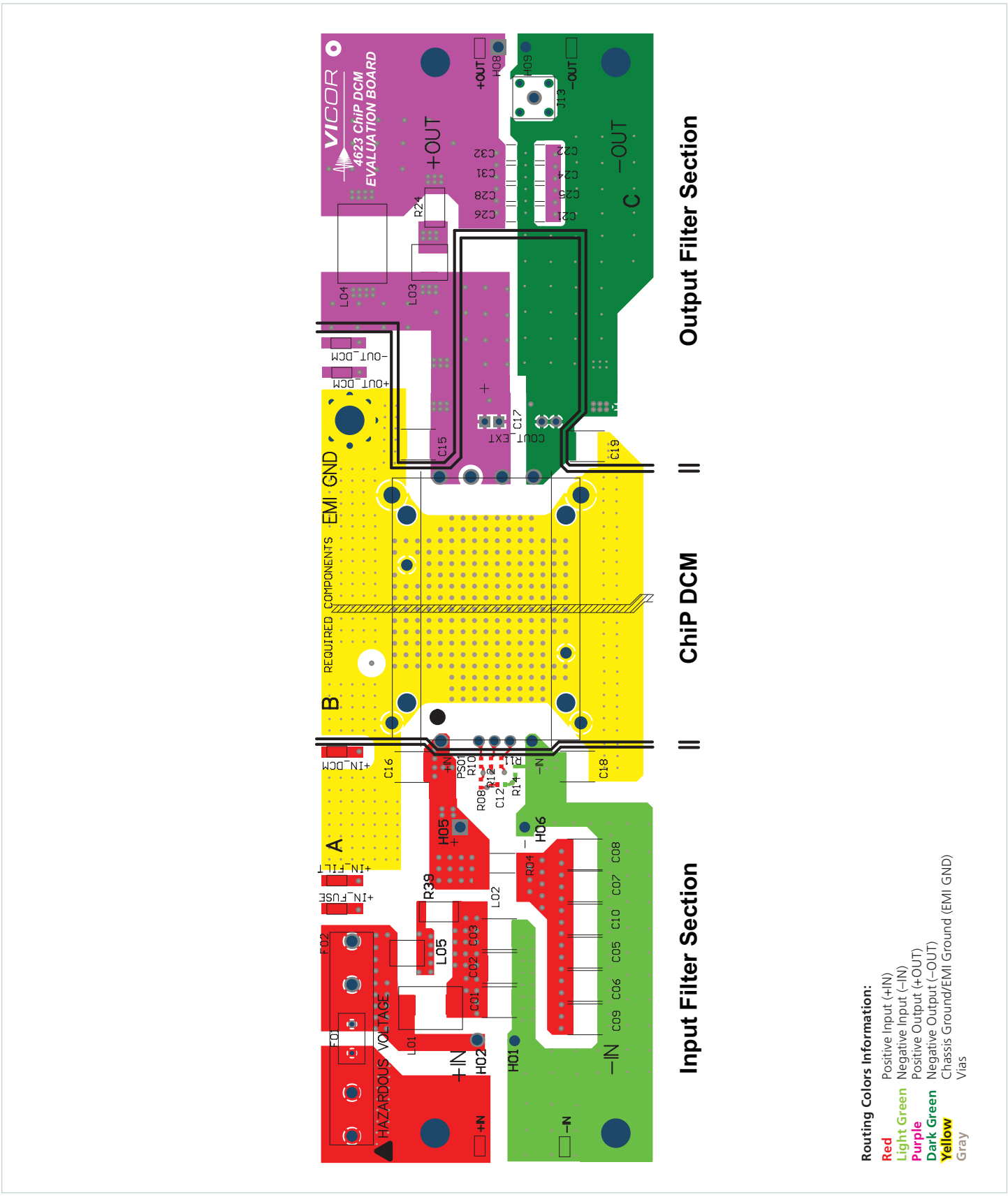


Figure 8.2 — *Filter component placement and input power trace routing on the top layer*

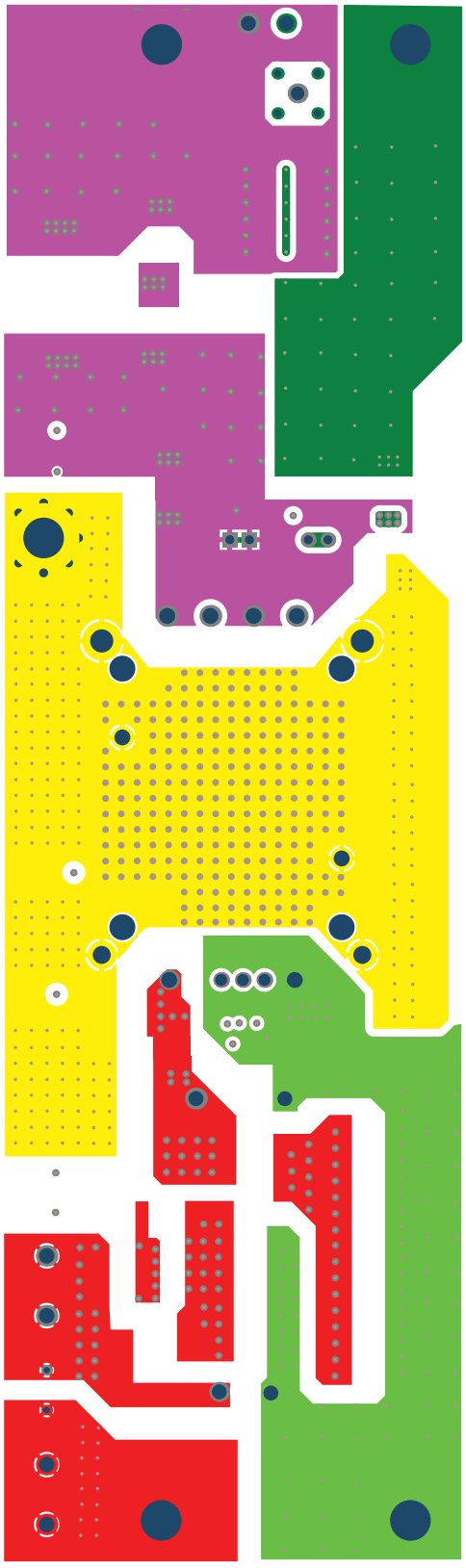


Figure 8.3 — *Input power traces routing and positive output power trace routing on layer 2*

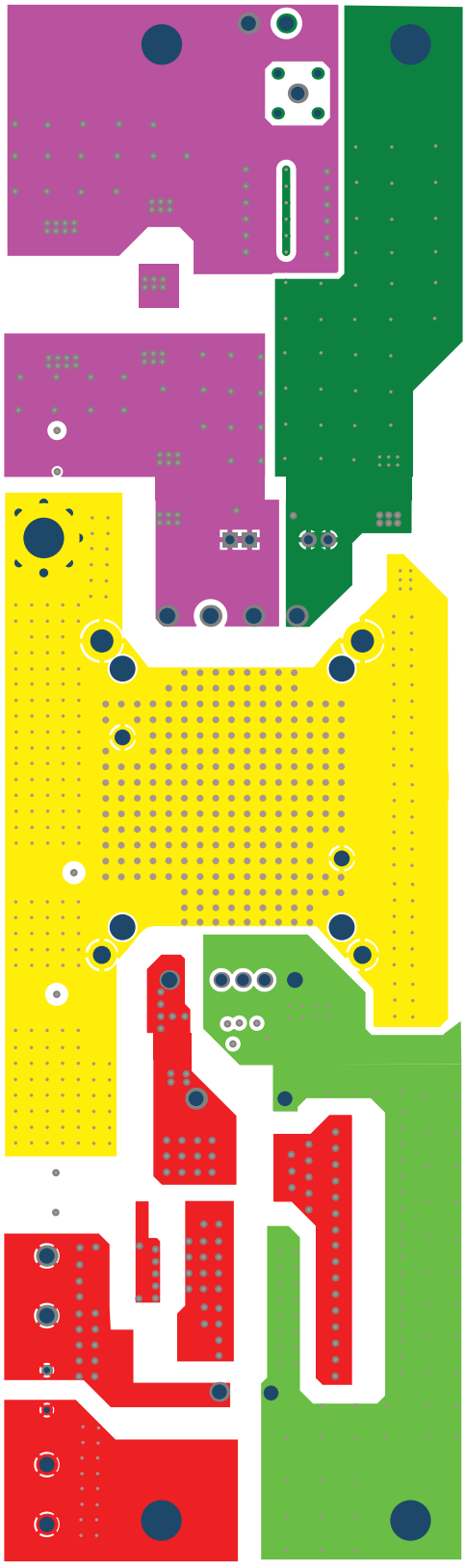


Figure 8.4 — *Negative output power trace routing on layer 4*

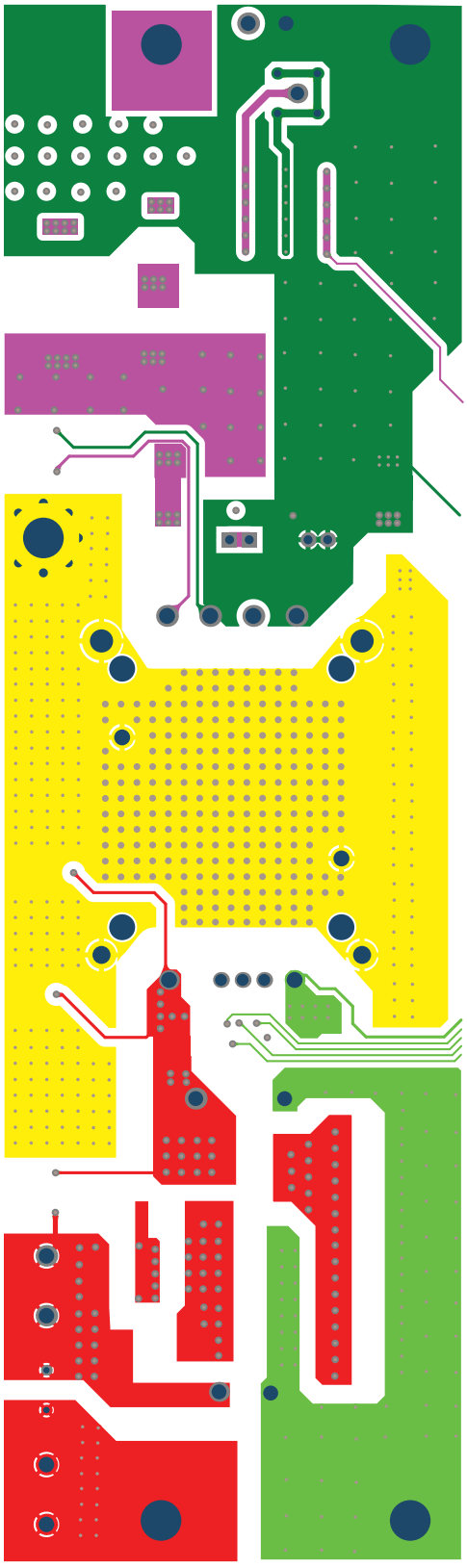
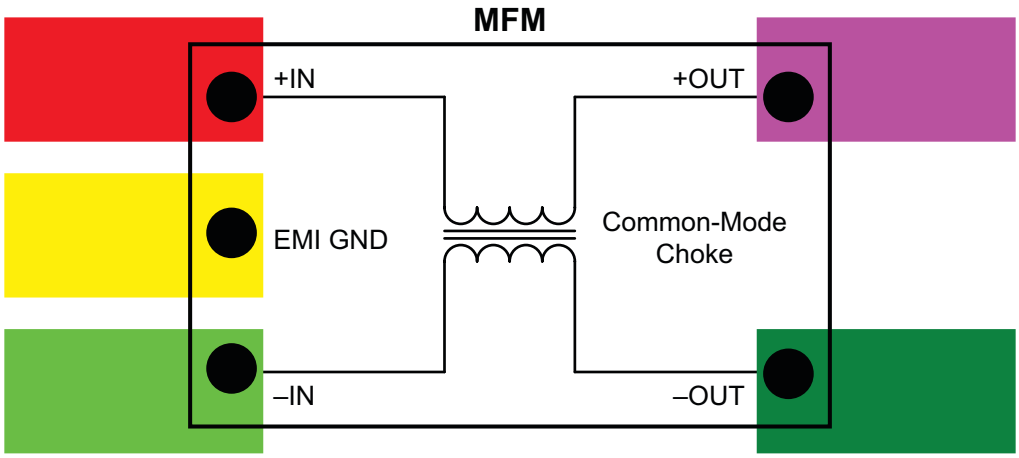


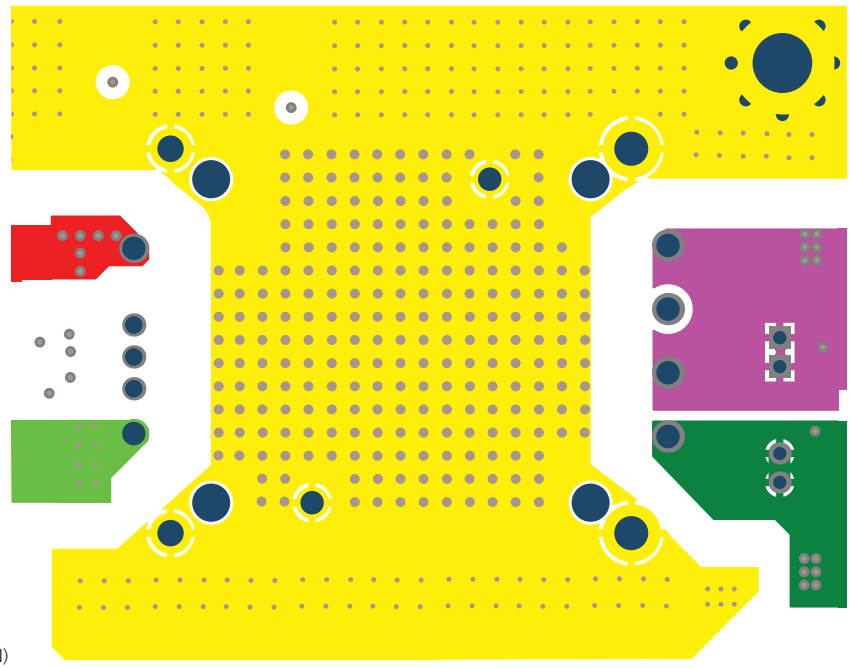
Figure 8.5 — *Signal trace routing on layer 3*



Routing Colors Information:

Red	Positive Input (+IN)
Light Green	Negative Input (–IN)
Purple	Positive Output (+OUT)
Dark Green	Negative Output (–OUT)
Yellow	Chassis Ground/EMI Ground (EMI GND)

Figure 8.6 — *Example power and ground trace routing of EMI filters*



Routing Colors Information:

Red	Positive Input (+IN)
Light Green	Negative Input (–IN)
Purple	Positive Output (+OUT)
Dark Green	Negative Output (–OUT)
Yellow	Chassis Ground/EMI Ground (EMI GND)
Gray	Vias

Figure 8.7 — *Ground trace routing*

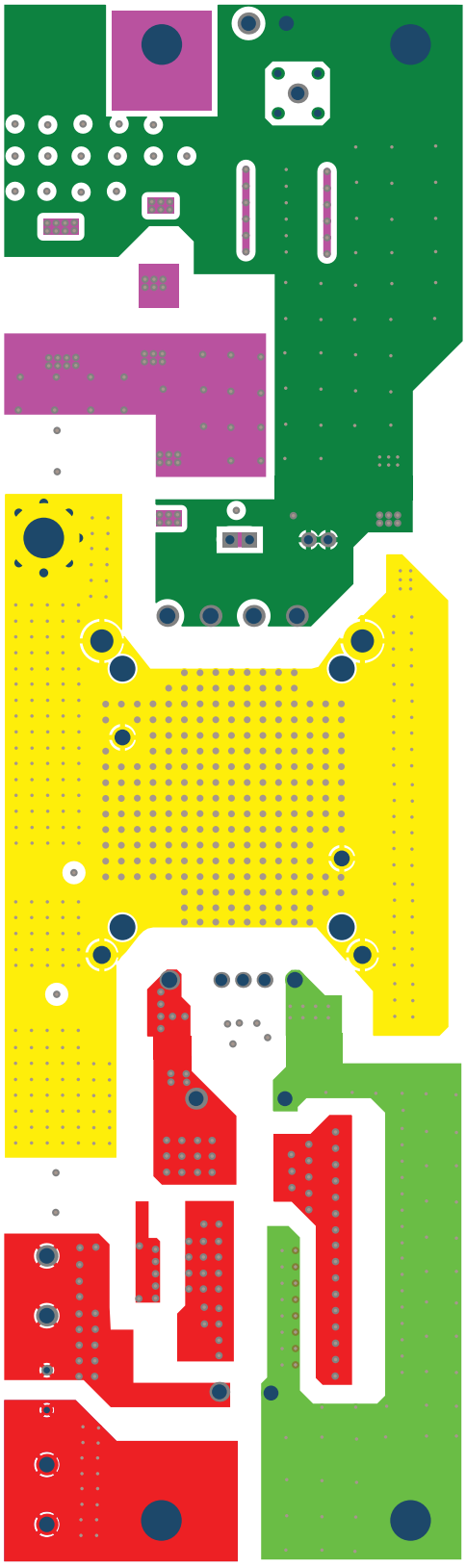


Figure 8.8 — *Input and output power trace routing on layer 5*

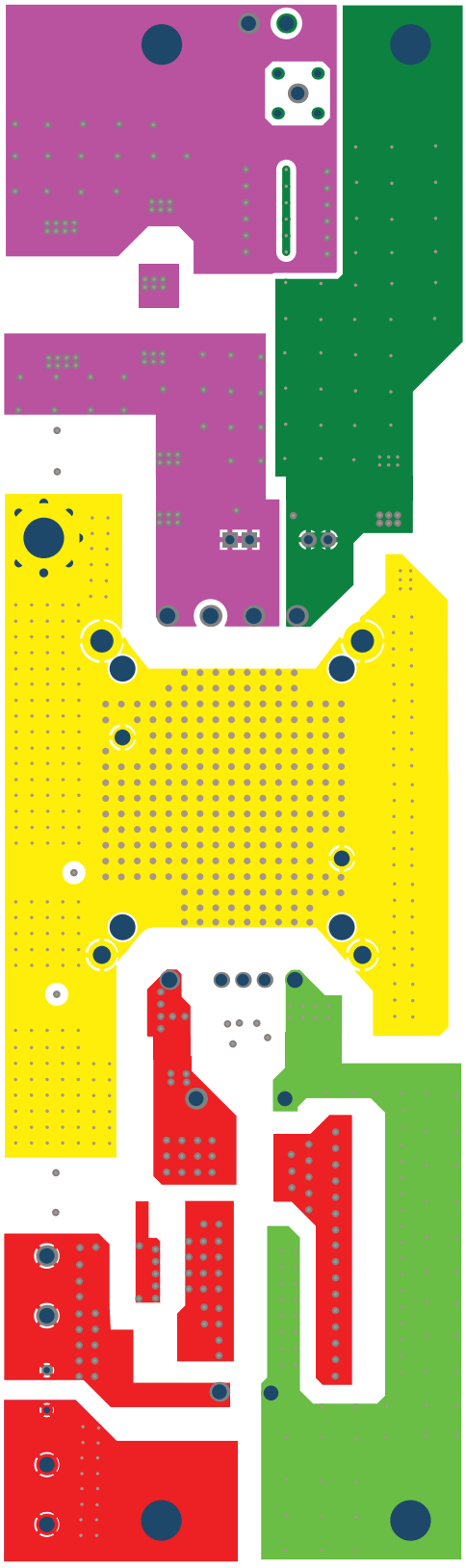


Figure 8.9 — *Input and output power trace routing on layer 6*

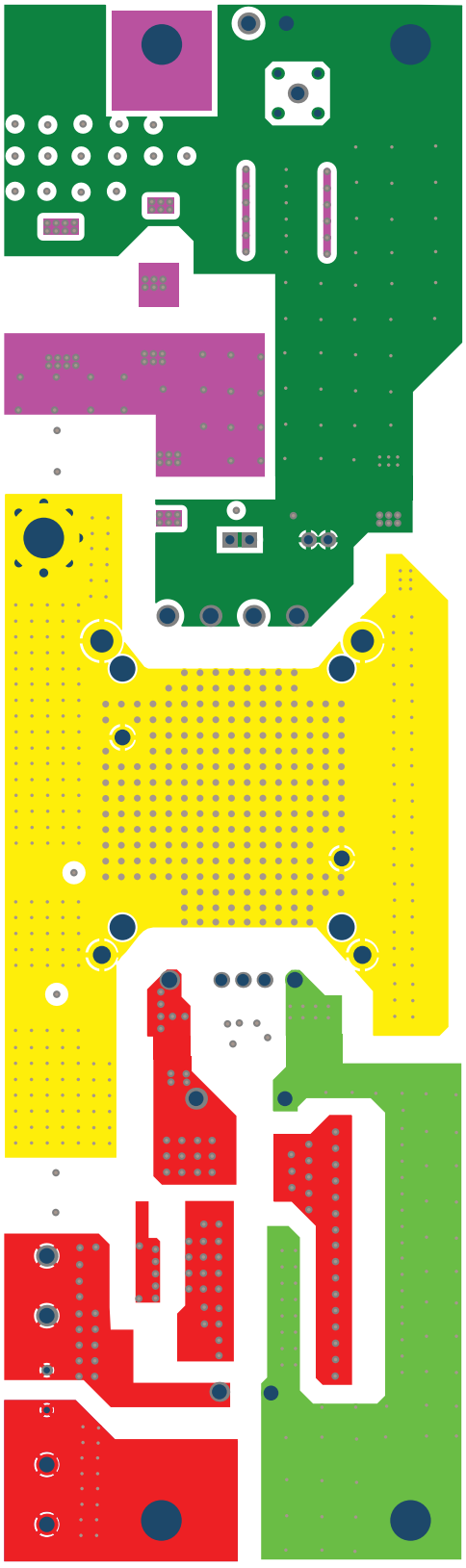


Figure 8.10 — *Input and output power trace routing on layer 7*

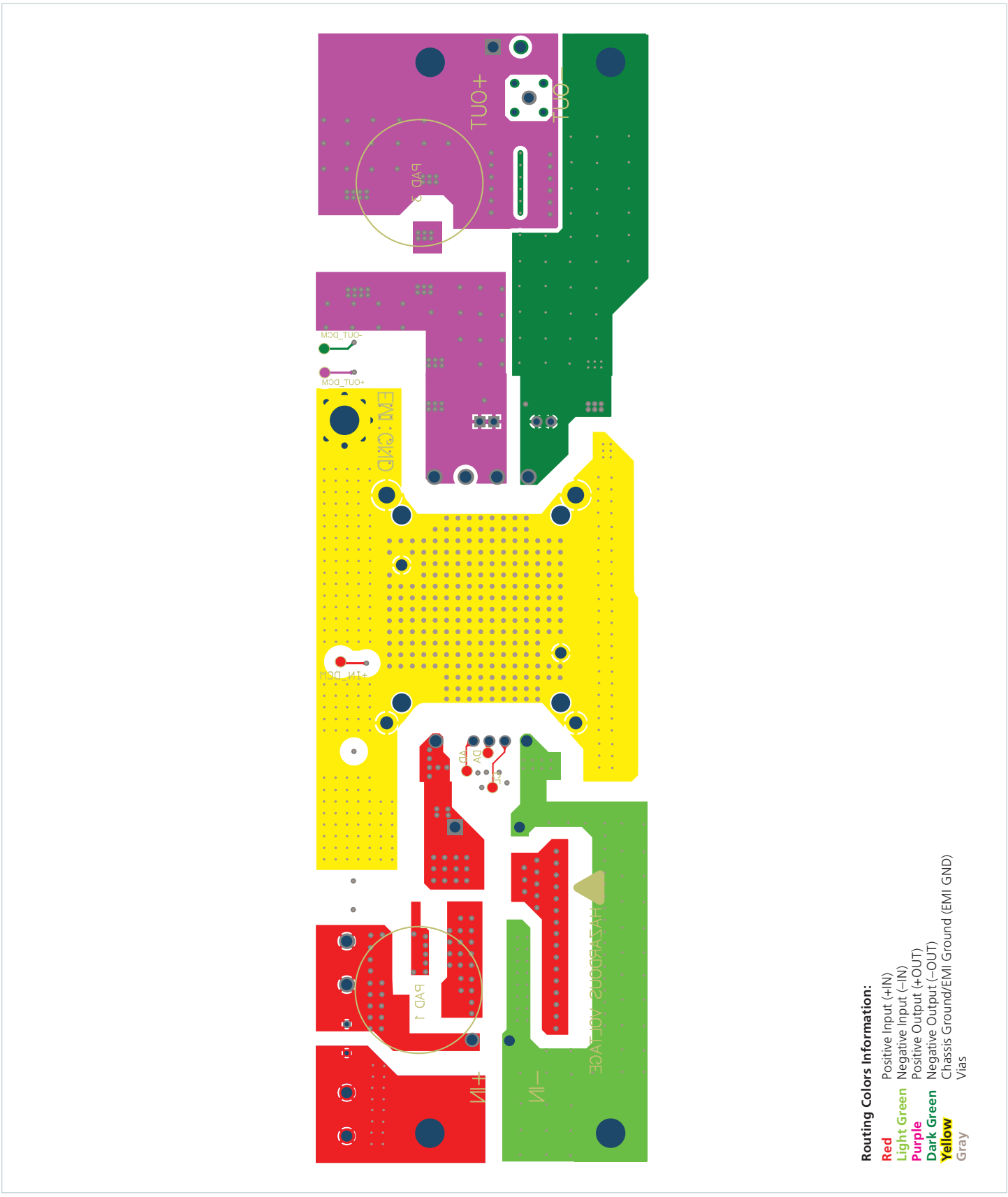
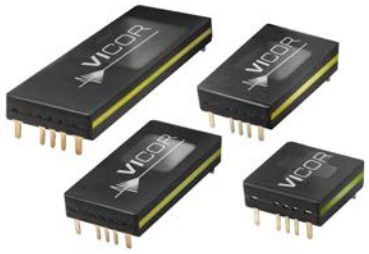


Figure 8.11 — *Input and output power trace routing on bottom layer*



Representative
Applicable Packages

This section is intended to provide guidance to users of the Vicor Converter housed in Package (ChiP) Technology to physically integrate ChiPs having through-hole leads into higher-level assemblies.

ChiPs having through-hole leads should be assembled onto printed circuit boards via wave or selective soldering. Manual soldering is not recommended.

Note: Solder and related soldering equipment may be hazardous. Industry-standard health and safety precautions must be observed in the design and operation of soldering processes.

Disclaimer

This section provides general guidelines, as well as preferred examples which have proven to yield defect-free, reliable results.

A carefully designed and controlled process is necessary to ensure defect-free, reliable results. Given the range of printed circuit boards and components in customers' higher-level assembly designs, as well as the variety of soldering equipment which may be used, significant developmental efforts are likely to be necessary in order to optimize the soldering process for each application/ process context. ChiP mechanical samples having through-hole leads are available to enable optimization of the soldering process.

Please contact Vicor Applications Engineering for further assistance or inquiries regarding the soldering of through-hole ChiPs not covered in this document.

Attribute	Symbol	Conditions / Notes	Min	Max	Unit
Storage Temperature	T_{ST}	T-Grade	–40	125	°C
		M-Grade	–65		
ESD rating	HBM	ESDA/JEDEC JDS-001-2012	CLASS 1C		
	CDM	ESD22-C101E	CLASS 2		

Handling

ChiPs should remain in original, sealed packaging until time of use. Once opened, exposure to humidity should be minimized.

Placement

Use the recommended hole pattern as illustrated on the data sheet to support proper seating of the ChiP leads within the PCB. The ChiP should be placed such that each lead rests in its appropriate hole without distortion.

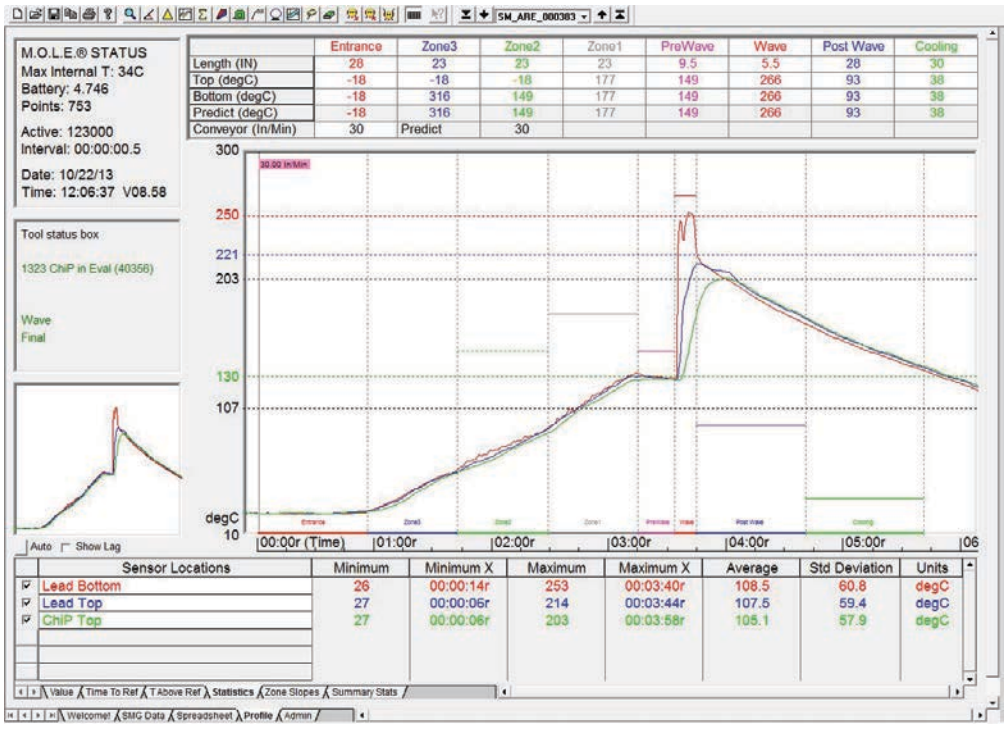


Figure 9.1 — *Preferred soldering process profile*

Soldering Process

The following description of a wave soldering process is based upon the use of preferred SAC305, high-temperature, lead-free solder with a preferred solder temperature of 265°C.

In general, a selective soldering process does not incorporate a conveyor, but uses other mechanisms to control the progression of the assembly through the process stages. The temperatures, times and rates described below should also be applicable to a selective soldering process. The maximum temperature at any point on the ChiP body must not exceed 205°C during the soldering process. The maximum temperature at the lead-to-ChiP interface must not exceed 215°C. In practice, this may be achieved in a typical wave soldering process by limiting the peak temperature at the top center of the ChiP body to 135°C during preheating.

Refer to IPC-A-610, "Acceptability of Electronic Assemblies" for relevant inspection methodology and criteria.

Fluxing

ChiPs are compatible with no-clean and water-washable fluxes. Alpha EF-2202 is preferred for use in wave soldering ChiPs having through-hole leads. Ultrasonic spray is the preferred method to apply flux to the bottom or solder side of the board. Precise control of flux quantity is necessary, as too much or too little flux will result in defective solder joints or other problems.

Preheating

The preheating stage prior to wave immersion must be carefully managed to ensure that flux activation is effective, and that PCB and lead temperatures are adequate immediately prior to wave immersion to support proper solder joint formation. The proper balance of pre-heating energy and preferred conveyor speed of 12.7mm/s should heat the top surface of the PCB at a preferred rate of 1°C/s to a preferred temperature of 130°C immediately prior to wave immersion.

Wave Immersion

The proper balance of conveyor angle, immersion depth and conveyor speed are critical to proper solder joint formation. The preferred wave immersion contact time is nine seconds.

Post-Wave Cleaning

If no-clean flux is used, no cleaning is required, although residues will remain on the assembly. The preferred ALPHA EF-2202 is a no-clean flux and the residues are designed to be left on the board. If desired, flux residues can be removed with Petroferm Bioact EC Ultra Semi-aqueous cleaner or with other commercially available solvent cleaners. ChiPs are generally compatible with commercially available solvents used to remove flux residues.

If water-soluble flux is used, the ChiP-on-board assembly should be washed using deionized water or water mixed with a commercially available saponifier. ChiPs are generally compatible with these mixtures.

Inspection

Refer to IPC-A-610, "Acceptability of Electronic Assemblies" for relevant inspection methodology and criteria.

Removal

Should it become necessary to remove a ChiP having through-hole leads from a PCB, it is preferred and generally most effective to mechanically sever the leads as close as possible to the top of the PCB. Alternatively, a selective soldering or re-work system may be used to de-solder the unit, but this may result in detachment of the lead structures from the body of the ChiP.

Once removed, the ChiP site may be reworked to restore the original condition of the PCB, and a new ChiP assembled as described above.

Revision History

Revision	Date	Description	Page Number(s)
1.0	09/06/18	Initial release	n/a
1.1	01/18/19	Corrections to output filter components	51
1.2	03/05/19	Updated to include 9 – 75V input, 80W DCM3623 models Added filter component values for TR pin Added filter component values for EN pin Updated FT pin minimum loading resistor value Updated figures 4.1, 5.1, 5.8, 5.9 Updated figure 2.34, added figure 2.36 for input current with an input filter	4, 7, 8 38 39 40 55, 67, 75, 76 33, 34
1.3	08/27/19	Updated to include DCM2322 product line extension Added referencing of input and output terminals section Wording corrections Corrected DCMxxxxxxxxxxxx00 timing diagrams Changed L1 component	4, 7, 38, 40, 41, 43, 48, 49, 50, 51 10 37, 58, 63, 80 44, 45 68
1.4	01/25/22	Fixed broken URL	13
1.5	03/03/25	Corrected parallel-damped filter network description	26

Note: pages added in Revs 1.2, 1.3.

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