Enabling Next Generation High Density Power Conversion

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Introduction

The drive to create Metadata[1] processing server systems plus the parallel push for increased port density and triple-play (voice / video / internet) traffic handling in telecommunication systems places greater demands on power management architectures.

The Problem: Inefficient Power Architectures

Traditional "AC to 12 Vdc Silver Box followed by 12 V to 1.x V synch buck" designs have run aground in terms of system power density and efficiency due to a combination of distribution bus losses and fundamental restrictions in topology performance as processor voltages reach sub-volt levels. Higher voltage (48 V or 350/380 V) bus voltages reduce distribution losses but usually mean the addition of an extra stage or stages to get down to the processor voltages which add size and may lower conversion efficiencies.

A new architecture is required to optimize processing real estate while minimizing the area used for power delivery in next generation systems.

The Solution: Factorized Power Architecture (FPA)[2]

FPA uses three flexible building blocks to redefine the boundaries of each conversion stage and enable higher densities and efficiencies.

The building blocks (known as "VI Chips") are:

Bus Converter Module (BCM®)
A narrow-range input, unregulated, high efficiency bus converter offering isolation and voltage transformation using a ZCS-ZVS Sine Amplitude Converter (SAC). High voltage (up to 384 V) and medium voltage (48 V) input versions are available.

Pre-Regulator Module (PRM®)
A unique ZVS high efficiency buck-boost converter.

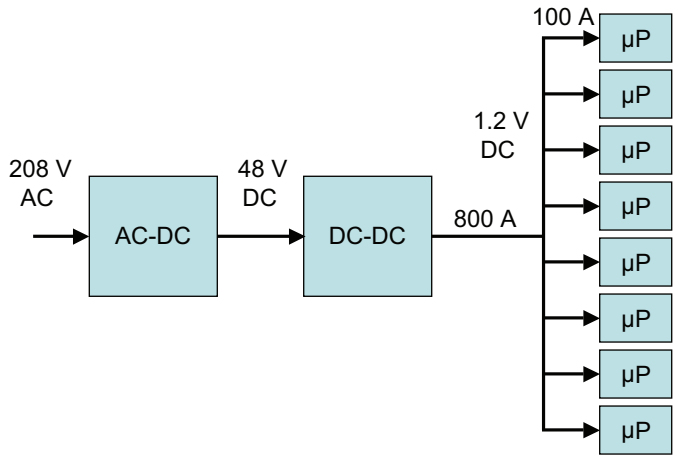
Voltage Transformation Module (VTM®)
Wide-range 48 V input, high efficiency voltage transformation unit using the ZCS-ZVS SAC and which works in combination with a PRM to give a low voltage output (down to 0.82 V as required).

FPA building blocks support greater flexibility, scalability and efficiency in power system design.

Example System

The paper presents an efficiency and space comparison for a mid-range / high-end data processing system comprised of one or more blocks of 8 microprocessors, each running at 1.2 V and 100 A for a combine load of 960 W per block. The system is fed via an AC to 48 Vdc front end from a 208 Vac input, as shown in Figure 1.

Figure 1
Basic System Block Diagram

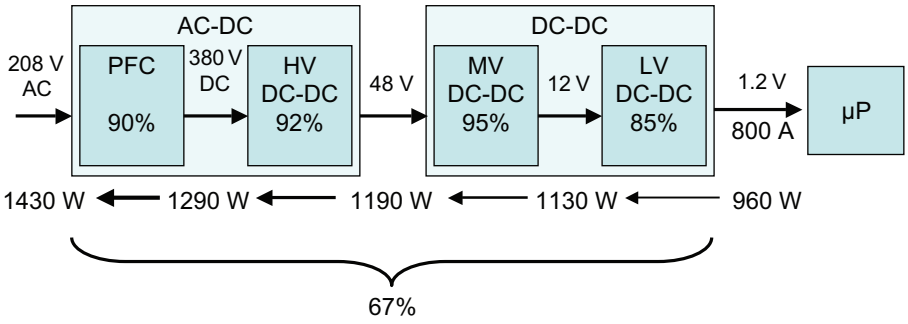


Baseline System Performance (Efficiency & Size)

Today's (2006) typical AC to 48 Vdc to 1.x V system has an overall 67% efficiency from AC to point-of-load (POL)[3] which means that for our 960 W load, the system draws ~1430 W from the AC line (Figure 2). The difference of 470 W is lost as heat – further increasing the demands on heat sinking / air conditioning systems and increasing to the running costs of the datacenter.

In this analysis, all components and sub-systems are considered to be in mass production now with widespread market acceptance and installed base. No 'exotic' components or materials are assumed.

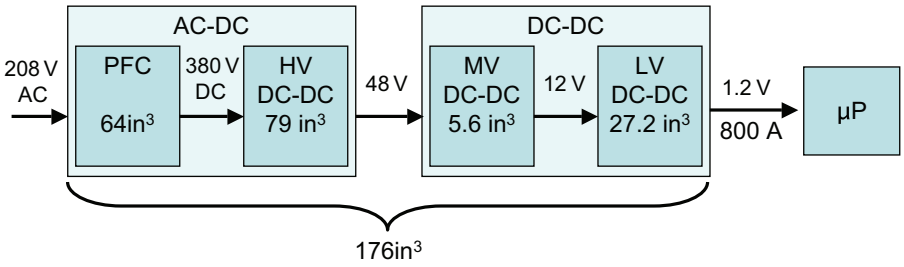
Figure 2
Baseline System Efficiency and Power Drawn from AC Line



Topological assumptions are that the AC to 48 Vdc unit comprises a standard bridge, filter and boost PFC generating 380 V and then using a two-transistor forward converter with diode rectification to 48 Vdc. The 48 –1.2 V conversion assumes four 48 V:12 V unregulated bus converters in 1/4-brick format followed by a 4- or 5-phase VRM to the processor.

In terms of size, for the front end AC to 48 Vdc, an assumption of 10 W/in^3 was made based on a survey of commercially available units[4]. In typical 800 W – 1500 W designs, the PFC stage (including AC-bridge and input EMI filter) occupy around 40% of the whole converter. Typical sizes for the PFC stage and HV (380 V – 48 V) DC-DC stage were then estimated based on the output power level of each stage. The MV DC-DC (1/4 bricks) and LV DC-DC (VRM including 'oscon' bulk capacitors) dimensions are from specific examples.

Figure 3
Baseline System Size



Improvement Phase 1: Utilizing BCMs for HV and MV DC-DC Conversion

The basic BCM® topology can be applied to both the HV DC-DC and MV DC-DC sections.

The B384F120T30 is a 300 W converter with a transformation ratio (K) of 1/32 which feeds directly from the PFC bus voltage and generates a 12 V output. A four-up array with paralleled inputs and serial outputs creates 1,200 W at 48 V with 94% efficiency. Figures 4a, b & c show the arrangement and performance details. Note that Figure 4a includes an optional 12 V output arrangement which could be used for drives or for lower power ancillary POL converters, though this is not included in the efficiency and size comparisons.

Figure 4a
HV BCM Simple Schematic

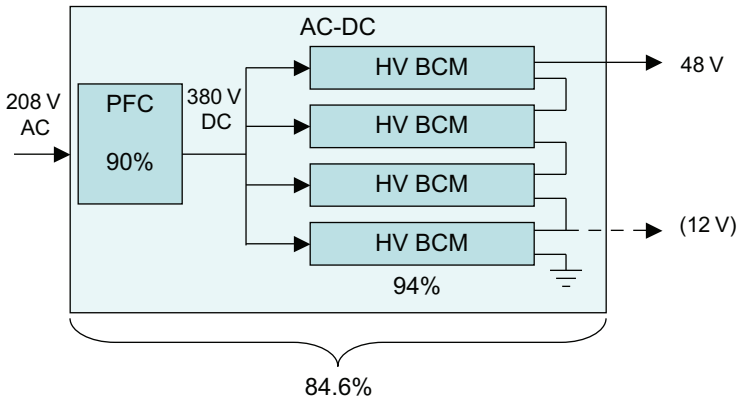
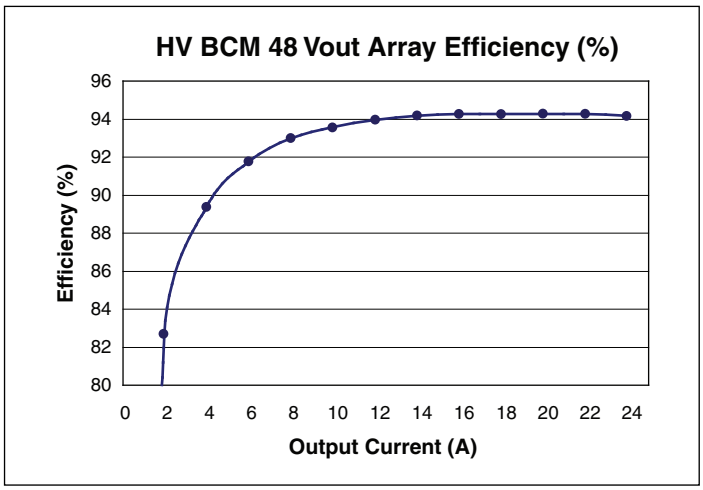
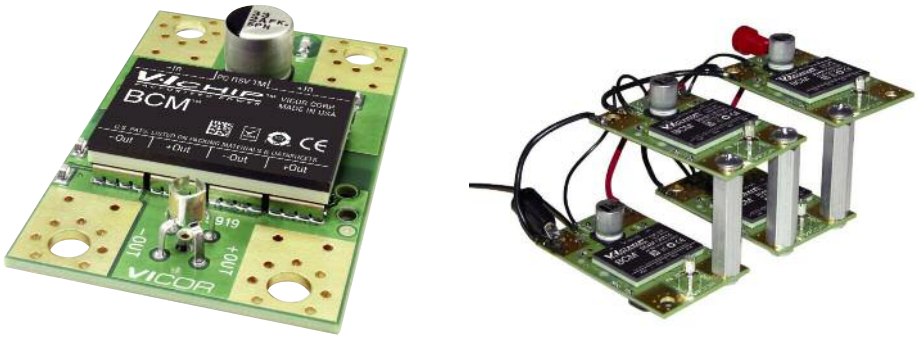


Figure 4b
HV BCM Performance Curves / Data



(4) x B384F120T30, each 12 Vout, Tcase 40°C, no heatsink

Figure 4c
HV BCM Demo Board (left) and Serial-output Array (right)



Further product developments are possible for improved system power granularity (e.g. with K of 1/8 for 384 V:48 V BCMs which could be connected with parallel outputs) and efficiency (with improved layout / interconnects).

For the MV DC-DC stage, the B048F120T30 is an unregulated, narrow-range 48 V input, 12 V output bus converter (K of 1/4) with 95% efficiency. Further BCM® performance data, including common mode noise performance is available(5).

In terms of size, the SAC in the BCM runs at an effective frequency of 3.5 MHz utilizing unique planar magnetics for high power conversion in a small package (see Figure 5), resulting in a power density of 1,034 W/in^3.

Figure 5
V•I Chip Dimensions. Note that all BCM, PRM & VTM units are identical in size

32.5 x 22.0 x 6.6 mm
1.28 x 0.87 x 0.26 in

Allowing for the necessary ancillary components in an HV DC-DC unit (pcb, connectors, output ORing, monitoring, etc.), the HV BCM enables a 60% size reduction as well as the 2% efficiency increase for this stage vs. traditional topologies. The MV DC-DC has similar efficiency as the baseline example but again has a 60% size reduction (including heat sinking). Phase 1 results (replacing HV and MV DC-DC stages with BCMs) are shown in Figures 6a and 6b.

Note that as the AC to 48 Vdc size assumed a nominal 10 W/in^3 power density, as the efficiency of the HV DC-DC improves, the PFC stage also reduces in power and subsequent size. Though a small integer reduction of an existing PFC stage size may not be practical, the lower power (current) requirement coupled with 48 W less power loss in the AC to 48 Vdc case would allow the power components (e.g. boost FET(s), diode(s)) to operate at lower temperatures and/or reduce heat sinking, improve efficiency and/or reliability etc.

Figure 6a
Phase 1 Efficiency

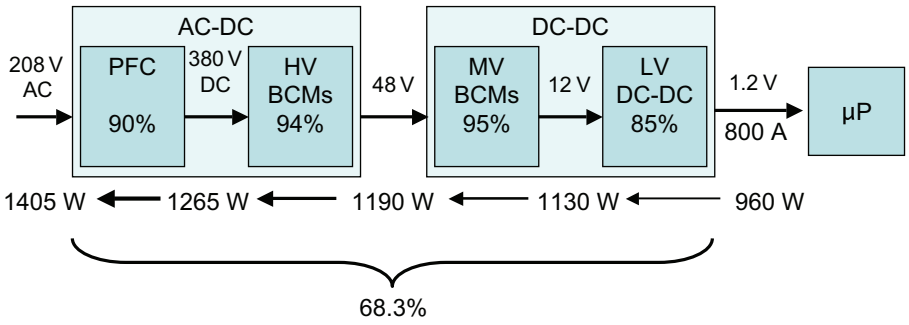
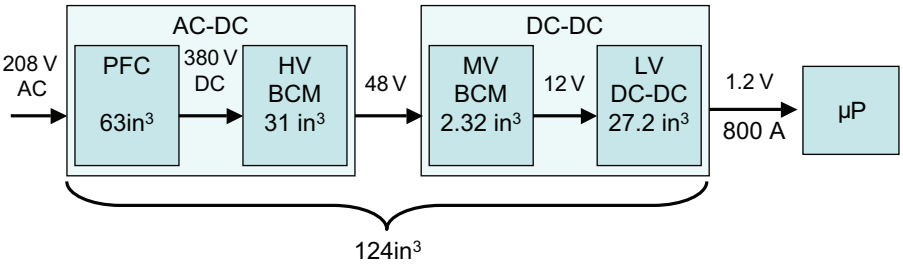


Figure 6b
Phase 1 Size



Improvement Phase 2:
From 48 V Direct to Processor Voltage with PRM®+VTM®

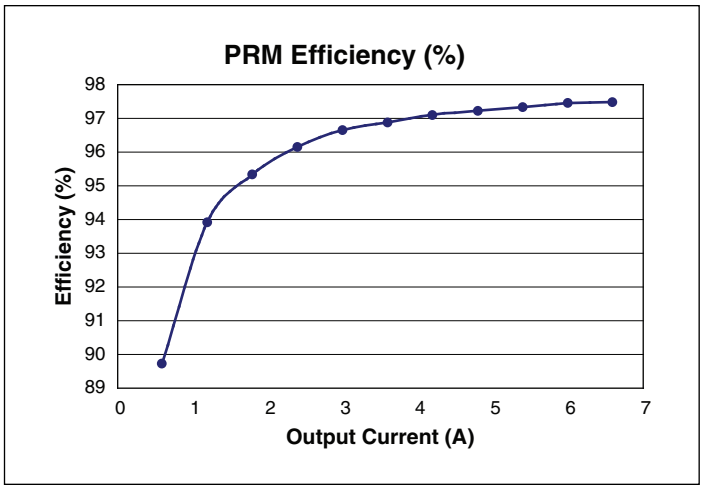
Traditional VRMs rely on the tried and trusted synchronous buck PWM converter. However, as processor voltages fall towards 1 V and below, the duty cycle from 12 V reaches 12:1 (Synch FET: Control FET). Using this PWM topology from 48 V in a high power, high efficiency system is challenging due to the extremes of duty cycle coupled with the higher FET voltage requirements and subsequent higher $R_{DS(ON)}$.
FPA enables the separation of the PWM's regulation and voltage transformation stages into two separate blocks. The PRM generates a factorized bus, controlled to a typical level of 48 V, and the VTM (a current multiplier with very low output impedance up to 1 MHz) provides high efficiency voltage transformation directly at the processor.

For the 960 W load, 8 VTMs are used (1 per 100 A processor). PRM VI Chips are capable of much higher powers (up to 320 W each) and so only four are needed (in parallel with connected outputs).

FPA delivers several key benefits:

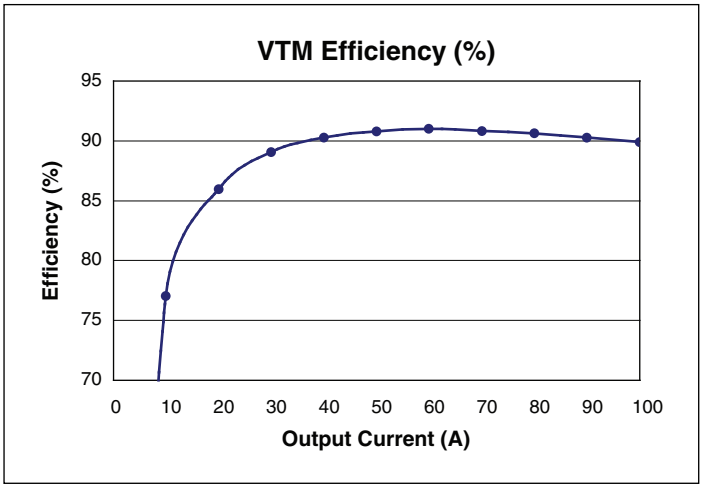
- High efficiency which allows power savings upstream (see Figures 7a, 7b & 7c).
- Physical separation of PRM and VTM
  - Allows the PRM to be placed at a distance from the VTM, with 94% reduction in distribution losses (W/Ω) at 48 V vs. a 12 V line.
  - Enables minimal form factor solutions directly at the processor (only the VTM is required to be at the processor, minimizing high current traces / losses).
- High bandwidth bi-directional transformation within the VTM uniquely enables the removal of bulk capacitance from the processor location and its replacement by a much smaller (~ 1/1000) capacitance at the factorized bus, resulting in a major reduction in bulk capacitors (used in size calculation, see Figure 7d). Owing to the VTM's high bandwidth and low Q characteristic, the ceramic bypass capacitor requirement at the POL is greatly reduced as POL capacitance is only needed to support dynamic response within a time scale of 1 uS.
- Excellent transient response (see Figure 8)

Figure 7a
PRM Efficiency



P045F048T32AL, 48 Vout, Tcase 40°C, no heatsink

Figure 7b
VTM Efficiency
Note that the efficiency is measured at 1.3 Vout to allow for drop across interconnects to processor voltage (1.2 V)



V048F015T100, 1.3 Vout, Tcase 40°C, no heatsink

Figure 7c
Phase 2
(MV and LV DC-DC replaced by PRM+VTM)
System Efficiency

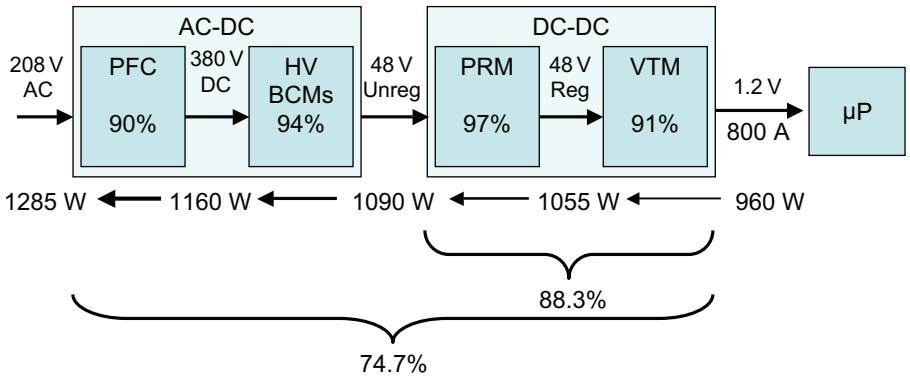


Figure 7d
Phase 2
(PRM+VTM) System Size

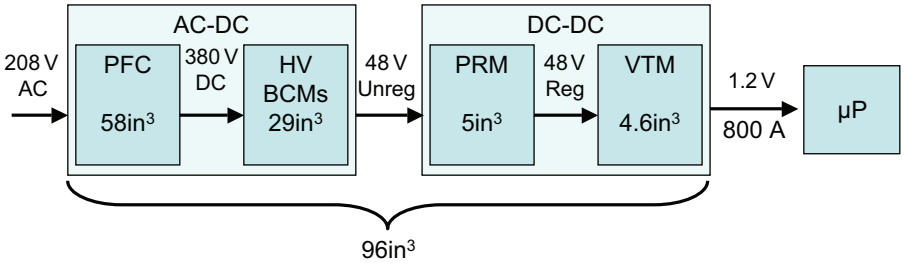
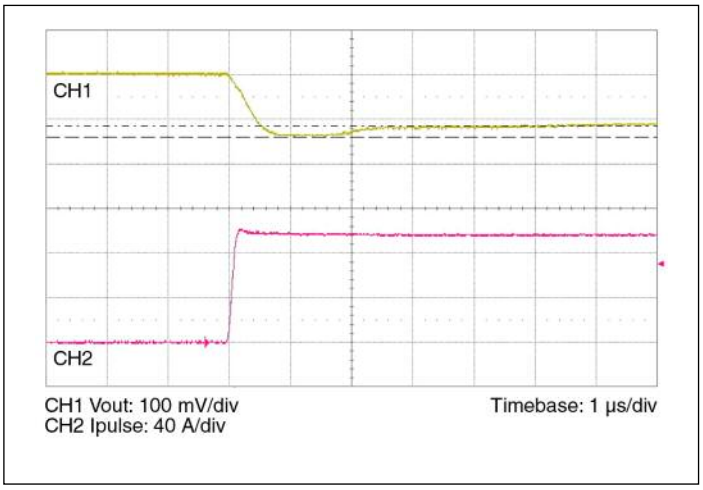


Figure 8
Transient Response of PRM+VTM Combination



48 Vin, 1.2 Vout, 0 – 100 A; 800 A/us load step; 220 uF Cout.
Less than 30 mV undershoot

Summary

For each version, the summarized power loss, size and efficiencies per stage are shown in Figures 9a, b & c below. Using BCMs to replace the HV and MV DC-DC stages (phase 1) results in a modest 1.1% overall efficiency increase but a 30% size reduction vs. the baseline system. Changing the MV and LV DC-DC stages from traditional bus converters and VRMs to an FPA solution (phase 2) means a 7.4% rise in efficiency and a 45% reduction in size vs. the original.

Figure 9a
Power Loss per Stage

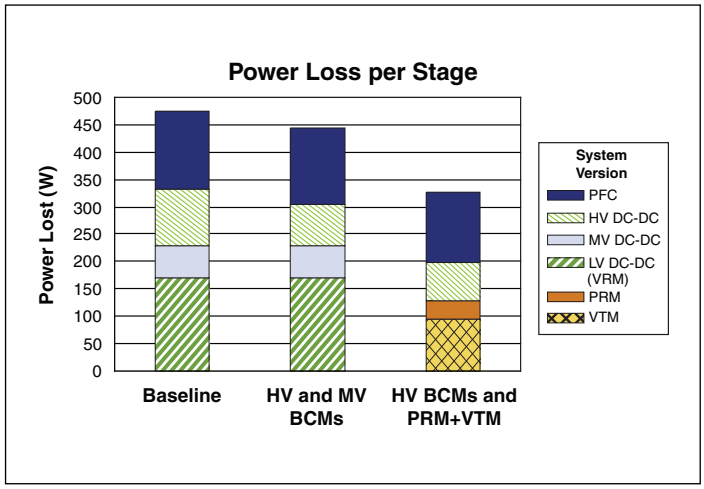


Figure 9b
Size (volume) per Stage

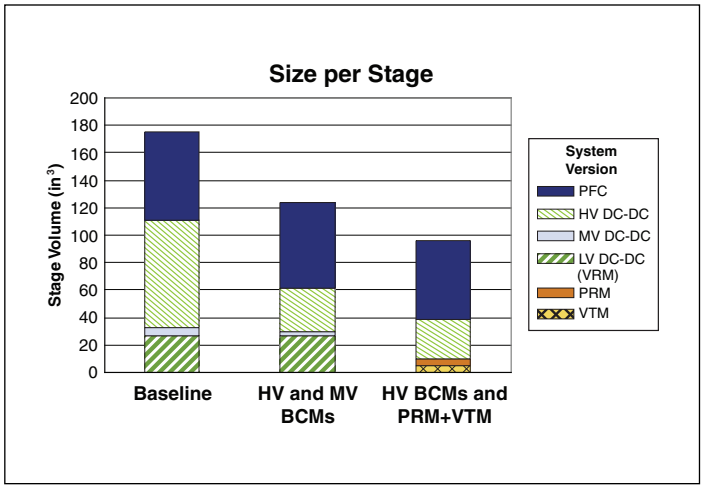
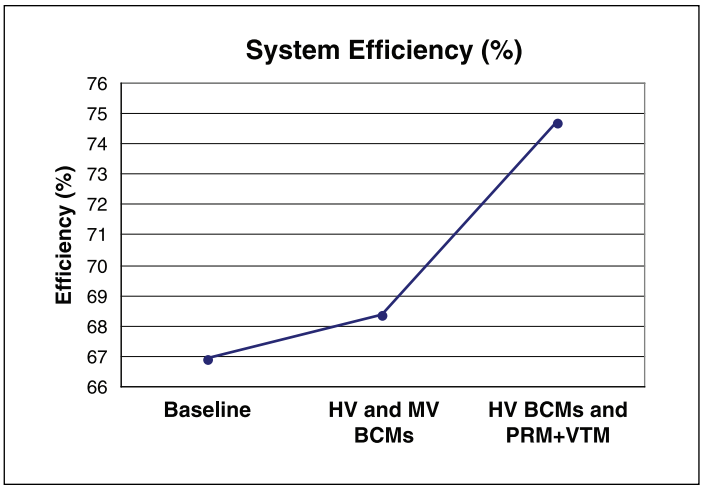


Figure 9c
Efficiency per Stage



Conclusions

The paper presents FPA building blocks (VI Chips: BCM®, PRM®, VTM®) and how they can be used to improve high power data processing system efficiency. Also, the flexible nature of FPA allows additional reductions in system distribution losses and the minimization of POL power train and bulk capacitance components directly at the processor load, thus enabling an increase in the number of processors and/or memory arrays per system board or 'blade'.

References

(1) "Future Power Technology in the Global Market" S. Strand, IBM Symposium 2005

(2) "FPA Overview"

(3) "Thoughts on Server Metrics", C.Belady, Hewlett Packard, Enterprise Servers and Data Centers: Opportunities for Energy Efficiency, 2006. Separated efficiency figures within the AC to 48 Vdc and 48 to 1.x V DC-DC stages are assumed by the author.

(4) It is noted that a small number of newly released, higher $/W 48 V output systems have become available with 15 – 19 W/in^3 power densities. A recalculation of AC to 48 Vdc size savings is required. The 48 V to 1.2 Vdc conversion size savings remain as in the main text.

(5) "IBM's Next Gen: Building Power Systems One Block at a Time", Switching Power magazine Vol 5, Issue 3, 2004.